Front-End Electronics of KOPIO Calorimeter

G.S. Atoyan, S. Dhawan, V.V. Issakov, A.A. Poblaguev, and M.E. Zeller
Physics Department, Yale University, New Haven, CT 06511

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1 Introduction

Because of the pipelined nature of the preradiator chamber readout, the entire KOPIO readout system will be pipelined in a similar manner. This allows a simplicity and coordination of data flow that is economical both financially and in developmental resources. The calorimeter front end electronics (FEE) are schematically designed with this in mind and are described below. This design will be used for other photo-detector systems in KOPIO, *e.g.*, photon vetos and preradiator scintillators, thus the material below should serve as a description of the readout for those systems.

2 The calorimeter in the L0 trigger

The calorimeter will play an important role in the lowest level trigger, L0, by providing information such as the number of photon clusters, and the energies and times corresponding to these clusters. Monte-Carlo simulation shows that a photon (which already converted in preradiator) usually produces a clump which occupies 4×4 array of modules, and which often contains isolated hits. Thus, for trigger purposes only, the calorimeter will be divided by 4×4 logical units, and will effectively look like an array of 12×12 supermodules. As shown below, energies deposited in such supermodules and times associated with them can be digitized within a few micro-bunch cycles and be used in L0. This trigger scheme is similar to those in PHENIX and LHCb, and we plan to strongly rely on the knowledge gained in the development of those systems.

3 Front End Electronics

The front-end electronics (FEE) of the calorimeter will process photodetector signals and provides energy, timing and trigger information to experiment's data collection and trigger systems. For the calorimeter this electronics will be designed to measure energies with 12-bit dynamic range ($0.5 \div 2000$ MeV) and time of arrival with respect to the beam micro-bunch clock with a nominal resolution of 50 ps and an uncertainty less than 100 ps. Operation of the FEE will be completely pipelined with dead time no more than the duration of the input pulses. It will also capable of forming and discriminating total energy signals and the total number of hits in the calorimeter.

3.1 Design requirements

Taking into account the performance requirements for energy and timing resolutions of the calorimeter and other detectors with PMT readout, we have chosen a single design with a 12-bit dynamic range for energy measurement and 10-bit dynamic range for time measurement.

The design of such a system should satisfy the following conditions:

- Shaping times of pulses less than 40 ns in order to avoid pile up between consecutive micro-bunches.
- Low-gain buffer amplifiers with adjustable gain (12 db) in order to compensate for gain variation of APDs operating with common HV.
- A fast integrator to limit the total tail noise after a 40 ns integration to less than one ADC count.
- A constant-fraction discriminator (CFD) and fast time-to-amplitude converter (TAC) for timing measurements with 50 ps time resolution.
- A fast flash ADC with a 12-bit dynamic range to cover an energy range of $0.5 \div 2000$ MeV.

- A fast flash ADC with 10-bit dynamic range has to cover a time range of 0. $\div$ 50 ns.
- Digitization of events at a 20 MHz rate, and storage in a 64-deep pipeline buffer, providing the 3.2 μs latency.
- 8-bit energy and timing measurements for the L0 trigger logic.

3.2 The design of FEE card

The design of our front-end electronics is based on the experience of the PHENIX project [1] and LCHb projects [2, 3]. A block diagram of the FEE is shown in Figure 1.

Taking advantage of the fact that the Shashlyk APD (or PMT) calorimeter system is inherently fast, it has been decided to build a system capable of measurements every micro-bunch while avoiding pileup from signals associated with the preceding micro-bunch. The APD (or PMT) pulses therefore have to be shaped to eliminate pulse tails of more than 40 ns.

The APD pulse is shortened with a clipping line about two meters long (Fig.1). The resistor-capacitor at the end of the line is adjusted to obtain a return to a zero-volt level after clipping, yielding a pulse about 20 ns (FWHM) in duration. The exact values of the parameters of this arrangement depend on the fall time of APD pulse and hence of WLS fiber used. The shaped pulses are then sent by ten meters of coaxial cables to the front-end cards located in crates on the calorimeter stand. The front-end card contains 16 channels of amplitude and time conversion. This is a convenient number for the calorimeter since a calorimeter trigger element contains 16 modules (see above).

For analog conversion each FEE channel contains the following: a low-gain buffer amplifier; a fast integrator; a 12-bit 40 MHz ADC with adjustable strobe timing; a register to synchronize the ADC output; and a 1K 12-bit memory used as a look-up table for pedestal, gain and possible nonlinearity correction. A FPGA-2 (Field Programmable Gate Array) processor, in conjunction with a second 1K 8-bit memory will compute the 4×4-sum energy E_{sum} used in the L0 trigger. Since the high volts will be applied in common, the gain of the low-gain buffer amplifier will be adjustible to compensate for photodetector channel-to-channel variations. The fast integrator will be discharged by subtraction of the input pulse in a buffer amplifier after a 40 ns delay [4].

For timing each FEE channel contains a CF discriminator with adjustable fraction threshold, a fast time-amplitude converter (TAC) with a 40 ns time window [5], a 10-bit 40 MHz ADC, register to synchronize the ADC output, a 1K 10-bit look-up memory for 'zero'-time correction and possible nonlinearity in the time scale. A FPGA-2 processor with a 1K 8-bit memory will determine a mean time, T_{mean}, for shower clusters, to be used in the L0 trigger.

Digitized amplitude and time signals from the calorimeter will be transmitted to store in the L0 pipeline buffer during the L0 latency. Data belonging to an accepted L0 trigger will be extracted from the L0 pipeline and passed to the L0 derandomizer buffer awaiting transfer to the level 1, L1, trigger. The pipeline buffer and derandomizer will be implemented as one FPGA-3 for all 16 channels. The E_{sum} and T_{mean} data, participating in the L0 trigger will be sent to L0 the trigger FPGA via a $(400 \div 600)$MHz serial link.

Digitization of calorimeter analog signals will occupy one-two micro-bunch cycle, correction of times and subtraction pedestals will take one micro-bunch cycle, transfering a digitized data in the L0 pipeline and preparation of the E_{sum} and T_{mean} data for the L0 trigger will require more micro-cycle. Thus, the total set of E_{sum} and T_{mean} data from entire calorimeter will be computed and sent to the FPGA module of the L0 trigger in $150 \div 200$ ns. It will be transmitted by 144 channels of fast serial link. In the L0 module the number of clusters, total cluster energy and average timing of each cluster will be computed. The mean position of clusters can then be compared with predicted positions from the preradiator scintillators. This information, along with data from veto detectors will then be used the as the basis of the L0 trigger. The expected time for data processing and decision making in the L0 FPGA module is three micro-bunch cycles or 150 ns.

The analog piece of the FEE - amplifier, the discriminator, the TAC and the integrator will be manufactured as a custom ASIC, as in LHCb. The remaining electronics will be constructed from commercial components: 12-bit and 10-bit 40 MHz ADCs (for example AD9042), 8-bit and 4-bit 40 MHz memories, and 472-input FPGAs. The latter will be used as processors, memories and for the organization of the pipeline buffers.

References

[1] A.L.Wintenberg et al., PHENIX Project, internal paper, 2000.

[2] The LHCb Technical Proposal. CERN/LHCC 98-4.

[3] The Front-End Electronics for LHCb calorimeters, LHCb 2000-028.

[4] Zero dead-time charge sensitive shaper for calorimeter signal processing, LHCb 2000-041.

[5] N. Harnew *et. al.*, Nucl. Instr. and Meth.**A279**, 290 (1989).

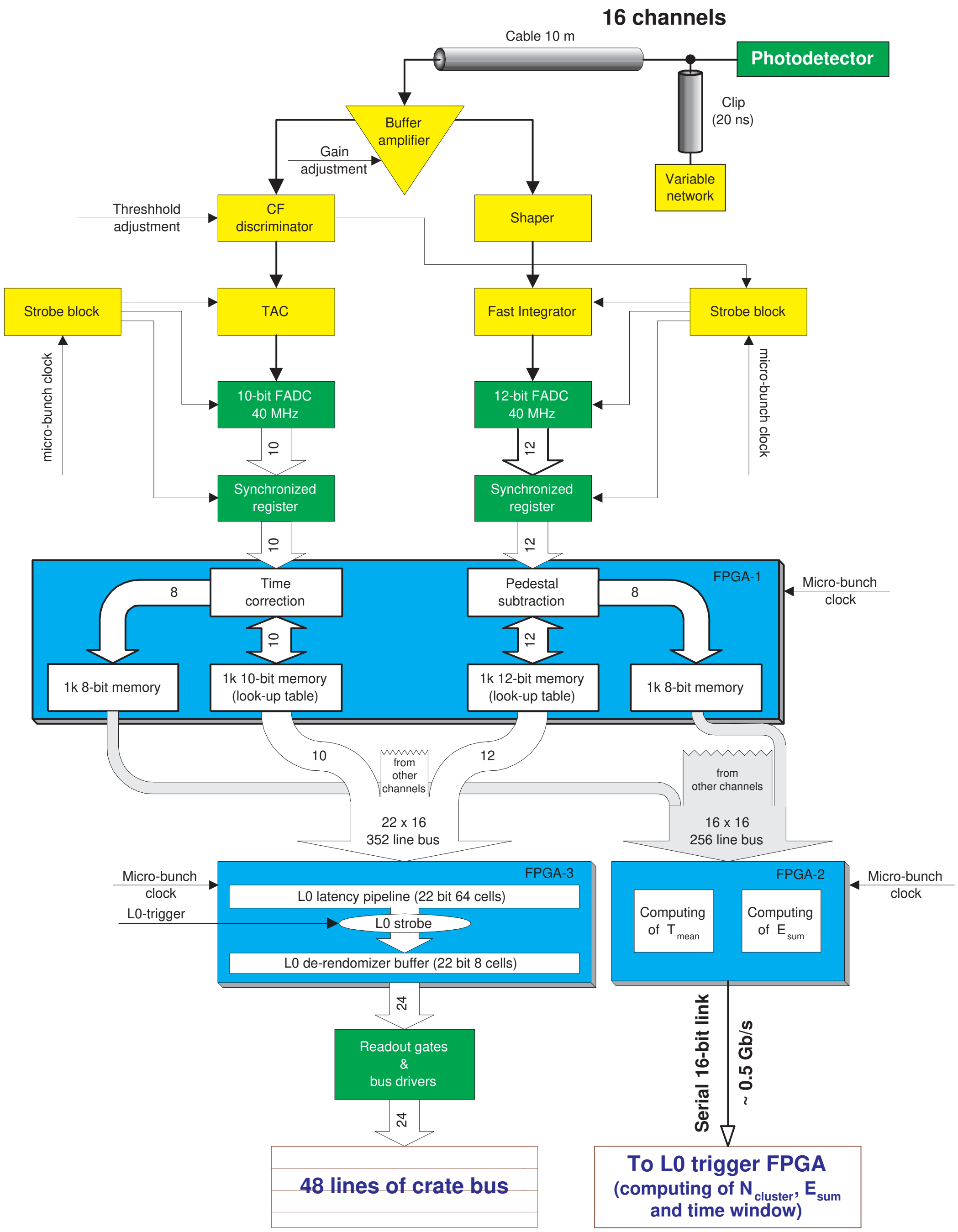

Figure 1: Schematics of custom designed Calorimeter Front-End Electronics card.