Time-of-Flight Electronics
Status Report

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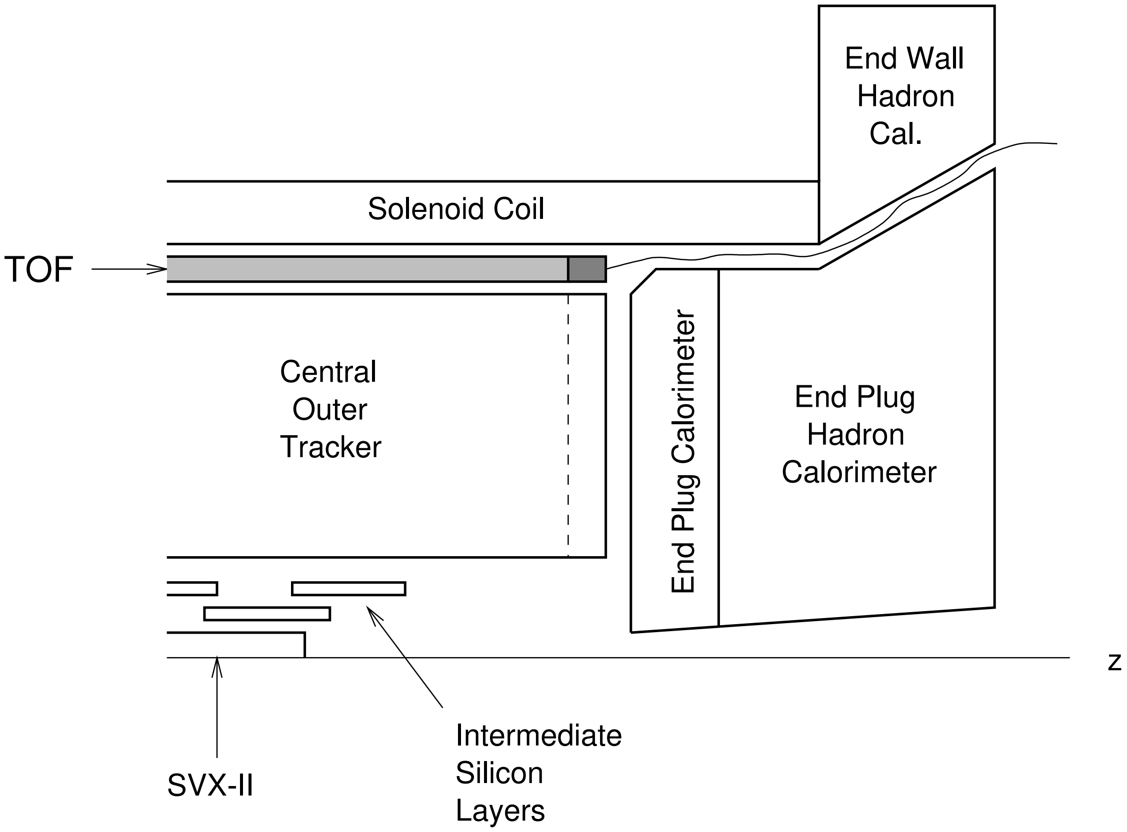
University of Pennsylvania

TOF Front-end Electronics Review

12 July 2000

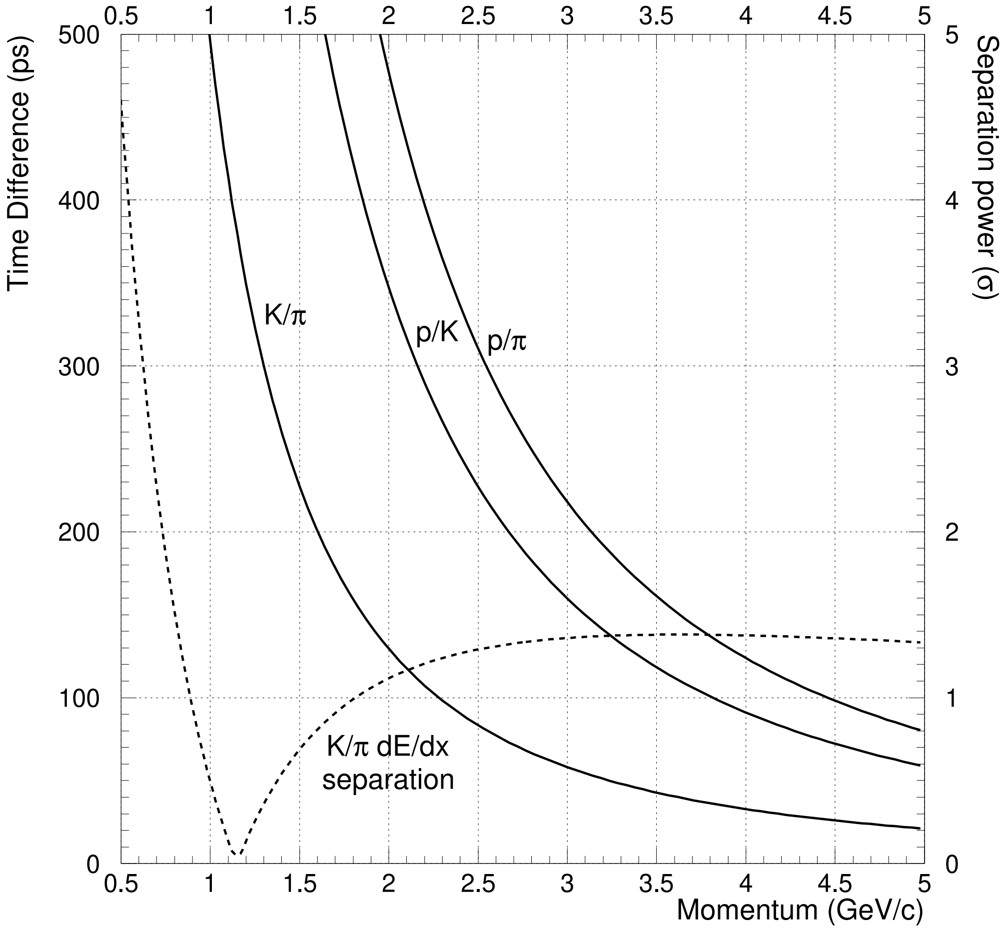
Overview of Time-of-Flight Detector



- **216 bars of Bicron BC-408, just outside COT**
  - **2.8 m long, $4 \times 4\,\mathrm{cm}^2$ cross-section**
  - **Long att. length ($\Lambda \approx 2.5$ m); Fast rise-time (0.9 ns)**
- **Hamamatsu R7761 19-stage, fine-mesh PMT**
  - **Operate in 1.4 T field (Gain loss: 500)**
  - **Small TTS (250 ns to 400 ns)**
- **Expected resolution: 100 ps (photostatistics)**

Particle Identification with TOF

Primary purpose: ***K*-id for *B* flavor tag**



With 100 ps resolution: 2σ separation of

- K and π for $p < 1.6$ GeV/c
- p and K for $p < 2.7$ GeV/c
- p and π for $p < 3.2$ GeV/c

Physics can tolerate poorer resolution

TOF Participating Institutions

Stage I approval only in Jan. 1999

9 Institutions are participating

- **Cantabria**
- **FNAL**
- **INFN Pisa and Rome**
- **KHCL Korea**
- **MIT**
- **LBNL**
- **Penn**
- **Tsukuba**

Project co-leaders:

- **Electronics: J. Kroll (Penn)**
- **Scintillator and installation: C. Paus (MIT)**
- **PMTs: F. Ukegawa (Tsukuba)**

TOF Institutional Responsibilities

Cantabria	**TOF test stand** **PMT assembly tests**
FNAL	**Mechanics, assembly, installation**
INFN **Pisa** **Rome**	**Clock and HV, PMTs** **mechanical mounts**
Korea	**PMT testing**
MIT	**Mechanics, TOF test stand,** **scintillator bar assembly,** **cables, installation**
LBNL	**laser calibration system**
Penn	**Electronics incl. cables,** **PMT assembly**
Tsukuba	**PMT procurement and testing**

TOF Signal Path

Use ADMEM to ease integration into DAQ

I. PMT to Transition Board (TB)

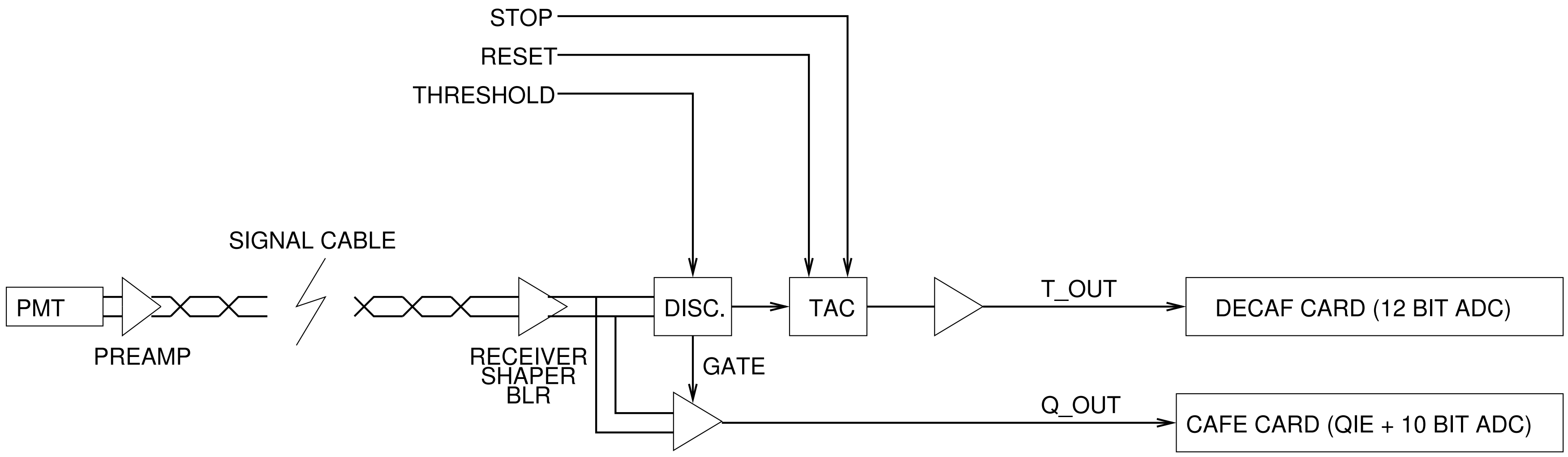
- Diff. PMT signal: anode - last dynode
- Preamplifier (gain loss in field)
- Twisted pair signal cable
- Transition board (TB) in VME crate
- Receive and split signal

  t: threshold discriminator $\rightarrow$ TAC

  Q: gated current source

II. Transition board to ADMEM

- Q goes to CAFE card (10-bit ADC)
- t goes to deCAF card (12-bit ADC)
- CAFE in even ch., deCAF in odd
- 9 PMTs per TB/ADMEM pair
  (2 spare CAFE card slots on ADMEM)


STOP
RESET
THRESHOLD
SIGNAL CABLE
PMT
PREAMP
RECEIVER
SHAPER
BLR
DISC.
GATE
TAC
T_OUT
DECAF CARD (12 BIT ADC)
Q_OUT
CAFE CARD (QIE + 10 BIT ADC)

TOF Channel Count

216 scintillator bars in 72 triplets
PMT at each end of bar $\rightarrow$ 432 PMTs

Measure time & charge of PMT pulse
$\rightarrow$ 854 measurements

Use spare slots in 8 end wall VME crates

1 TB serves 9 PMTs
(3 triplets adjacent in ϕ)

1 ADMEM serves 9 PMTs
does time and charge $\rightarrow$ 18 measurements

6 TB/ADMEMs per VME crate
$\rightarrow$ 54 PMTs (108 Measurements)

8 VME crates total
$\rightarrow$ 432 PMTs (864 Measurements)

TOF Clock Signal Distribution

Discriminator STARTs TAC

Need precise common STOP for TAC

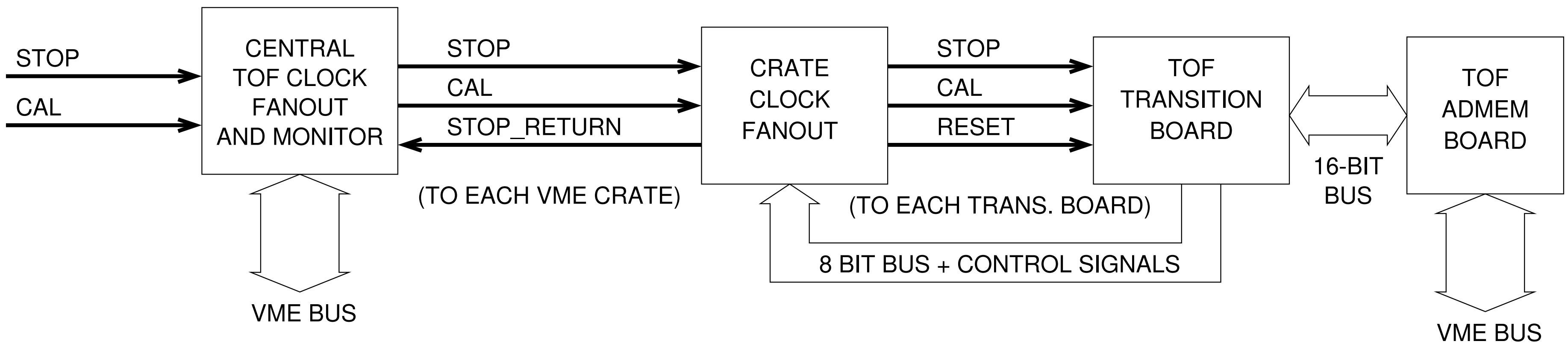
VME crates have CDF Clock (Tracer)
but jitter too large (200 ps) $\Longrightarrow$
Precise clock dist. system: Spec: $<$ 25 ps jitter

I. Central Distribution Module (1):
9U double width (connectors) VME module
Location: one of 8 end wall VME crates
Distributes signal on stand. CDF clock cable

II. Crate Distribution Module (8):
Single transition board in each crate
Location: unoccupied ADMEM slot
Distributes STOP, RESET, CALIBRATION

Adjust common STOP phase in control room

Adjust RESET via ADMEM through TOF TB.



NOTES:

1. ONLY ONE OF EIGHT FRONT END CRATES IS SHOWN.
2. ONLY ONE OF SIX TRANSITION BOARDS IN A SINGLE CRATE IS SHOWN.
3. ONLY ONE TOF TRANSITION BOARD COMMUNICATES
   WITH CRATE CLOCK FANOUT MODULE

Performance Specifications

Goal: time-of-flight resolution of 100 ps

Specifications for Electronics:
Contribute less than 25 ps to this 100 ps

Comment from Bob Kephart:

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I would request that the performance specifications of the
electronics be written down. We are attempting to achieve 100 ps overall
timing resolution. To achieve that resolution the electronics contributions
to the errors in the time measurement have to be negligible WRT transit time
spread /sqrt(Npe) in the FM phototubes.  Relevent issues include  preamp
rise times, clock stability, preamp noise, pickup noise, rise time
degradation in cables, digitization error, pedestal errors, etc.  We need to
have a budget for each contribution and a careful analysis of what the final
performance will be.
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Excellent suggestion (tough to fulfill).

Have studied some of these quantities.
But do not necessarily have hard specs

Difficult & time consuming to quantify affects:
e.g. no B field at Penn
Hard to connect quantities to resolution:
e.g. 5 ns fall time okay, but not 10 ns?

Performance Specifications cont.

Fall-time (10% to 90%) of PMT signal $\sim$ 2.3 ns
(using 1 ns pulse from blue laser) $\Longrightarrow$

Fall-time from cosmics in scintillator
Typically 5 ns after preamplifier
n.b. preamp adds only around 1 ns

Not degraded significantly
after 12 m of signal cable

Powered 36 preamps in situ
Ambient pick-up around 2 mV
Disc. thresh. $\sim$ 30 mV
(typical signal around 1 V)
So far: preamp pick-up probably okay

<u>More studies in progress:</u>

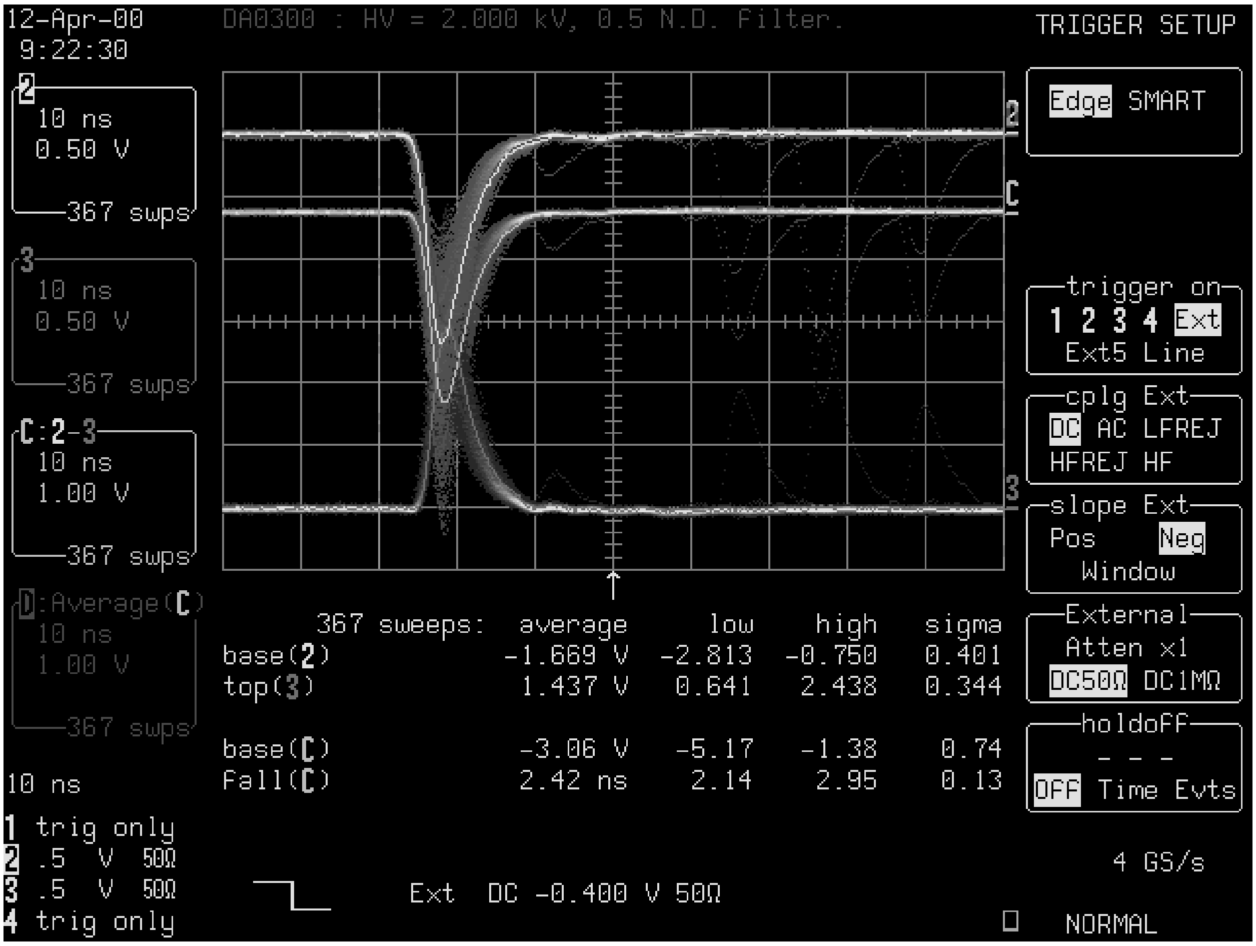
Use combined system of actual components:
2.8 m scin., silicone pad, Winston Cone,
phototube, preamplifier, 12 m signal cable,
with PMT in B field (B0 test magnet)

Example of PMT signal

Infrared laser with freq. doubling crystal

Shine blue light directly on PC

Laser pulse about 1 ns wide



Typical fall-time (10% to 90%): 2.3 ns

Status of Electronics

Component	Responsible	Status
PMT Base	Penn	installed
Preamp	Penn	installed
Cables	Penn/MIT	installed
Trans. Board	Penn	design/prototyping
ADMEM	Penn/MIT	procured/tested
CAFE cards	Penn/MIT	procured/tested
deCAF cards	Penn	design
Clock System	Pisa	
Central fanout		schematic
Crate fanout		PC board man.
LV modules	Penn	1 of 2 built
preamp power		2nd + spare soon
HV system	Rome/Penn	50% of system at FNAL: testing

TOF Electronics: Personnel

University of Pennsylvania

Faculty: J. Kroll 100% of research time on TOF)
Staff: F. M. Newcomer, R. Van Berg (available as needed)
Post-docs: M. Jones, R. Oldeman (starts mid Aug.) (100%)
Grad. Students: C. Chen, D. Usynin (100%)

University of Pisa

C. Cerri, S. Galeotti, C. Magazzu, A. Menzione
(see attached message)

University of Rome

D. Depedis, A. Di Girolamo, C. Dionisi,
S. Giagu, G. Lunadei, M. Rescigno,
plus 3 more starting 2001
(see attached message)

Message from S. Galeotti (Pisa)

Manpower is constitued by Claudio Cerri, that is the local "chairman", me (working full time to the schematics) and Carlo Magazz, that works on layouts. Claudio is supposed to be in Fermilab in August, possibly with the transition boards, I suppose to come sometime in september, with, I hope, the calibration-fanout and monitor VME9U board.

The Transition board is under construction: the PCB will be in Pisa next week, and then they will be mounted by a firm, with which we already have a commitment; the components are also almost all here.

Instead for the main calibration and clock fanout board and monitor (in CDF VME) the schematics are in an advaced state, the components are all at least ordered, and soon we will start with the layout: we have also a PCB firm that will work in august, very unusual thing here.

For the commissioning run (19th august?) we suppose to be ready with the 8 transition boards + spares, but we are not sure to be ready with the monitor card; in priciple the clock can be fanned-out by using an additional transition board, making working the whole system, without the monitor function, that will be available presumably at the end of september.

Message from C. Dionisi (Rome)

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==============>>Manpower from Rome :

 from year 2000 onward :

  Daniele Depedis 60%                                         HV
                       3 months/year at Fermilab

  Alessandro Di Girolamo ( student ) 100%                     HV
                       2 months/year at Fermilab

  Gaetano Lunadei 60%                                        Clock
                       1  month/year at Fermilab

  Stefano Giagu   70%                              lab test + analysis
                       4 months/year at Fermilab
  Carlo Dionisi   70%                                 "          "
                       3 months/year at Fermilab

  Marco Rescigno  50%    12 months/year at Fermilab (Rome contact person)

  STARTING FROM 2001 :

  Claudio Luci     30%                                          ?
  Pierferruccio Loverre 60%                                     ?
  Sandro De Cecco ( PHD student ) 100%                          ?



==============>> Schedule
>
>    plans for the commissioning run : installation of the HV monitoring
     system and analysis of the data coming up.
>
>    will entire system be ready for March 2001? yes for the HV.
                                                  ==============
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Plans and Schedule

Previous messages summarized Clock and HV

- HV ready for commissioning run
- CLOCK possibly ready for commissioning run

  Should be ready for March 2001

  Important: improve communication on Clock

Transition board and deCAF

- Main TB understood (digital functions)

  Functions have been prototyped

  Ready to start layout soon
- Continue analog DB design/prototyping
- Continue deCAF design/prototyping
- ADMEMs and CAFE cards procured/tested

  Must develop ADMEM diagnostics

Goal:

- Some production main TBs this fall
- test with prototype TB analog DB and deCAF
- Full production electronics by March 2001

Important: We need to make a schedule

Request of CDF FNAL Group

M. Jones will move to FNAL in Sept. 2000

TOF electronics work at FNAL difficult
No TOF technical support as at Penn
No dedicated TOF VME test stand

Request

VME test-stand and lab space

This could be in muon building
where we have Penn office space

Test-stand might include

- CDF 9U VME crate
- MVME processor and tracer
- PC or other terminal
- Good digital scope

Basically whatever is required
to test ADMEMs