The D0 Silicon Microstrip Tracker ⋆

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For the D0 Collaboration

Abstract

The D0 collaboration has completed building a 793,000 channel silicon microstrip tracker for the D0 upgrade. The tracker consists of 768 ladder and wedge assemblies including both single and double sided detectors. Detector readout utilizes the SVX-IIE radiation hard chip with on-chip digitization and sparsification. A brief review of the detector design is presented along with results from the assembly and testing processes. The operation of the full readout chain and the performance of the silicon tracker are described. Finally, lessons for future production of large scale tracking systems are discussed.

1 Introduction

Run IIa is now underway at the Fermilab Tevatron collider. An integrated luminosity of 2 fb^{-1} is expected for this run, with instantaneous luminosity reaching 2×10^{32} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ or ten times that of Run I. The bunch crossing times have been reduced from 3.5 μs to 396 ns, and will be further reduced to 132 ns. Significant upgrades to the collider detectors were required to accommodate these beam conditions. A major part of the D0 upgrade [1] is the addition of a central tracking system shown in Figure 1, which includes a 2 T superconducting magnet, a scintillating central fiber tracker (CFT), and a silicon microstrip tracker (SMT).

Two classes of beam interactions drive the SMT design. High-p_T processes give rise to highly collimated jets. These jets produce high track densities within a luminous region of ~ 25 cm RMS. This necessitates the construction of a long detector to achieve good high-p_T acceptance. QCD and B physics produce

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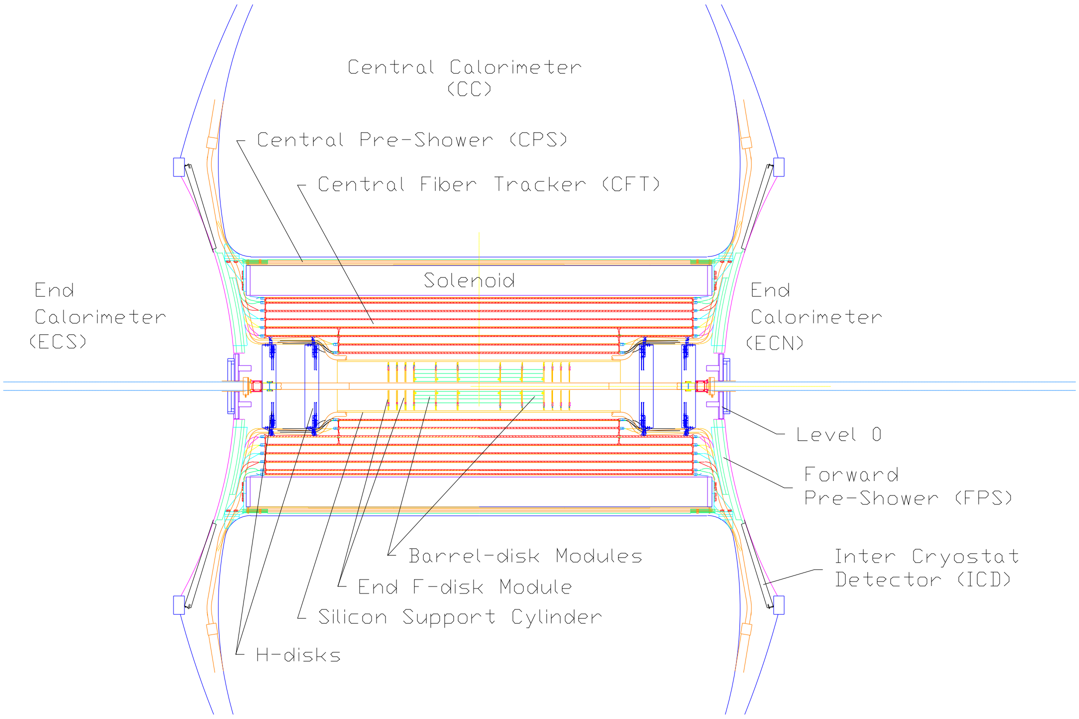

Fig. 1. The D0 central tracking system consisting of a 2 T superconducting solenoid, Central Fiber Tracker, and Silicon Microstrip Tracker. The SMT includes six barrel/F disk modules, two end modules with three F disks each, and four forward H disks.

lower p_T tracks extending into regions of high pseudo-rapidity. Resolution is optimized if tracks are normally incident to the detector, therefore disk geometries are employed in the forward regions.

Construction of the SMT was finished in December, 2000 and installation was completed in time for the beginning of Run IIa in March, 2001. Successful commissioning of the detector is now drawing to a close. Results from each phase of the SMT project will be discussed, as well as lessons from experience with the SMT thus far.

2 Design

Six barrel/disk modules are used to measure tracks with low pseudo-rapidity ($|\eta| < 1.5$). Figure 2 shows the ladder detectors in the 12 cm long barrels arranged into four layers, each with two staggered and overlapping sub-layers. An "F" disk with 12 wedge detectors is mated to each barrel. The barrels and disks yield $r\phi$ and rz measurements for efficient 3D track reconstruction in the central region. Two end modules of three F disks combined with four far-forward "H" disks provide good resolution for tracks at high pseudo-rapidity. This design should keep momentum resolution less than 10% at 1 GeV/c and

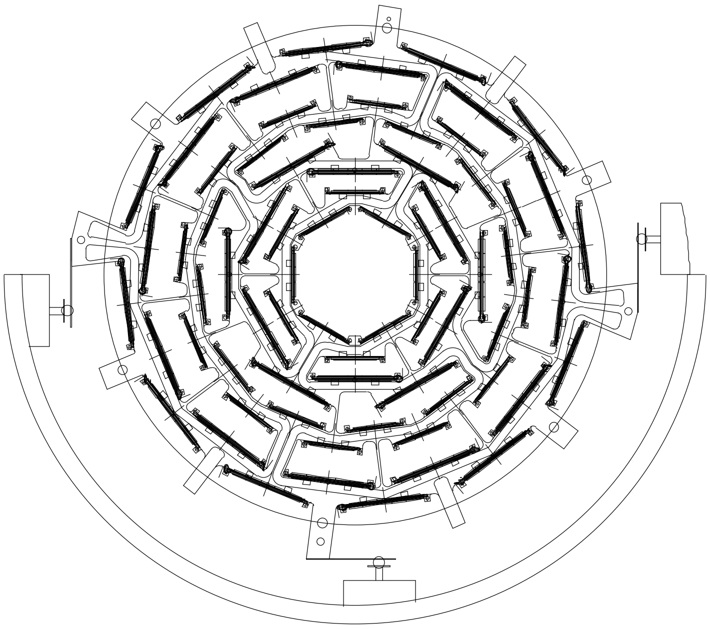

Fig. 2. SMT barrel geometry with four concentric layers of silicon ladders. The ladders in each layer are mounted onto a beryllium bulkhead in a staggered, overlapping arrangement. Alignment and cooling are provided through the precision bulkhead.

Table 1
SMT detector types

Location	Type	Stereo Angle (°)	Pitch (μm)	Number of Assemblies	Number of Chips
Barrel Ladders:					
L1, L3 (outer)	SS	0	50	72	3
L1, L3 (central)	DSDM	0/90	50/153	144	6
L2, L4	DSSM	0/2	50/62.5	216	9
Disk Wedges:					
F	DSSM	±15	50/62.5	144	14
H	SS	±7.5	80	96	12

impact parameter resolution within 30 μm out to $|\eta| < 3$.

The five different detector types used in the SMT are detailed in Table 1. The central barrels have 90° and 2° stereo double-sided sensors. Double-sided detectors are used to minimize material in the tracking volume. However, in the outer barrels, the 90° sensors are replaced with single-sided detectors because charge deposition from small angle tracks would be distributed over many strips degrading resolution. F disk wedges are comprised of double-sided sensors, and an H disk consists of 24 wedge assemblies, each with two back-to-back single-sided detectors.

Front-end readout is accomplished using the SVX-IIE chip [2]. The SVX-IIE is a 128 channel chip with a 32 cell analog pipeline depth and an 8-bit ADC. It features 53 MHz readout speed and downloadable ADC ramp, pedestal, and bandwidth settings. The SVX-IIE is manufactured with 1.2 μm rad-hard technology.

3 Assembly and Testing

All SVX-IIE chips and silicon sensors were tested prior to assembly. The chips were put through a battery of tests to verify digital and analog functionality and to exercise various control registers. The yield of chips passing all tests is 64%. Individual sensor testing included measurements of depletion voltage, leakage current, coupling capacitance, strip current and bias resistance. Various production failure modes were observed that decreased sensor yield. One failure in double-sided detectors is the micro-discharge effect caused by high fringe fields around misaligned p implants. At a limiting bias voltage, this effect causes avalanche breakdowns which produce large leakage currents and noise. The most serious problem with silicon production was lithography defects in the 90° sensors. This led to p^+ stop isolation defects, resulting in a 30% yield from the manufacturer. Yields are much higher for other types, greater than 90°% for single-sided sensors.

Assembly of individual detectors begins by mounting SVX-IIE chips and other components to a flexible kapton High-Density Interconnect circuit (HDI), which is itself glued to a beryllium substrate. The chips are wirebonded to the HDI which is then tested for electronic functionality. Then a long-term readout, or "burn-in", test is conducted for 72 hours to simulate experimental conditions. Ladders and wedges are assembled by positioning sensors relative to notches in the beryllium substrate and wirebonding the sensor to the HDI. The alignment is carried out under a coordinate measuring machine (CMM), which results in typical position accuracies of 2-5 μm for ladders and 5-10 μm for wedges. Detectors that are mechanically sound and pass a battery of electrical tests are mounted onto the barrel or disk beryllium bulkheads. This final assembly is done under a CMM, resulting in positioning accuracy of 20 μm.

The electrical testing is performed on each ladder or wedge after it is assembled. Bias voltage is applied in order to identify broken capacitors and measure the V-I characteristics of the sensors. Then a second burn-in test is conducted to measure pedestals and gain and identify noisy channels. Finally,

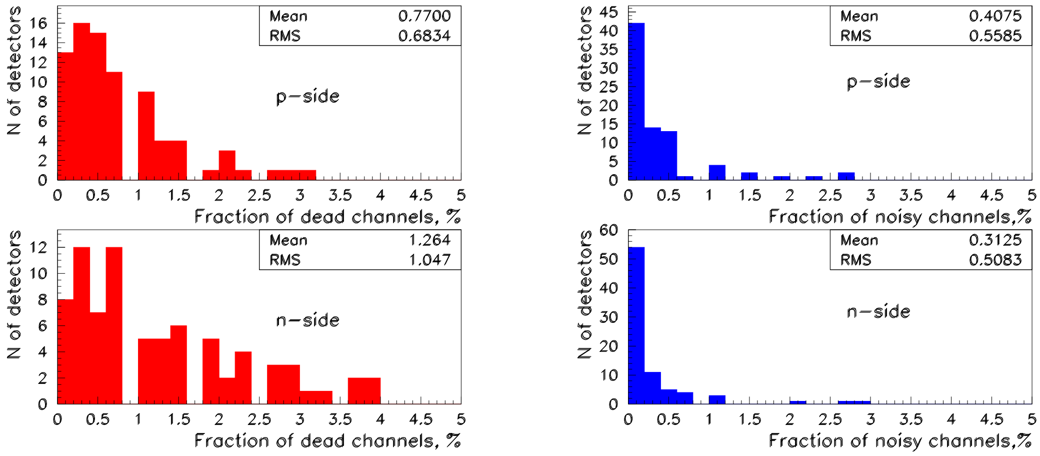

Fig. 3. Fractions of dead (left) and noisy (right) channels for 90° stereo ladders

the detector is subjected to a test in which an infrared laser is used to scan all channels of a sensor. This laser test measures depletion voltages and identifies dead channels.

Detectors are classified according to the number of dead and noisy channels. Dead channels are defined as those with a response to the laser of less than 40 ADC counts ($\sim 1/3$ the expected pulse height). Noisy channels are those which have a pedestal width greater than 6 ADC counts (three times the typical width). Only detectors which satisfy mechanical specifications and have less than 5.2% dead or noisy channels are accepted for barrel and disk assembly. The fraction of dead and noisy channels for a portion of the 90° ladders is shown in Figure 3. Averaged over all detectors, the SMT has 2% dead and 0.5% noisy channels.

The overall yield of detectors accepted compared to those assembled is 85%.

4 Readout

Figure 4 illustrates the SVX-IIE readout system. Signals from the HDIs are brought out of the tracker with 2.5 m low-mass cables, which are essentially extended flexible kapton circuits. At the face of the calorimeter cryostat, the low-mass cables connect to adapter cards which transfer the signals to 10 m high-mass cables. The high-mass cables travel to interface board crates mounted at the side of the cryostat. Interface boards refresh signals, adjust timing, distribute bias voltage, and handle chip monitoring and power management.

SVX-IIE control and data signals are passed in and out of the detector volume through high-mass cable connections to sequencer crates. The sequencers control SVX-IIE operation and convert the silicon data into optical signals

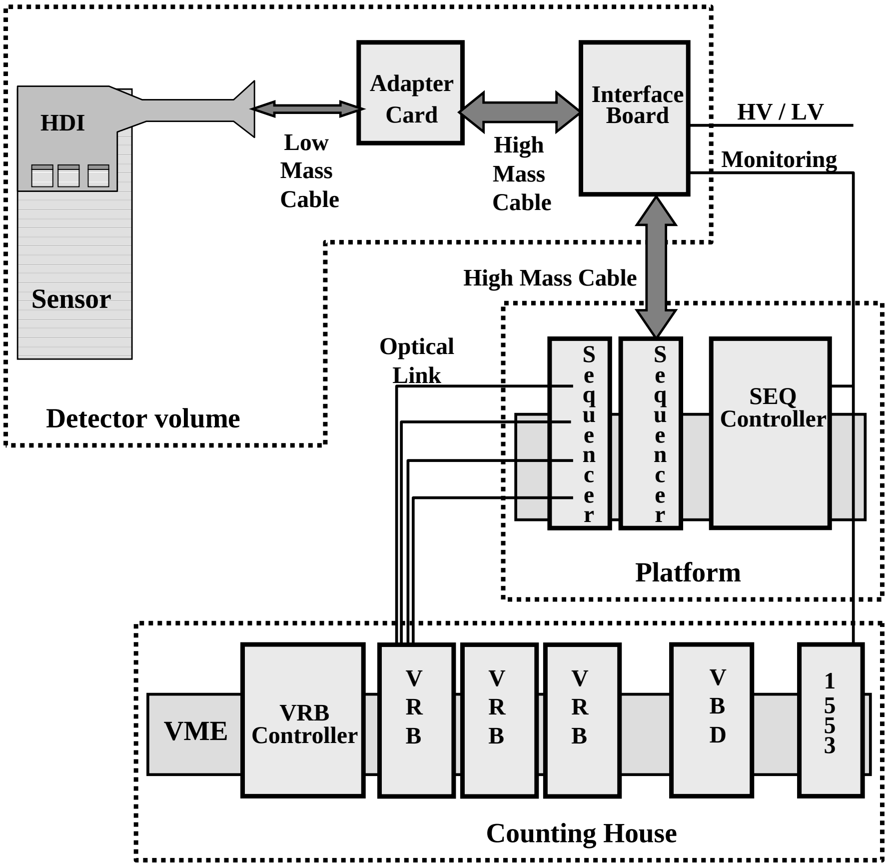

Fig. 4. The SMT readout system.

which are carried over 1 Gb/sec optical links into the counting house. There, VME Readout Buffers (VRBs) receive and hold the data pending a Level-2 trigger decision. The maximum Level-2 accept rate at D0 will be 1 kHz, which corresponds to a data output rate of $\sim$ 50 Mb/sec.

5 Installation and Commissioning

Installation of the barrels and F disks within the bore of the CFT was completed in December, 2000. The final H disk was installed in early February, 2001, and about 20% of the electronics were in place for the beginning of Run IIa in March. The final cabling and electronics installation took place during a shutdown in April, at which point the entire SMT was connected and powered.

Initially, about 15% of the detectors could not be read out. Disk wedges were two times more likely than ladders to experience readout problems. These problems ranged from bad cables and connections to failures of electronic board

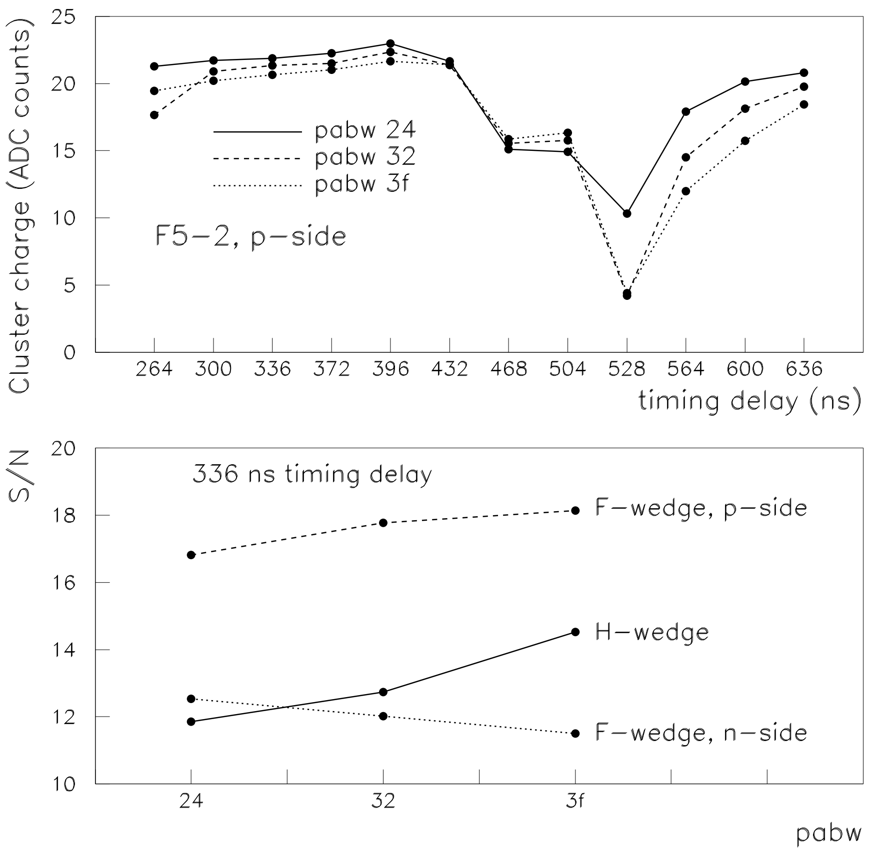

Fig. 5. Timing curve for the p side of a single F wedge (top) and signal to noise ratio for a subset of F and H wedges with a 336 ns timing delay (bottom). The parameter pabw refers to the setting of the chip integration rise time. Higher pabw corresponds to a longer rise time.

channels, HDIs and chips. Most were repaired during an extended shutdown in October. The exceptions are HDI or chip failures, which are unserviceable due to their location within the enclosed tracking volume. Now less than 5% of the detectors can not be read out.

One of the first commissioning activities is to time in the detector. This is done by optimizing the measured cluster charge collection as a function of a downloadable signal delay relative to the timing of beam crossings. A cluster is defined as a contiguous sequence of sensor strips with 6 or more ADC counts on each strip and 12 or more ADC counts for the entire cluster after pedestal subtraction. A timing curve for the p side of a single F wedge is shown in the top plot of Figure 5. The charge collection is plotted for several different values of the preamplifier bandwidth setting (pabw), which determines the charge integration rise-time. A higher pabw setting generally results in a slight decrease in cluster charge, but also a significantly larger reduction in noise.

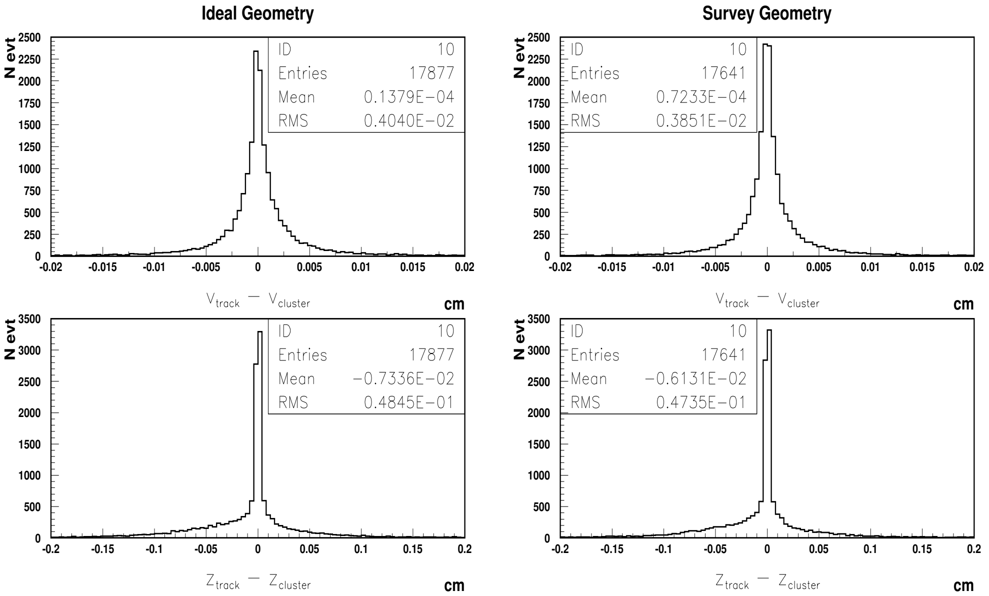

Fig. 6. Residuals using ideal (left) and survey (right) geometries. The bottom plots (Z) represent residuals in the axial, or beam direction, and the top plots (V) are of residuals transverse to the beam and parallel to the sensor.

However, this noise reduction is not observed on detector n sides. The signal to noise dependence on pabw setting for F and H disks is seen in the bottom plot of Figure 5.

Alignment studies show that the SMT has been constructed and installed with exceptional accuracy and precision. Figure 6 shows track residuals using ideal and as-built survey geometries. The difference between reconstructed track position and measured clustered positions from associated hits is plotted. The data is from magnet off runs and is reconstructed using SMT-only tracking with at least four hits per track. There is very little improvement in the residuals when using the actual survey geometry, indicating excellent internal alignment.

Track matching between the SMT and CFT confirms that the two detectors are aligned very precisely with respect to each other. In this study, tracks are found separately in the SMT and CFT. The SMT tracks are extrapolated to the first plane of the CFT at which point the track offsets are measured. These differences are plotted in Figure 7 which shows that the relative alignment of the two detectors is -28 $\pm$ 37 μm.

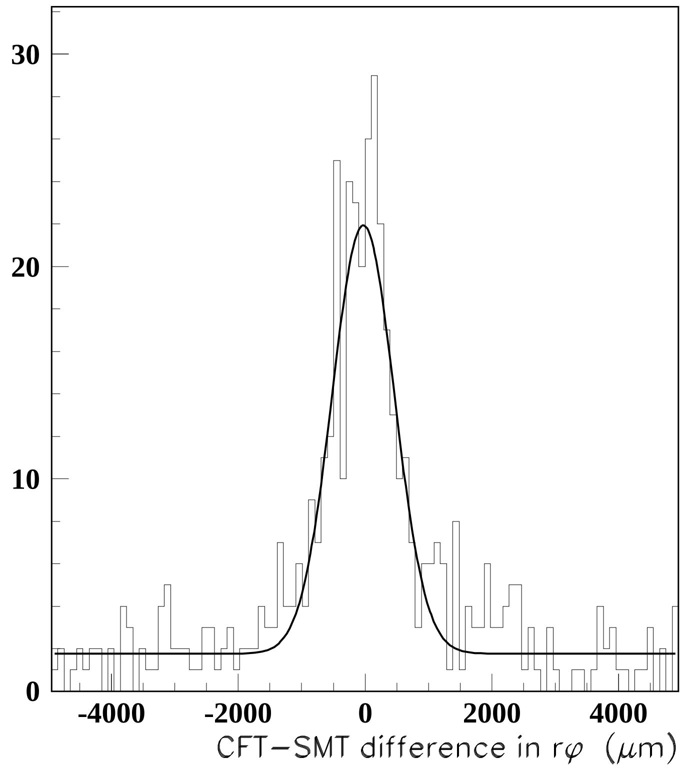

Fig. 7. SMT and CFT track offsets at the first plane of the CFT.

6 Conclusions

The D0 SMT was assembled and installed on-time for the start of Run IIa. Commissioning has progressed steadily to the point at which more than 95% of the detector is functional and included in the readout. Calibration results from the early Run IIa data show that the SMT has been constructed and aligned extremely well and is nearing stable and efficient operation.

However, several lessons were learned during production of the SMT. The relatively complicated design presented many challenges to a tight production schedule. For example, the use of five different detector types resulted in extensive logistical complications. Experience with double-sided detector production has shown that it is less reliable than that of single-sided detectors, which are also more radiation hard. This all points to building a simpler, single-sided detector silicon tracker for the Run IIb Upgrade [3], which must accommodate a very short production schedule and an integrated luminosity greater than 15 fb^{-1}.

References

[1] The D0 Collaboration, The D0 Upgrade: The Detector and Its Physics, Fermilab Pub-96-357-E (July, 1966).

[2] T. Zimmerman et al., The SVXII Readout Chip, *IEEE Trans. Nucl. Sci.* **NS 42** (1995) 803.

[3] R. Demina, these proceedings.