Back-Illuminated, Fully-Depleted CCD Image Sensors for use in Optical and near-IR Astronomy

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Abstract

Charge-coupled devices (CCD's) of novel design have been fabricated at Lawrence Berkeley National Laboratory (LBNL), and the first large-format science-grade chips for astronomical imaging are now being characterized at Lick Observatory. They are made on 300-μm thick n-type high-resistivity ($\sim$10,000 Ω-cm) silicon wafers, using a technology developed at LBNL to fabricate low-leakage silicon microstrip detectors for high-energy physics. A bias voltage applied via a transparent contact on the back side fully depletes the substrate, making the entire volume photosensitive and ensuring that charge reaches the potential wells with minimal lateral diffusion. The development of a thin, transparent back side contact compatible with fully depleted operation permits blue response comparable to that obtained with thinned CCD's. Since the entire region is active, high quantum efficiency is maintained to nearly $\lambda = 1000$ nm, above which the silicon bandgap effectively truncates photoproduction. Early characterization results indicate a charge transfer efficiency > 0.999995, readout noise 4 e's at -132° C, full well capacity $> 300,000$ e's, and quantum efficiency $> 85\%$ at $\lambda = 900$ nm.

1 Introduction

Astronomy was revolutionized in the mid-1970's by the advent of the charge-coupled device (CCD)[1]. With 30–100 times the quantum efficiency (QE) of a photographic plate, the device allowed a 1-m telescope to have the light-gathering capability of the world's largest telescopes, while extending the reach

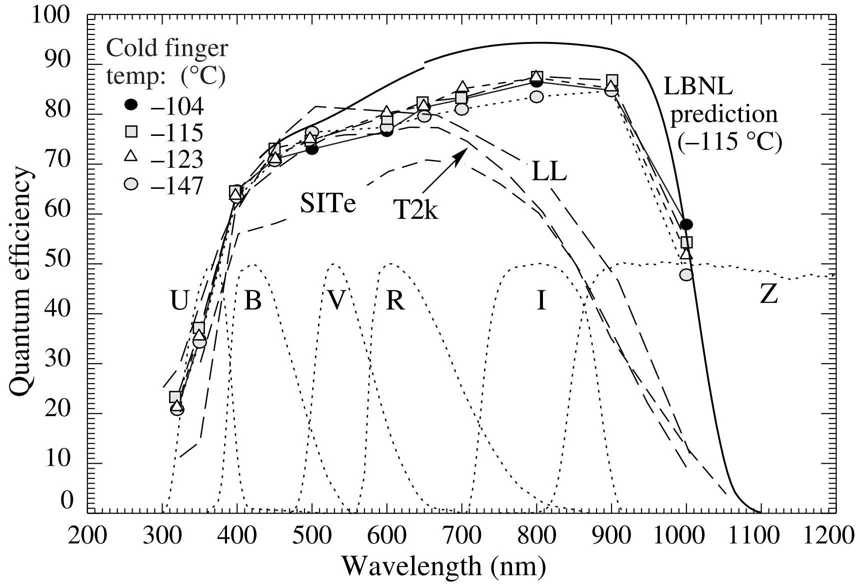

Fig. 1. *Preliminary* QE measurements for a CCD from the first back-illuminated wafer. The CCD temperature was higher than that of the cold finger. Difference between theory and experiment could be due to calibration problems or to the nonoptimal back surface quality of the first wafer. For comparison, QE measurements are shown for (a) a Lincoln Labs CCD (LL), (b) a Tektronix (SITe) CCD at Cerro Tololo Observatory (T2k), and (c) a SITe CCD recently characterized by the SUBARU telescope group (SITe). The bandpasses of the commonly used wide-band filters and a short-wavelength cutoff infrared filter (Z) are also indicated.

of the large telescopes to a substantial fraction of the observable universe. In addition, the linearity of the CCD response meant that sky light could be subtracted, and images at 1% or less of sky brightness could be observed for the first time.

But this remarkable device still has limitations. Even modern astronomical CCD's are small compared to photographic plates, necessitating ongoing development of both larger-format CCD's and cameras containing mosaics of the CCD's. The sensitive region of most scientific CCD imagers is a 30–50 Ω-cm p-type epitaxial silicon layer $\approx 20\ \mu$m thick, which is grown on a lower-resistivity p-type substrate. Blue light entering from the front is absorbed by the polysilicon gate structure. The polysilicon is transparent to longer-wavelength light, but so is the light-sensitive epitaxial layer. As a result, the QE for $\lambda \gtrsim 700$ nm falls rapidly with increasing wavelength.

In order to obtain improved QE for blue light, the CCD's in use at major facilities are thinned and back-illuminated. The original substrate is removed by mechanical and chemical means, leaving just the epitaxial layer. Special steps are taken to eliminate blue light absorption in a dead region near the back surface, which is associated with electron accumulation under a thin oxide layer. An antireflective (AR) coating is added. The resulting device

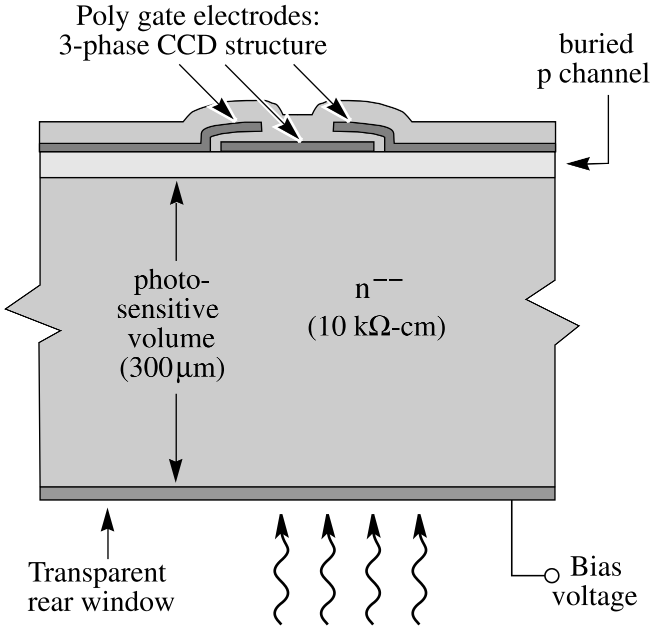

Fig. 2. Structure of the LBNL CCD. The gate structure, on top of insulating oxide and protective nitride layers, is conventional, as is the buried channel. A bias voltage on the back window/electrode depletes the entire substrate.

can approach 80–90% QE at 600 nm (see the dashed curves in Fig. 1). The transparency of the sensitive region for sufficiently red light remains, but a new problem emerges: The fall in QE in the red is accompanied by multiple reflections from the front and back surfaces, resulting in the production of interference fringes. An astronomer trying to do precision work in the I-band (centered at 800 nm) must face the Siamese twins of reduced QE and fringing. The red response is particularly crucial to cosmological observations[2,3], since the light from distant objects is substantially red-shifted.

In addition to the technical problems are those of cost and availability. The thinning process is non-standard, lengthy, low-yield, and expensive.

Using technology originally developed for high-energy physics detectors, a group at Lawrence Berkeley National Laboratory (LBNL) has fabricated large-format science-grade CCD's which appear to avoid all of the problems of thinned CCD's without introducing significant new ones[4]. The sensors are fabricated on high-resistivity n-type silicon, and are operated with the 300-μm substrate totally depleted via a potential applied to a thin back-side contact/window. (See Fig. 2.) Spatial resolution, a concern for such a thick active volume, is controlled by this bias voltage[5]. The absorption length for light becomes comparable to the wafer thickness only for $\lambda \gtrsim 1000$ nm (depending somewhat on temperature), resulting in essentially flat QE until the inevitable dropoff as the bandgap is approached[6].

In contrast to our fully-depleted devices on high-resistivity substrates, MOS

CCD's developed in support of the major x-ray astronomy missions Chandra (AXAF) and XMM have 40–80 μm thick depletion regions, due to the use of more highly doped starting silicon and the lack of a back-side bias voltage [7–9]. The XMM mission also includes a fully depleted, 300 μm thick p-n junction CCD [10]. In its present form the pn junction CCD has large pixels, (150 μm)^2, and requires two-sided lithography. The CCD reported here uses standard fabrication technologies, thus promising easy availability of much lower-cost CCD's for astronomical imaging.

We have previously reported characterization results on a small prototype CCD with high QE extending to 1000 nm [11,12]. In this work we describe initial results on the fabrication and testing of large-format devices, the largest so far being a 2048$\times$2048 (15 μm)^2 pixel CCD. Preliminary ideas for packaging which permits four-side abutability are also discussed.

2 Technology

The CCD's are fabricated in a conventional triple-polysilicon, single-metal, 10-mask process, using n-type, high-resistivity silicon. The starting material is $>$ 10,000 Ω-cm float-zone refined silicon manufactured by Wacker Siltronic Corporation. The majority of the processing is carried out at the LBNL MicroSystems Laboratory, a Class 10 clean room facility dedicated to high-resistivity silicon processing.

The gate dielectric consists of 50 nm of thermally grown SiO_2 capped by 50 nm of Si_3N_4 deposited by low-pressure chemical vapor deposition. The CCD channel is implanted with boron at a dose of 1–1.5 $\times$ 10^{12} cm^{-2}. A new feature of this run is a notch implant, used to improve charge transfer efficiency for low signal levels [13]. This 3 μm wide implant is placed in the serial register, which is relatively wide in order to allow for on-chip binning. The dose is 0.5 $\times$ 10^{12} cm^{-2}.

Conventional CCD processing requires relatively high temperatures for such steps as polysilicon oxidation and implant anneals. A concern for high resistivity silicon processing is the introduction of undesired impurities that could affect dark current and resistivity. Given that 10,000 Ω-cm corresponds to a purity level of one part in 10^{11}, care must be taken during processing to achieve low dark currents. Key to this development is the use of efficient gettering. This is achieved by depositing approximately 1 μm of in-situ phosphorus-doped polysilicon on the wafer back side near the beginning of the process [14]. A Si_3N_4 capping layer prevents oxidation of the gettering layer, which allows for efficient gettering during all high temperature processing.

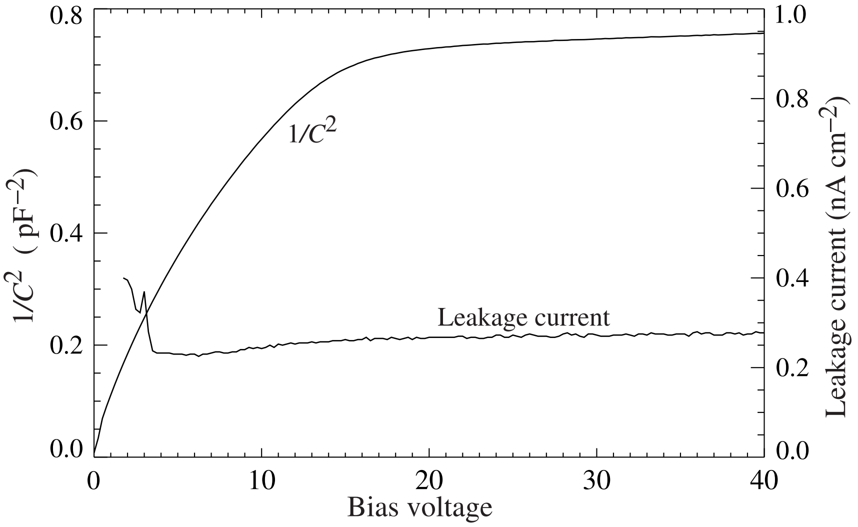

Fig. 3. Inverse square capacitance and reverse leakage current measured at room temperature on a 2 mm^2 p-i-n diode test structure from a CCD wafer.

For conventional p-i-n diode detectors such as those used in high-energy physics, the n$^+$ back-side gettering layer acts as the ohmic contact of the device. However, for back illumination this thick layer is removed and replaced by a much thinner layer in order to achieve good blue response [11,15].

Figure 3 shows dark current and inverse square capacitance measured on a 2 mm^2 p-i-n diode test structure that is included on the CCD wafers. This wafer went through the entire CCD process, including the removal of the thick back-side polysilicon and replacement by a ∼20 nm thick film. Several 950°C furnace steps are used in the process. The dark current at room temperature is about 0.3 nA/cm^2, and does not increase significantly for bias voltages above that necessary for full depletion, where the $1/C^2$ curve flattens out, indicating full depletion for $\gtrsim$ 20 V. The nominal thickness of this wafer is 280 μm.

The relatively low levels of oxygen in high resistivity, float-zone refined silicon make the material more susceptible to dislocation generation, which can lead to dark current and trapping problems [16]. All high temperature furnace steps in this process minimize thermal shock to the wafers by using slow, well controlled temperature ramp rates.

Figure 4 shows the mask layout used to fabricate large format devices on 100 mm diameter wafers. Both (15 μm)^2 and (24 μm)^2 pixel CCD's are included, with the largest device having 2048 × 2048 (15 μm)^2 pixels. Wafer-stepper lithography utilizing stitching has been used at LBNL for large-area detector development [17] and more recently for large-format CCD development at EEV and Philips[9,18]. However, for both simplicity in mask design and flexibility in the number of CCD variants possible on one wafer we choose to fabricate the large format arrays using scanner lithography. This was fa-

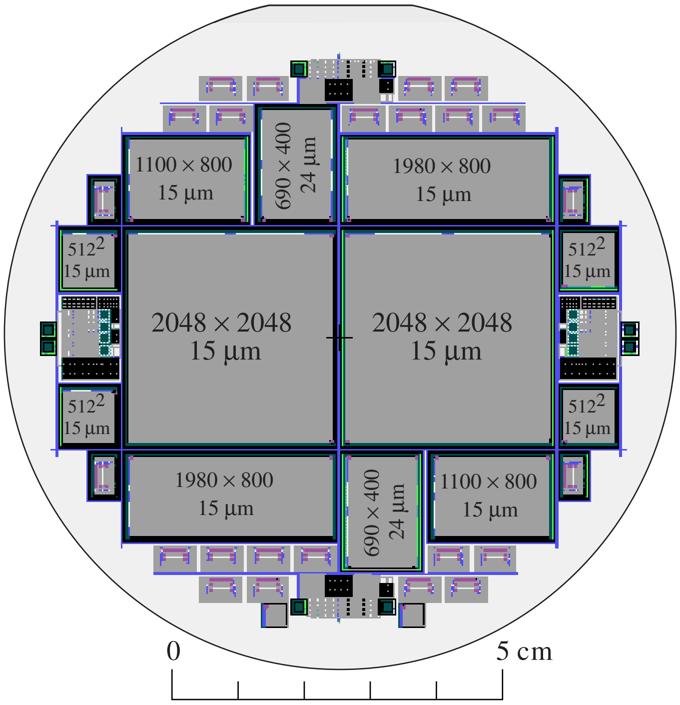

Fig. 4. Mask layout used in this work.

cilitated by the acquisition, via donation from Intel Corporation, of a Perkin Elmer 641 aligner.

3 Experimental results

The first wafer from this fabrication run was processed with the thick back-side polysilicon, and serves as a reference for subsequent back-illuminated devices. CCD's from this wafer were mounted for front illumination on a universal printed circuit board that could accommodate most of the CCD designs shown in Fig. 4. These CCD's feature a split serial register, allowing for operation with one or two amplifiers, and a split vertical register for use in either frame transfer or frame store mode. The CCD's are tested cold, typically at −120°C. So far a 400×690 $(24\ \mu m)^2$ and a 2048×2048 $(15\ \mu m)^2$ pixel CCD from this wafer have been characterized at Lick Observatory.

Preliminary results have also been obtained for a 2048×2048 $(15\ \mu m)^2$ pixel CCD from a second wafer with a back-illumination window. The window consists of ≈ 20 nm P-doped polysilicon, plus 50 nm of indium-tin oxide and 95 nm of SiO_2[6].

Charge transfer efficiency (CTE) could not be well demonstrated on the 200×200 prototype CCD. It is defined as the efficiency with which charge is trans-

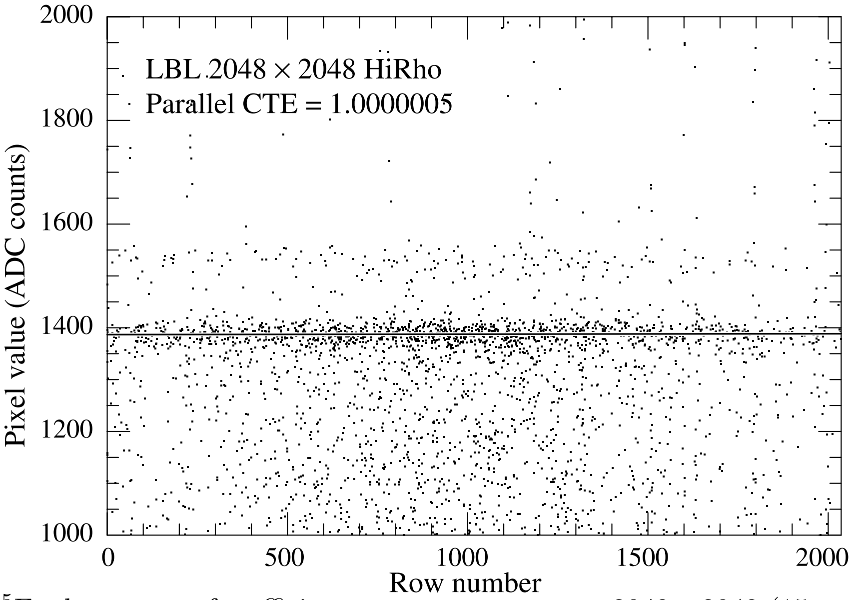

Fig. 5. ^{55}Fe charge transfer efficiency measurement on a 2048×2048 (15 μm)^2 pixel CCD. Events in the dark band (used in the fit) correspond to charge deposition in a single pixel. Charge is split between pixels in points below the band, and multiple hits produce events above the band.

fered from one pixel to the next[19], and is normally measured from the slope of the signal size as a function of row (or column) number for ^{55}Fe x-ray events, selecting events in which all of the charge was collected on one pixel. Figure 5 shows measured vertical CTE for the 2048×2048 (15 μm)^2 pixel CCD's. Similar results were obtained for the 400×690 (24 μm)^2 device and for serial register CTE. In all cases, the CTE is basically indistinguishable from unity (> 0.999995).

The output amplifier for these CCD's consists of a single-stage source follower. The output transistor has a width to length ratio of 47/6, with a 1.5 μm gap between gate and drain to minimize overlap capacitance [20]. Figure 6 shows the measured noise for this amplifier versus the sample time of the correlated-double-sampler circuitry. At the longest sample time measured (8 μs) the noise is 4.0 e rms. The noise varies approximately as the inverse square root of sample time, implying that the performance is white-noise limited over this range of sample time [19].

Dark current at -133°C was 11.8 e/pixel/hr for a 400×690 (24 μm)^2 pixel CCD from the first wafer. It was measured at a substrate bias voltage of 80 V, a factor of four or so above that needed for full depletion. The technology thus seems to be robust in terms of the amount of over-voltage that can be applied to the substrate, with implications for spatial resolution, where the standard deviation of the charge diffusion varies as the inverse square root of the substrate bias voltage[5]. No evidence for dislocations was observed, although more testing is required to determine the extent of any dislocation

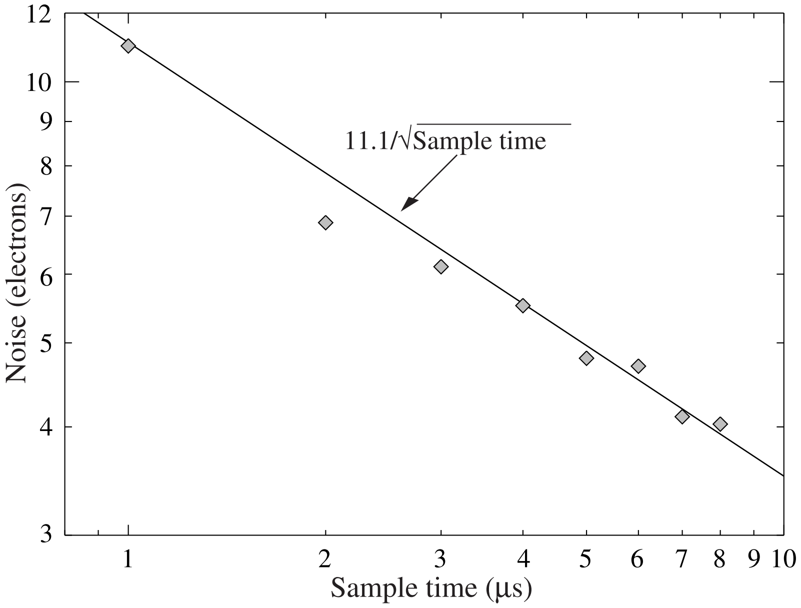

Fig. 6. Noise in electrons versus sample time for the single-stage source follower amplifier on the 400 × 690 (24 μm)^2 CCD. The CCD output is processed by a correlated-double-sampling circuit.

problem.

Full-well capacity was measured by imaging a test pattern and determining the light level at which blooming occurred. A value of ∼320 ke was measured on the (15 μm)^2 pixel 2048 × 2048 CCD from the first wafer. Nonlinearity in the amplifier was noted at ∼240 ke.

Quantum efficiency was measured on a front-illuminated 2048 × 2048 CCD using narrow-band filters. The QE peaked at a value of 56% at 900 nm, and was 39% at 1 μm. Preliminary QE measurements for a back-illuminated CCD from the second wafer are shown in Fig. 1. The predicted QE with back illumination and a two-layer AR coating is discussed in reference [6].

Figure 7 shows a test image taken with the first back-illuminated 2048 × 2048 CCD, demonstrating the cosmetic quality of the device.

4 Packaging with four-side abutability

In a thinned CCD, pad contacts are etched through the wafer and are available at the back surface. The packaging normally includes a circuit board to which external cabling is attached and to which wire bonds are made to the CCD pads. This arrangement substantially extends the dimensions of the package on any CCD edge with pads. Thus if a mosaic is extended in the direction of any CCD edge with pads, close abutment is impossible and the cabling obstructs

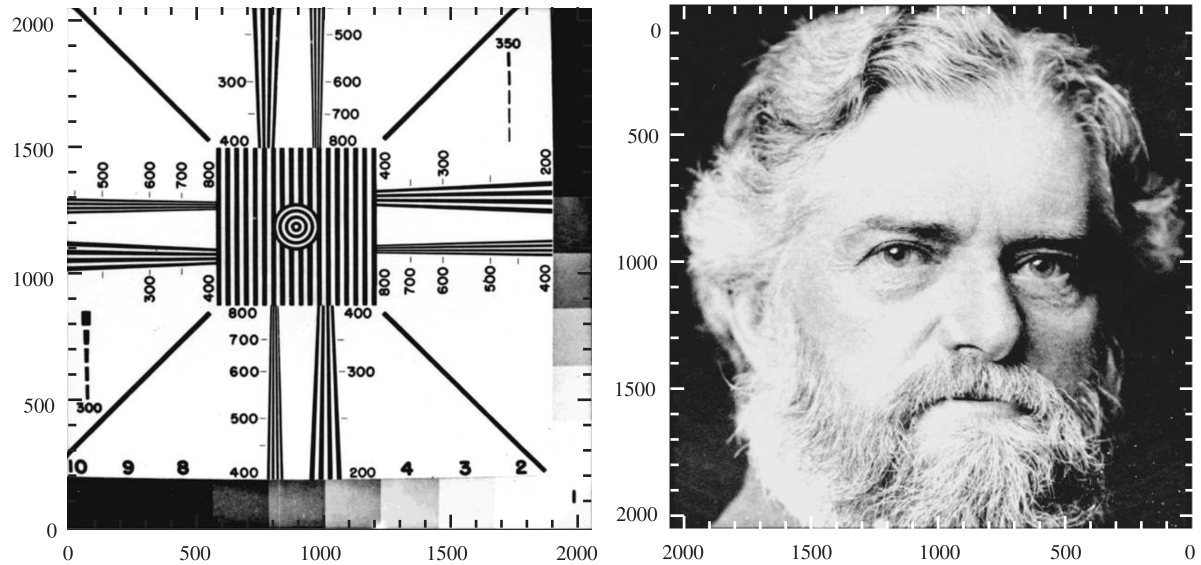

Fig. 7. Test image (of Simon Newcomb) taken with the first LBNL back-illuminated 2048×2048 CCD.

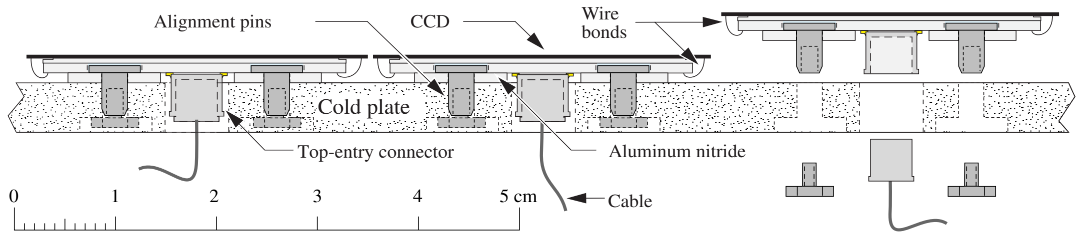

Fig. 8. Conceptual design for total-depletion CCD packaging. The CCD is cemented to a three-layer aluminum-oxide subassembly described in the text.

light. These problems are normally dealt with by making the connections to one (or two adjacent) CCD edges, achieving two- or three-side abutment[21–26]. Pixel-to-sawcut distances of 240 μm or better have been achieved. In some cases, as in the Big Throughput Camera (BTC)[27] and the Sloan Digital Sky Survey mosaic[28], wide gaps between the CCD's are allowed. This format is not appropriate for spectroscopy, but it is acceptable for imaging except for the loss of high-quality image area. Bump-bonding methods to permit four-side abutment are also being investigated[29].

For our thick CCD's, back surface access to the pads is not possible. In a packaging scheme under development, the pad edges of the chip cantilever from a 3-layer aluminum-nitride structure. The first is a thin insulating layer cemented to the front of the CCD. The second is a circuit board with edge pads to which the CCD pads are wire-bonded. (Wire-bonding to the unsupported cantilevered chip has been successful.) The traces go to a center top-entry miniature connector through which cabling is brought out perpendicular to the CCD package and through the cold plate. The third layer is an additional insulator which also captures three indexing pins. Screw-on extensions to the pins facilitate installation, removal, and handling. Four-side abutability and a certain amount of assembly jigging is therefore automatic. This scheme is shown in Fig. 8.

On the other hand, several times the 300-μm wafer thickness must be allowed between the pixels and the sawcut because of the need to bring the depletion field to zero before the cut is reached. This results in an inactive edge which is about 1 mm wide along the sides of the chip and slightly wider along the ends with pads.

5 Conclusions

Several important milestones have been reached in the development of fully-depleted back-illuminated CCD's at LBNL. Scientific quality charge transfer efficiency has been demonstrated on a 2048×2048 CCD. While based on limited statistics, the yield seems to be quite high. Noise, dark current, and full well capacity have been measured and are adequate for most science applications. Acceptable cosmetic quality has been obtained with most chips, front and back illuminated. Preliminary QE measurements with back-illuminated devices demonstrate the expected high red and IR quantum yields. Since pads are not accessible from the back side, the easiest packaging schemes under discussion provide four-side abutability.

Note added in proof

The calibration problem in the measured quantum efficiency (Fig. 1) has been solved, and the data now agree with the model prediction. They also agree with independent measurements of the reflectivity in the region where surface effects are not important.

In addition, the packaging scheme described in the text and in Fig. 8 has been very much simplified. A single aluminum nitride circuit board is now proposed, to which "wide-head" indexing pins are cemented.

Acknowledgement

This work was supported by the U.S. Department of Energy under contract No. DE-AC03-76SF00098.

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