National Institute for Nano Engineering

Atom Chips at Sandia

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Much like laser cooling in the 1990's, atom chip technology today is rapidly gaining popularity as a convenient and powerful approach to achieving precise control over an atom's motion and internal state. While great success has been achieved in magnetically manipulating the atoms, integrating optical elements onto the atom chip is an active area of research. Premier applications for these "optoatomic circuits" can be foreseen in both quantum information science[1] and in quantum sensors.[2]

At Sandia, our efforts are focused on developing atom chips for quantum information processing applications in collaboration with researchers at the University of New Mexico and California Institute of Technology. Our atom chips will contain patterned conductors forming magnetic traps and guides integrated with open access optical cavities. Although at first, the magnetic trapping chips and the optical cavities will be developed separately, later efforts will be focused on integrating the fabrication process.

1. H. Mabuchi, M. Armen, B. Lev, M. Loncar, J. Vuckovic, H. J. Kimble, J. Preskill, M. Roukes, and A. Scherer, *Quantum Information and Computation,* **1**, 7 (2001).
2. Y.-J. Wang, D. Z. Anderson, V. M. Bright, E. A. Cornell, Qu. Diot, T. Kishimoto, M. Prentiss, R. A. Saravanan, S. R. Segal and S. Wu, *Phys. Rev. Lett.* **94**, 090405 (2005). T. Schumm, S. Hofferberth, L. M. Andersson, S. Wildermuth, S. Groth, I. Bar-Joseph, J. Schmiedmayer, P. Kruger, *Nature Physics*, **1**, 57 (2005).

Collaborators:

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Hideo Mabuchi, Stanford University

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

Magnetic Micro Traps

Goals

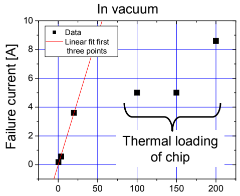
- High current carrying capability.
- Low sidewall roughness
- Multi layer capability
- Top surface mirror for mirror-MOT as close to the conductors as possible

Properties of current atom chip

- Wire material: Al, 0.5% Cu
- Substrate material: Si
- Wire thickness: 2.5 μm
- Distance from wire to mirror: 1.5 μm

Failure current of Al wires

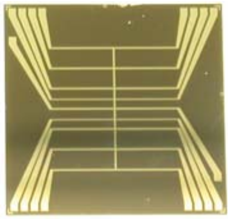
In vacuum



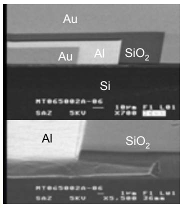
Conductor width [μm]

Ideal scaling of maximum current:
$I_{max} \alpha\, wh^{1/2}$

The atom chip

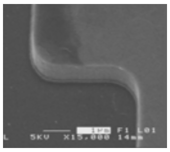


Prior to SiO_2 and Au coating
Caltech conductor pattern



Cross section of the atom chip
across a wire bonding pad

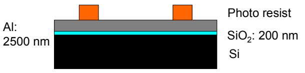
Al wire sidewall



SEM image

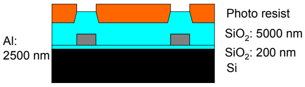
Patterned Conductor Fabrication

Deposit Al (0.5% Cu) and photo resist. Pattern photo resist.

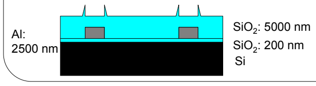


Cl plasma etch the aluminum

Deposit SiO_2 and photo resist.
Pattern photo resist.

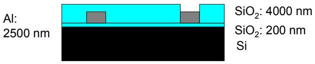


Block out plasma etch



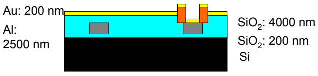
Chemical mechanical polish

Deposit photo resist and pattern.
Etch SiO_2 for contact pads or vias.

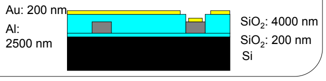


After this step the process can be repeated to add another layer of wires.

Deposit photo resist and pattern.
Deposit gold mirror (Ti/Pt adhesion layer).



Lift off resist



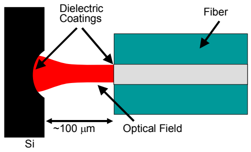
Engineered high finesse micro optical cavities

Optimized fabrication gives smooth micro-optical cavity templates

Goals

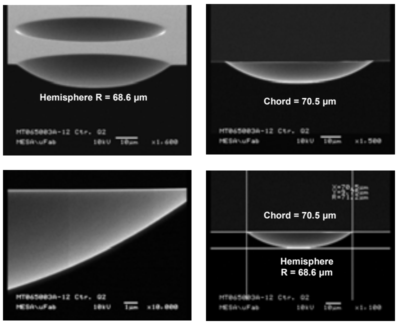
- Open access Fabry-Perot cavity
- Finesse > 10,000
- Low mode volume
- Process compatible with Al wire process

Cavity design



M. Trupke, E.A. Hinds, S. Eriksson, E.A. Curtis, Z. Moktadir, E. Kukharenka, M. Kraft, *Appl. Phys. Lett*. **87**, 211106 (2005).

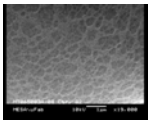
1 μm SiO_2 aperture, 60 min F* chemical downstream etch,
100 μm SF_6 plasma smoothing, 2 μm oxidation + strip



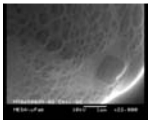
Silicon substrate type

Before plasma etch
1 μm SiO_2 aperture

High resistivity Si

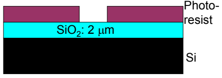


Low resitivity Si

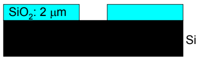


Spherical mirror fabrication

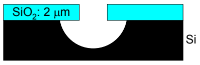
Deposit SiO_2 and photo resist.
Pattern photo resist.



Plasma Etch SiO_2

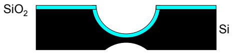


Chemical downstream etch with fluorine radicals



Strip SiO_2 with HF.
Smoothing etch with SF_6 and Ar plasma.

Thermal oxidation smoothing.



Strip SiO_2 with HF.

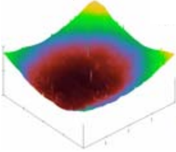
Surface Roughness

AFM measurements at bottom of mirror

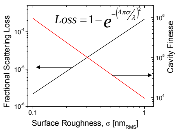
Units: nm_{rms}; 1 μm SiO_2 aperture

Wafer	1st plasma etch	2nd plasma etch	Oxidation	Anneal	Wet etch
1	1.13	0.67	-	-	0.30 cavity 0.30 field
2	0.98	0.62	0.55	0.48 well 0.66 field	0.46 cavity 0.58 field
3	0.94	0.85	0.48	Yes	0.216 cavity 0.218 field

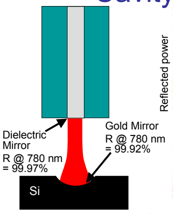
Post 1st plasma etch
AFM scan, Wafer 1

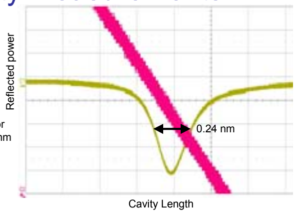


Scattering loss v. surface roughness



Cavity Measurements



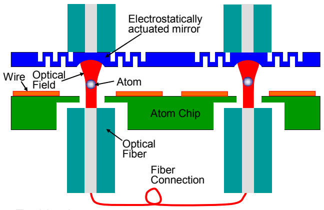


Measured at 852 nm: **strong coupling regime**

Finesse = 1750
Expected Finesse = 2400
Cavity Length = 15 μm
Q = 60,000

$g_0 = 3.3 \times 10^9\ s^{-1}$
$\kappa = 6.7 \times 10^9\ s^{-1}$
$g_0^2/\kappa\Gamma = 36$

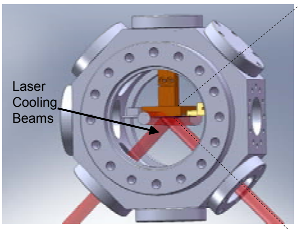
Integrated Opto-Atomic Circuit



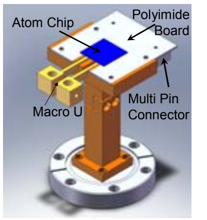
- Enable photon mediated interactions between atoms trapped in optical cavities.
- Trap atoms in a remote mirror-MOT and magnetically transport to the individual cavities.

Sandia Atom Chip Testing Apparatus

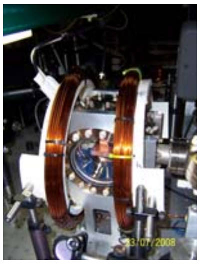
- Atom chip testing apparatus assembly including vacuum chamber and laser systems is complete
- 1st Experiments: make mirror-MOT and then magnetically trap atoms on the atom chip
- Chamber has good optical access
- Atom chip is mounted on a polyimide circuit board
- Rapid changing of the atom chip with a modular design.
- DFB lasers with frequency offset locking for the MOT.

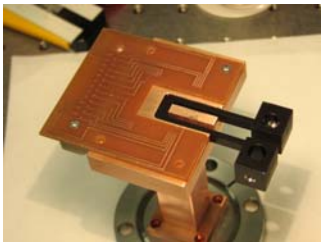


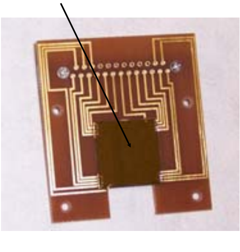
Atom chip mounted in a spherical octagon



Atom Chip Assembly







First Atom Chip shipped to Mabuchi Group March 2008

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