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Radiation Hardness of the SVX4 Preamplifier Chip

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Abstract

A sample of SVX4 preamplifier test chips in $0.25\ \mu$m CMOS technology was exposed to ionizing radiation of ≈ 20 Mrad. A single chip was exposed to ≈ 40 Mrad. The preamplifier signal shape, rise time and gain are found to be unaffected by the irradiation. A small but significant shift of the preamp bias voltages is observed. The largest shift is -115 mV after 40 Mrad which is equivalent to a PMOS transistor threshold voltage shift of -80 ± 20 mV.

1 Introduction

This note summarizes the irradiation measurements performed on a prototype preamplifier for the SVX4 read-out chip. The SVX4 chip is currently being developed by FNAL, LBNL and Padova. It will read out the CDF and D0 silicon detectors upgraded for Run 2B. The functionality of the chip corresponds largely to the existing SVX3 chip [1] thus providing digitized output signals with zero-suppression and pedestal subtraction in dead-timeless operation. The SVX4 chip will be produced in TSMC 0.25 μm technology in order to withstand the maximum expected radiation dose of ≈ 20 Mrad of Run 2B. The preamplifier circuit is described in [2].

Three preamplifier test chips were exposed to ionizing radiation at the ^{60}Co γ source of the DMEA irradiation facility in Sacramento, CA [3]. The test chips were powered during irradiation and a clocked reset signal was applied. Regular measurements of the preamp bias voltages, output signal voltage and signal rise time were performed. The measurements are compared with HSPICE simulations using post layout simulations of the test chip including parasitic capacitances.

2 Experimental details

The external circuitry of the preamp chip is similar to that described in [2]. The bandwidth bits of the three preamplifiers are set to bw0 = 2.5 V and bw1 = 0 V, leading to an expected rise time of ≈ 50 ns for 10 pF detector capacitance and no ringing even for a detector capacitance (to ground) as small as 0 pF. In order to measure the noise, the input and output of the preamplifier are shorted by a 10 MΩ resistor providing a continuous reset. The on-chip buffer (inverting amplifier) is

chip	channel	capacitance [pF]	max. dose [Mrad]
#4	11	33	42
#5	0	10	19
#5	4	27	19
#5	11	56	19
#6	0	10	23
#6	4	27	23
#6	11	56	23

Table 1: Detector capacitance and absorbed dose of irradiated chips.

operated with an external 1KΩ resistance instead of 500 Ω. The test chips are powered during irradiation and a clocked reset signal is applied. The corresponding cable lengths are aproximately 2 m as requried by the dimensions of the radiator vessel.

Signal waveform, maximum output voltage, rise time, and noise measurements are performed on seven channels distributed over three chips. The preamp bias voltages of the chips are also measured. The measurements are typically performed every 3 Mrad of absorbed dose. During the measurements the clocked reset is switched off by setting PARSTB to 2.5 V. The chip output signals are connected to a low noise (2nV/$\sqrt{\mathrm{Hz}}$) amplifier CLC425 providing an additional output voltage amplification to facilitate the noise measurement.

During irradiation the chips are located in a lead-lined aluminum filter box in order to achieve spectrum hardening and charged particle equilibrium [4]. The dose rate in the box at the chip location is measured before or after the irradiation with a small NIST calibrated ionization chamber which is accurate to $\approx$ 5% [5]. The total absorbed dose is given by the measured dose rate times the irradiation time. The precise positioning of the ionization chamber at the chip position is important to make a precise dose measurement. We estimate the uncertainty of the absorbed dose to be $\approx$ 20% from the spread of independent dose measurements at the same chip location. The irradiator temperature was about 29 °C during the 6 hours of irradiation, the room temperature was $\approx$ 23 °C. The on-chip temperature was not measured.

The maximum dose per chip and the chosen detector capacitances for each channel are listed in table 1. Chip #4 was irradiated longer than the others and received a dose of 40 Mrad.

3 Results

3.1 Bias voltages

The bias voltages measured before and after irradiation are summarized in table 2. The nominal bias node voltages obtained from HSPICE are also given. The bias voltages of chip #4 before irradiation are unknown, unfortunately. A selection of the results is also shown in figures 1 and 2.

Numerical values are listed in table 2.

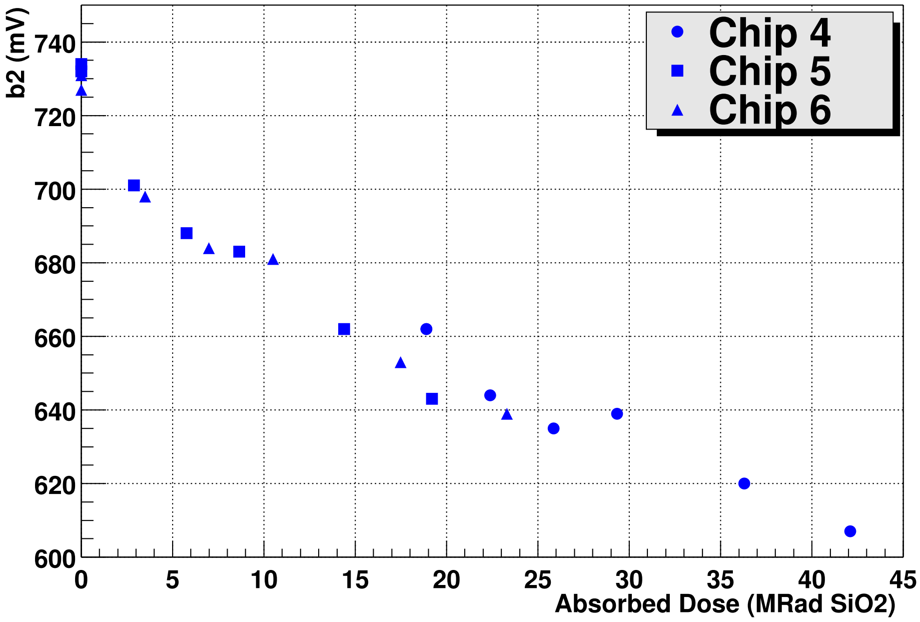

Figure 1: Bias voltage b2 as a function of absorbed dose for three chips.

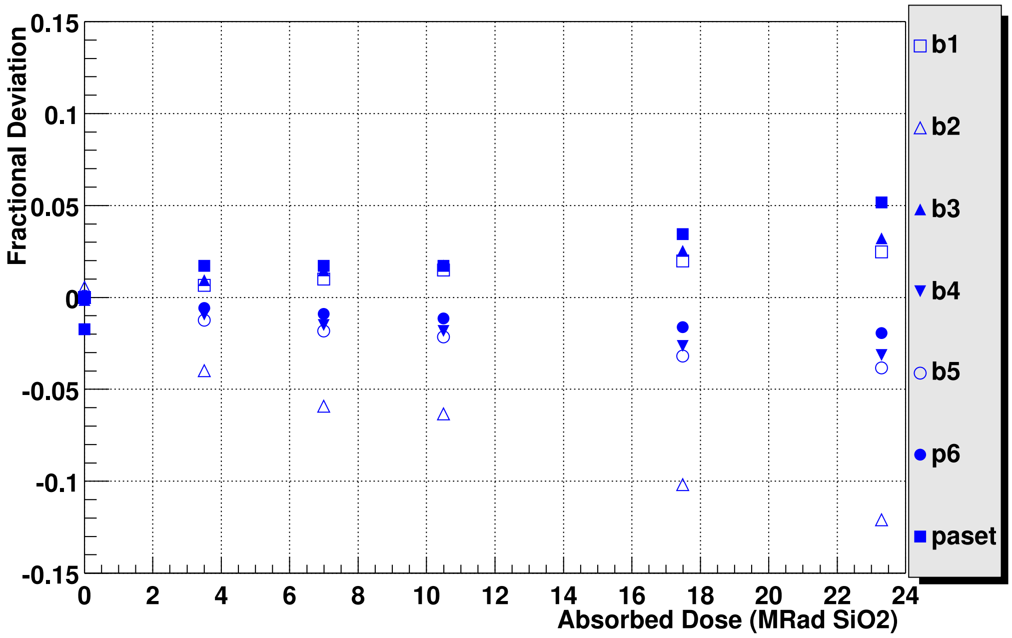

Figure 2: Change of bias voltage b1 - p6 as a function of absorbed dose for chip 6.

We observe a mild variation of the bias voltages during our measurements due to the different air temperatures in the irrradiator and in the area where we measured the bias voltages. This leads to an uncertainty of the bias voltage b2 of $\approx$ 4 mV. The temperature effects on the other bias nodes are negligible which is consistent with HSPICE simulations performed at different chip temperatures.

The measured bias voltages at corresponding irradiation levels agree within a few per cent. A difference of 19% is found between simulated and measured (before irradiation) bias voltages for the node b2. The other voltages agree with the simulation to better than a few per cent.

Significant radiation effects are observed for most bias voltages. The largest change, a drop by $\approx$ 115 mV, is found for the b2 voltage. The second largest shifts are for the b4 and b5 voltages. These changes can be described by a global change of the PMOS transistors threshold shift of $-80\pm$ 20 mV over 40 Mrad in the HSPICE simulations. E.g. the threshold voltage of the PMOS transistor connected to the node b2 is expected to change from the nominal value of -606 mV to ≈ -690 mV. The simulated bias voltages for various threshold variations and temperatures are listed in table 3 (appendix).

Considering chips 5 and 6 only, we observe a threshold shift of $-56\pm$ 4 mV in 20 Mrad. The data suggest that the radiation damage does not increase linearly with time but that the first few Mrad of dose cause a disproportionately large amount of damage.

The bias voltages b1 and b3 change by roughly 30 mV over 40 Mrad. Note that the above change of the PMOS threshold does not change the b1 and b3 voltages. (The b1 and b3 nodes are coupled to NMOS transistors, the nodes b2, b4 and b6 to PMOS transistors.) The observed change in b1 and b3 is equivalent to an NMOS transistor threshold shift of roughly 30 mV. (Here the typical NMOS transistor threshold voltages of 420 mV to 460 mV are expected to increase to $\approx$ 450 mV or 490 mV, respectively.)

chip	dose [Mrad]	b1	b2	b3	b4	b5	p6	paset
#4	0	-	-	-	-	-	-	-
#5	0	599	732	742	1,601	1,546	1,921	58
#6	0	605	727	748	1,592	1,536	1,912	58
#4	19	619	662	770	1,548	1,488	1,881	-
#5	19	613	650	763	1,555	1,492	1,884	61
#6	23	620	645	770	1,542	1,479	1,874	61
#4	42	626	615	780	1,521	1,458	1,860	62
simulated	0	612	656	768	1,574	1,493	1,894	57.95

Table 2: Measured and simulated bias voltages in [mV].

The extracted threshold voltage shifts are in good agreements with the results of [6] where a threshold voltage shift of -70 mV after 30 Mrad total dose was observed for PMOS transistors, and a shift of $\approx$ 35 mV was observed for enclosed NMOS transistors after the same dose.

3.2 Signal waveform

In figure 3 a selection of typical signal waveforms is shown for four absorbed doses: 0, 3.5, 10.5, and 20.3 Mrad. The three waveforms are separated by an arbitrary vertical shift. Without the shift they can barely be distinguished by eye.

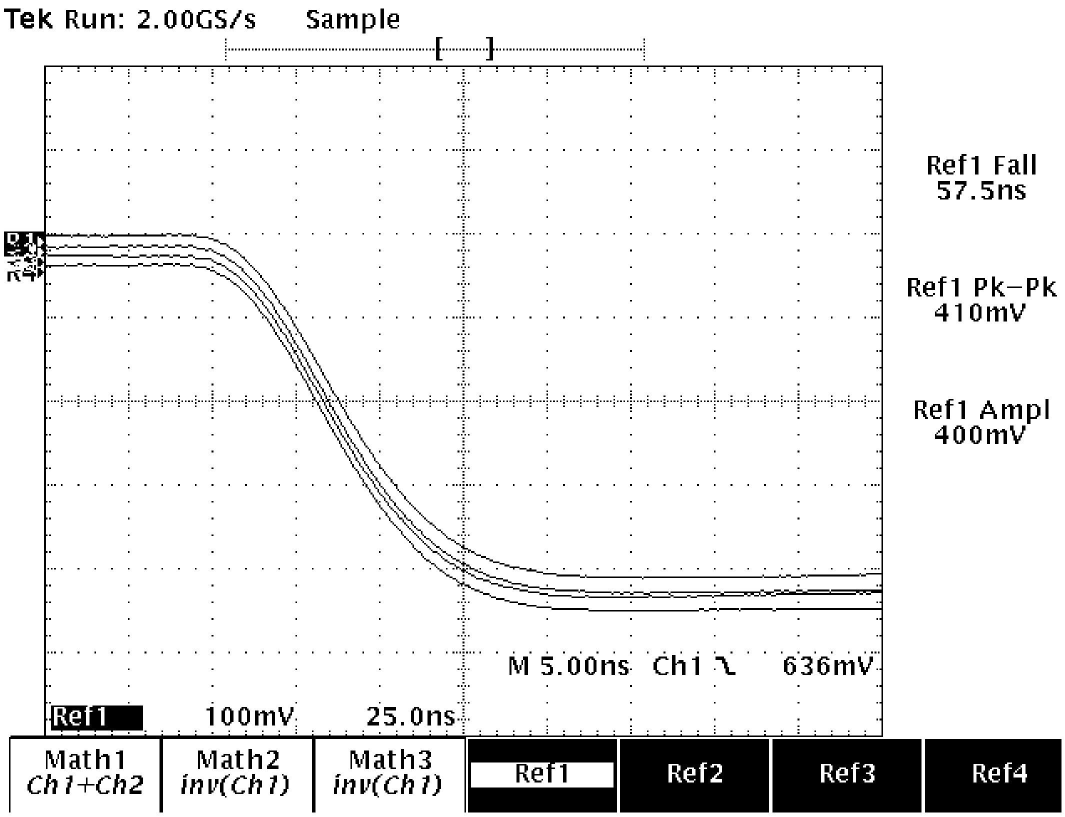

Figure 3: Preamp waveforms of chip #6, ch. 4 after different levels of radiation.

A complete compilation of signal amplitude and rise times for all channels and chips as a function of absorbed dose is given in figures 4 and 5. With the exception of one channel, no significant change in signal amplitude is found. A 10% amplitude increase is observed for channel 11 of chip #4. The reason for this increase is not understood but is likely to be related to the buffer transistor that will not be present on the full SVX4 chip. In any case, the size of the increase is far to small to be of any practical relevance for the use of the preamp in Run 2B. The mildly different amplitudes of different channels are due to the different detector capacitances which lead to different signal waveforms.

In figure 5, no significant change in rise time is observed with the exception of channel 4, chip #6. This channel is the example displayed in figure 3. While the change for this channel may be

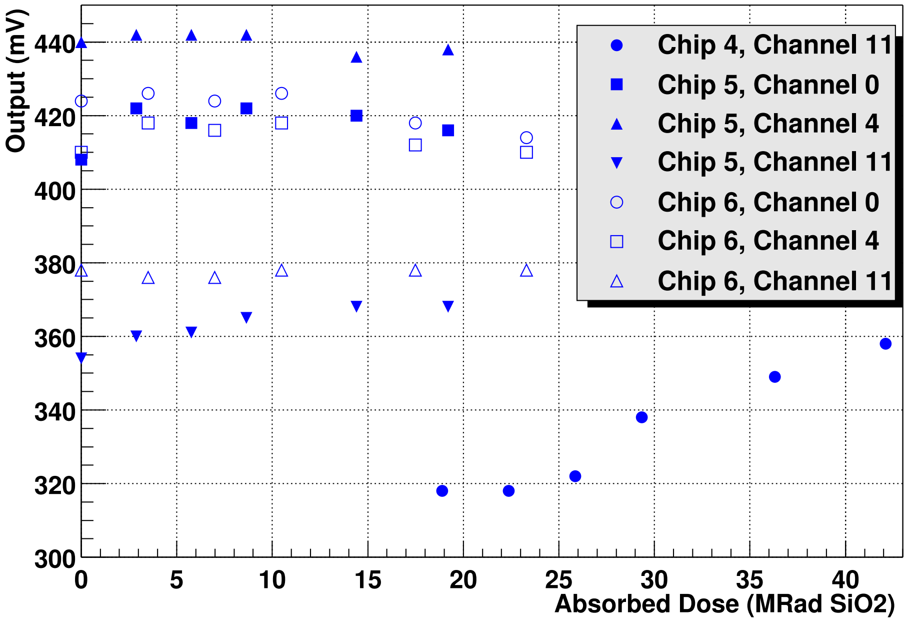

Figure 4: Output signal amplitude as a function of absorbed dose.

significant, it is too small to be a concern. Again, the differences in rise times between different channels are mostly due to the different detector capacitances.

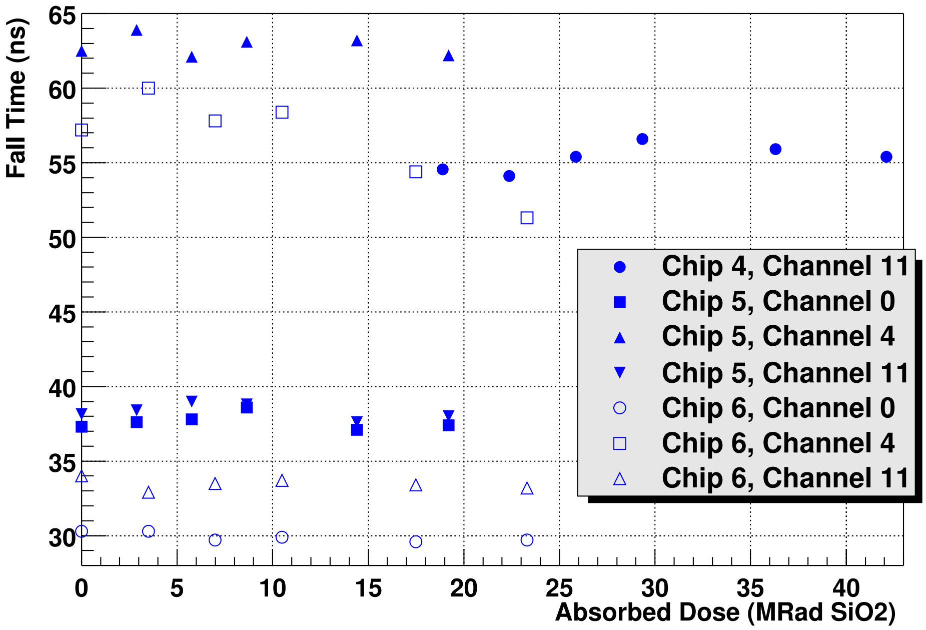

Figure 5: Rise time as a function of absorbed dose.

3.3 Noise measurements

The RMS of the noise signal, amplified by the low noise amplifier CLC425, is measured over a time of order 1000 μs using the RMS function of a digital oscilloscope. The results are shown in figure 6. The upper and lower values for a given channel correspond to the maximum and minimum RMS values observed within typically 1 min.

No significant change in noise level with radiation is observed. The noise values of the different channels with nominally equal capacitances are consistent with each other.

We observe the expected linear rise of the noise level with capacitance. The combined gain of the preamplifier and CLC425 is $\approx$ 28 fC/mV. Thus the noise for 10 pF detector capacitance corresponds to $\approx 890\ e^-$ while that at 56 pF corresponds to ≈ 3350 e$^-$. The latter value exceeds the simulated noise by nearly a factor of 2, suggesting that there may be an added system noise component or a systematic effect in the gain measurement (such effects were looked for and not found). While we do not observe a noise level change, a small increase of noise with radiation cannot be excluded given the considerable systematic uncertainties of the measurements.

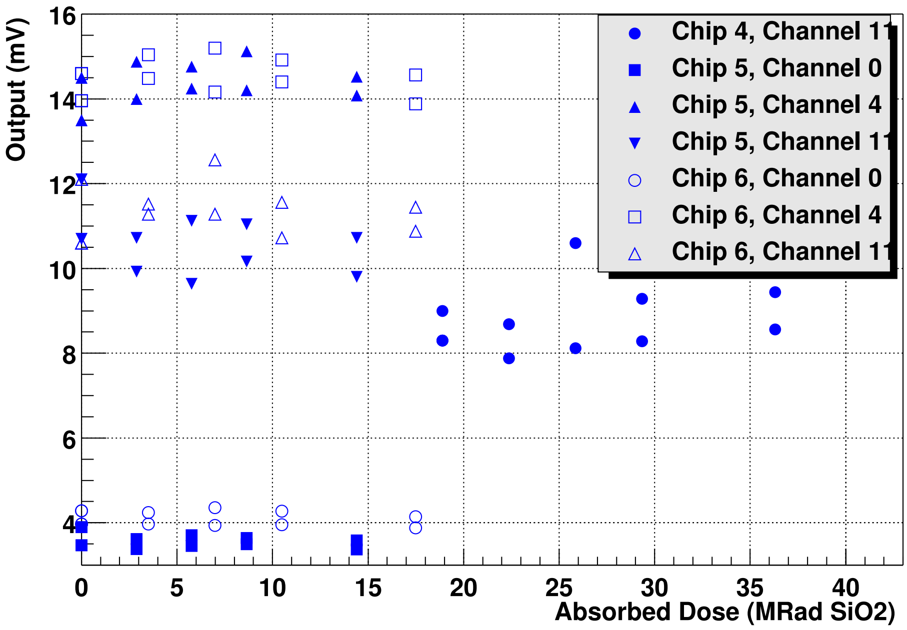

Figure 6: Noise as a function of absorbed dose.

3.4 Summary

An irradiation of several SVX4 preamplifier test chips with ^{60}Co γ radiation of $\approx$ 20 Mrad. A single chip was exposed to a 40 Mrad dose. All chips are fully functional after the irradiation. No significant change of the preamp output signal waveform was observed, while there is a small but significant shift in the preamp bias voltages. The largest shift is -115 mV after 40 Mrad absorbed dose. This is equivalent to a PMOS transistor threshold voltage shift of -80 ± 20 mV.

Acknowledgements

We would like to acknowledge the work of Oren Milgrome (LBNL) and Andrea Neviani (Padova) who designed the preamplifier, and the contribution of Gerit Medeller (LBNL) to the submission of the test chip. Also the help and advice of Jean-Pierre Walder (LBNL) and Brad Krieger (LBNL) during the measurements is highly appreciated.

References

[1] T. Zimmerman *et. al*, NIM **A409** (1998) 369-374.

[2] M. Garcia-Sciveres and M. Weber, CDF/DOC/SEC_VTX/CDFR/5546.

[3] http//www.dmea.osd.mil/testb.html

[4] American Society for Testing and Materials, standard E 1249 - 93, *Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co-60 Sources*.

[5] National Institute of Standards, see eg. http://physics.nist.gov/Divisions/Div846/calguide.html

[6] A. Giraldo, *Evaluation of Deep Submicron Technologies with Radiation Tolerant Layout for Electronics in LHC Environments*, PhD thesis (1998), University of Padova.

node	b1	b2	b3	b4	b5	p6	paset
default	612	656	768	1,574	1,493	1,894	57.95
$15\,°$C	614	682	762	1,573	1,498	1,885	56.60
$25\,°$C	612	656	768	1,574	1,493	1,894	57.95
$35\,°$C	610	630	774	1,576	1,488	1,902	59.29
$45\,°$C	609	604	780	1,577	1,483	1,910	60.64
$\Delta V_{thp} = +0.1$	611	771	766	1,676	1,601	1,995	58.00
$\Delta V_{thp} = +0.07$	611	736	767	1,646	1,567	1,964	57.98
$\Delta V_{thp} = +0.05$	611	713	767	1,625	1,547	1,944	57.97
$\Delta V_{thp} = +0.03$	612	690	768	1,605	1,525	1,924	57.97
$\Delta V_{thp} = 0$	612	656	768	1,574	1,493	1,894	57.95
$\Delta V_{thp} = -0.03$	612	621	769	1,544	1,460	1,863	57.94
$\Delta V_{thp} = -0.05$	613	598	769	1,524	1,438	1,843	57.93
$\Delta V_{thp} = -0.1$	613	540	770	1,472	1,384	1,793	57.91
$\Delta V_{thn} = +0.1$	712	655	870	1,574	1,492	1,894	58.03
$\Delta V_{thn} = 0$	612	656	768	1,574	1,493	1,894	57.95
$\Delta V_{thn} = -0.02$	592	656	748	1,574	1,493	1,894	57.94
$\Delta V_{thn} = -0.1$	512	656	667	1,574	1,493	1,894	57.90

Table 3: Simulated bias voltages in [mV].