Programmable Level-0 Trigger Board and Mean Timer for Experiment 949

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Abstract

Descriptions of the new level-0 (L0) trigger board and the new mean timer (MT) board are provided in this note. In addition, tests of the prototypes (ver.1) of both boards, during the March–April 2001 pulse-on-demand running, are reported.

1 Programmable L0 Trigger Board

The purpose of this board is to replace the 4 Princeton TB2A boards, with one new board. This new board would allow for rapid and simple programming of new triggers.

1.1 Specification for New L0 Trigger Board (ver.1)

The new L0 Trigger Board for E949 was developed at Osaka University and KEK. The board has several Complex Programmable Logic Devices (CPLD) chips, produced by the ALTERA cooperation. Almost any trigger logic can be programmed, using the Hardware Description Langu age (HDL). The specification of the New L0 Trigger Board (ver.1) is as follows:

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- single-width FASTBUS board (no FASTBUS protocol is needed or provided).
- Two MAX7128B devices (ALTERA CPLD) are used for trigger logic (operate with LVTTL signals).
- A FLEX10K100E device (ALTERA CPLD) is used for monitoring the trigger log ic and/or the trigger inputs (operates with LVTTL signals).
- inputs
  - 65 differential ECL inputs from the Trigger-Bus (backplane) to the MAX and FLEX devices.
  - 16 differential ECL inputs from the front panel to the FLEX device.
- outputs
  - 24 differential ECL outputs from each MAX device to the front panel.
  - 16 differential ECL outputs from the FLEX device to the front panel.

Figure 1 is a block diagram of the New L0 Trigger Board (ver.1). Outputs from the MAX device are also fed to the FLEX device.

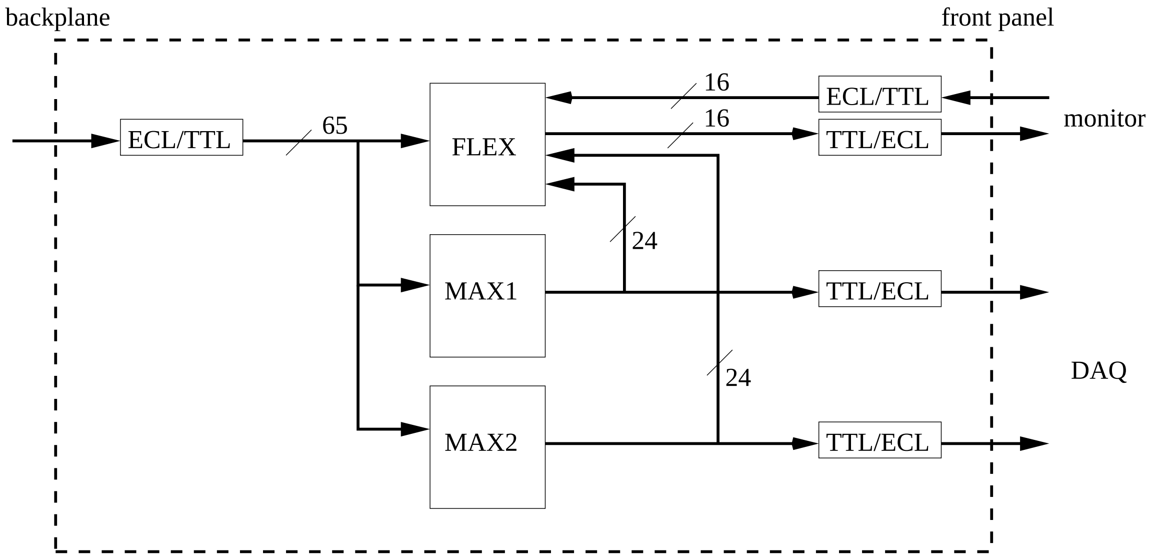

Figure 1: Block diagram of New Level 0 Trigger Board

Any combination of the 65 Trigger bus inputs can be used to form a trigger; the trigger signal will then be output to the prescaler (and on to the rest of the trigger logic) and to a scaler and IO register (for testing). An “OR” output also goes to the RZ board. A summary of the Trigger Bus inputs is provided in Table 1.

pin No.	From	definition	pin No.	From	definition
1	RZ	T+2+3+4+5+6+7+8	34	TT	EC
2	RZ	9	35	TT	(not used)
3	RZ	10	36	TT	E_{tgt}
4	RZ	11	37	TT	#T•2=1
5	RZ	12+13+14	38	TT	#T•2=2
6	RZ	15+16+17+18	39	TT	#T•2=3
7	RZ	19	40	TT	#T•¿3
8	RZ	(not used)	41	TT	C_K
9	RZ	(not used)	42	TT	BV high sum
10	RZ	3_{ct}	43	TT	$N_{TG} > 20$
11	RZ	4_{ct}	44	TT	BV cluster>1
12	RZ	5_{ct}	45	TT	Integrated BV sum
13	RZ	6_{ct}	46	TT	US, DS
14	RZ	7_{ct}	47	TT	(not used)
15	RZ	8_{ct}	48	TT	(not used)
16	RZ	9_{ct}	49	TT	(not used)
17	RZ	10_{ct}	50	TT	(not used)
18	RZ	11_{ct}	51	TT	(not used)
19	RZ	12_{ct}	52	TT	(not used)
20	RZ	13_{ct}	53	TT	reserved for L0 control 1
21	RZ	14_{ct}	54	TT	reserved for L0 control 2
22	RZ	15_{ct}	55	TT	Hex
23	RZ	16_{ct}	56	TT	L0rr1(1)
24	RZ	17_{ct}	57	TT	L0rr1(2)
25	RZ	18_{ct}	58	TT	L0rr1(3)
26	RZ	19_{ct}	59	TT	L0rr1(4)
27	RZ	(not used)	60	TT	L0rr2(1)
28	RZ	(not used)	61	TT	L0rr2(2)
29	TT	K_B(latched)	62	TT	L0rr2(3)
30	TT	π_B	63	TT	L0rr2(4)
31	TT	DC	64	TT	T•2(not latched)
32	TT	IC	65	TT	K_B(not latched)
33	TT	BV			

Table 1: Summary of the Trigger Bus inputs.

1.2 Performance Test

1. During the pulse-on-demand period (Mar.-Apr.,2001), the new L0 Trigger Board (ve r.1) for E949 was plugged into the trigger crate slot #5, replacing the existing Princeton trigger board #5 (containing prompt, CEX board in E787).

2. We examined various trigger signals from the new trigger board with oscilloscope: the trigger signals were about 1nsec later than those from the existing boards used for E787. The version 2 board, which will be ready by the end of June, will save extra $\sim$2nsec by replacing the ECL-LVTTL conversion chips with fas ter ones.

3. The E949 trigger board has powerful diagnostic capabilities: the FLEX chip can be programmed to extract Trigger Bus signals to the front-panel. We have measured the timing of Trigger Bus signals relative to the T•2.

   On the RZ board and the Trigger Transmitter, all Trigger Bus signals (except for unlatched KB and T•2 itself) are latched by the T•2 signal, and there should be no time jitter of any of the latched signals relative to T *bullet*2. However we found 3$\sim$5 nsec of timing jitter. This can be understood as follows: 1) The signals are latched on ECL flip-flop chips on the RZ and TT boards by the T•2 signal. 2) The chip requires a proper setup-time to ensure the operation. The setup-time is the minimum time that is needed before the clock pulse, which must be present at the timing of the input signal. 3) However, the late arrival of any input signal could cause some delay on the output[1]. Delay of several nano-seconds was observed when the signal comes after the setup time.

   Outputs from the new board are fed into the TDC#3 and measured. The data bn-lku7:/e949dsk/towa12/bnlonl/data/km21_mix.41753-41755 taken by the Kmu2(1) trigger in existing trigger board were analyzed. The number of km 21 events which were accepted by the new board is listed in Table 2.

	run41753	run41754	run41755	total
existing board	21831	94403	48859	165093 events
new board	21828	94383	48846	165057 events

   Table 2: Summary of the number of events in the km21 data.

   There is a 0.022% disagreement, which might be caused by the acceptable time of the Trigger Bus signals. We have measured the acceptable time of the new trigger board and found that it was 3.6 nsec. Because T•2 is delayed to latch the results, Trigger Bus signals which come after the T•2 signal can be accepted. The measured acceptable time is enough long to accept almost all of the Trigger Bus signals. The acceptable time of the existing trigger board is longer (3.6$\sim$4.0nsec) than the new trigger board, and may be the cause of the disagreement (see Figure 2). To assure ourselves that this is the correct interpretation we are developing a new Trigger Bus monitor system. A program for monitoring the Trigger Bus signals will be downloaded on the FLEX device and will be read into a VME CPU. This system will read the monit or data and provide Trigger Bus signal time distributions.

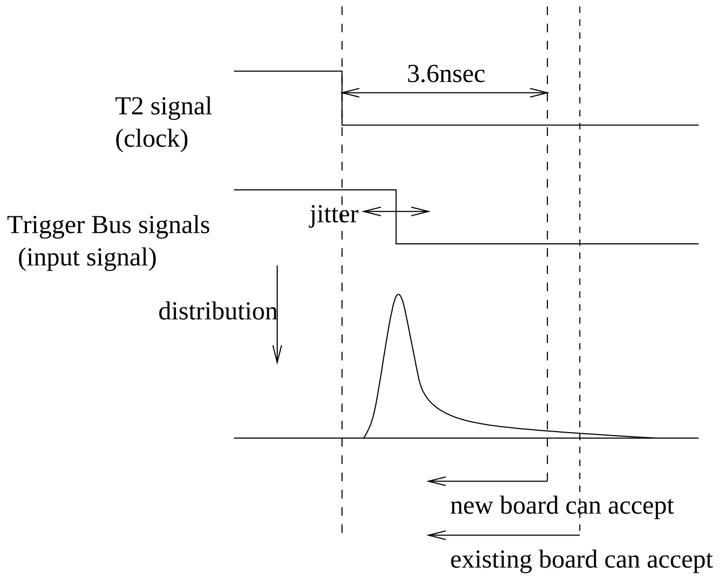

Figure 2: Trigger Bus signals can have timing jitter. The new trigger board can accept Trigger Bus signals up to 3.6 nsec after the T•2.

4. The data taken by the Kbeam trigger in existing trigger board were analyzed. The number of events of various trigger which were reconstructed by tr2bits and accepted by the new board are listed in Table 3.

	tr2bits	e949	fake
minbias	30933	30933	
km21	15282	18254	2972
km22	0	0	
kp21	9828	12850	3023
kp22	6121	6121	
kp23	0	0	
pnn1l0	500	500	
pnn1l0o	7807	7807	
pnn2	593	593	

Table 3: Summary of the number of events in the kbeam data

There is ∼30% disagreement in kmu2(1) and kpi2(1), and not yet understood. Other triggers reconstructed from Kbeam data are OK. Probably related to the fact that ∼75% of kbeam triggers do not have kbeam bit in Trigger Transmitter.

5. New Kmu2(2) trigger was programmed on the new trigger board. The trigger condition for the new Kmu2(2) trigger in E949 is

$$K\mu 2(2) \equiv K_B \cdot T \bullet 2 \cdot DC \cdot (6_{ct} + 7_{ct}) \cdot (20_{ct} + 21_{ct}) \cdot BVL$$

The new trigger board was used to take Kmu2(2) data. We provided the Kmu2(2) trigger signal from the new trigger board to the existin g Kmu2(2) prescaler (PS2-2), and to RZ board for level 0 decision (level 0 decision bit #3). During the run41748-41750,41752,41756, the new Kmu2(2) data was successfully taken by new trigger board.

2 Programmable Mean Timer

The primary purpose of this new Mean Timer (MT) module is to reduce the online E949 deadtime due to accidental photon vetos in the Hextant (RS) and BV and BVL systems. This module provides the combined functions of discriminator and meant imer. In addition, this module will provide a signal from teh L19 counters to veto the $T \bullet 2$ signal for $K_{\mu 2}$ events and improve the L0 deadtime.

2.1 Specification for Programmable Mean Timer module

The Programmable Mean Timer module has a CPLD chip produced by ALTERA. The specification of the Programmable Mean Timer module is as follow:

- single-width CAMAC module.
- A FLEX10K50E device (ALTERA CPLD) is used for mean timer logic.
- 6 mean timer channels per module.
- 12 analog inputs (front panel Lemo connector).
- 16 differential ECL outputs (front panel 34 pin header).

Figure 3 shows the block diagram of the programmable Mean Timer module.

2.2 Performance Test

1. One Programmable Mean Timer module was installed into a CAMAC crate during the pulse-on-demand running period.
2. Time between the mean timed layer 19 (L19) signals and the ORed T•2 out put from the MT2A board was measured. Currently a 12 nsec delay line is programmed on the mean timer module. The latest signals of the mean timed L19 come 16.0∼26.8nsec

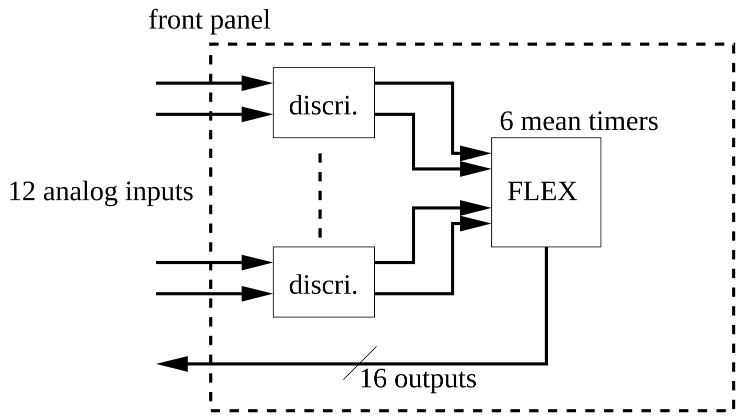

Figure 3: Block diagram of Programmable Mean Timer

before the T•2. We measured the time of the IC to come 23.6∼31.0 nsec before the T•2 output. The RS L19 cables therefore have to be cut out by at least ∼8 nsec. New RS L19 cables (from detector to splitter) are prepared for this purpose. The length of both the new and existing cables was measrued, and it was confirmed the new cables are ∼22 nsec shorter than the existing cables (as expected). At present, we need to cut at least 8 nsec, but a cut of ∼20 nsec is desirable for future logic modifications such as longer delay line.

3. The km21_mix.41754 data was analyzed with the following conditions:

   - Km21 bit,T•2 and charged truck are required.
   - stopping layer should be 19.
   - $60 <$ rd energy < 150.

   Figure 4 shows the timing of L19 HEX1 (MT input #1). The upper left (middle) figure shows the time distribution of the upstream (down stream) signals, and the upper right figure shows their correlation. Lower left (middle) figure shows the time distribution of the online (offline)

   mean timed signals, and the lower right figure shows their correlation. Figure 5 shows the difference of the online and offline mean times.

   In conclusion, we confirmed that the Mean Timer module works well as expected. The Mean Timer module improves the resolution of layer 19 signal timing; the RMS of the online mean times is 1.31nsec, compared to the RMS of the upstream-end signals (2.25nsec) and that of the downstream-end signals (2.31 nsec). At KEK, we have measured the RMS of the difference of the online and offline mean times, using a test pulse, to be 0.3 nsec (with a TDC whose least count is 25psec). In the pulse-on-demand beam test we observed a 0.623 nsec RMS for this distribution, due to the 1nsec TDC#3 least count.

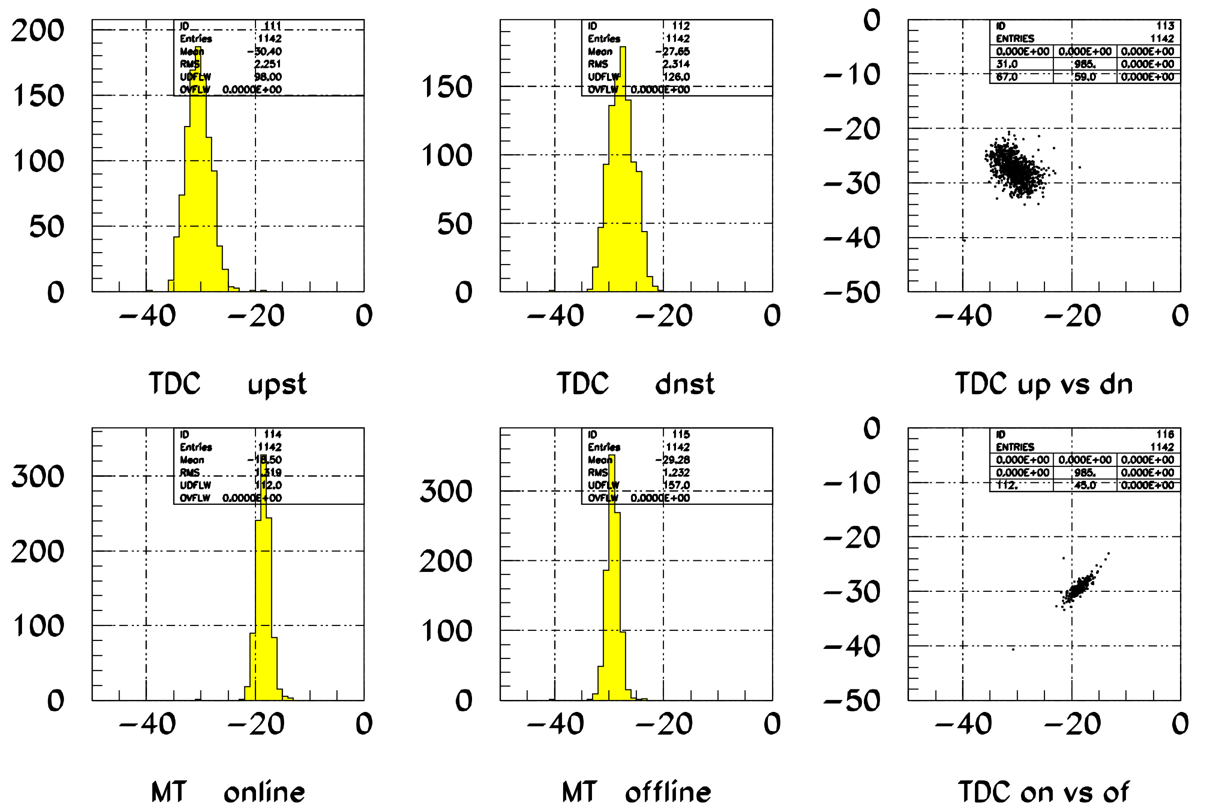

Figure 4: (Upper plots) Distribution of the upstream signal, downstream signal, and scatter plot, and (lower plots) online mean time, offline mean time, and scatter plot.

References

[1] ON Semiconductor, Metastability and the ECLinPS Family(AN1504/D),available from http://www.onsemi.com/pub/Collateral/AN1504-D.PDF.

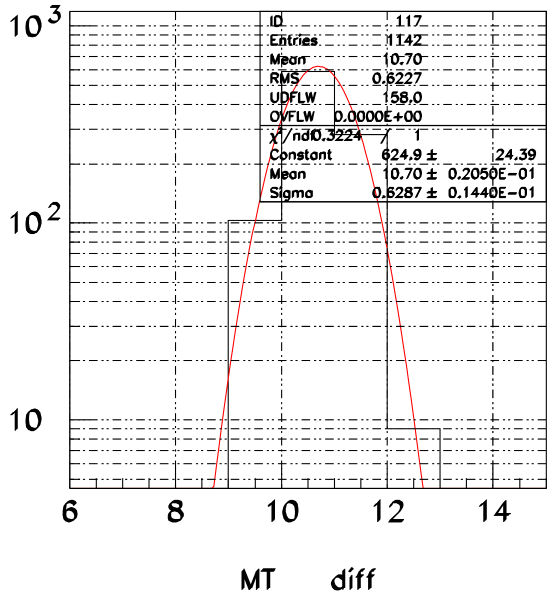

Figure 5: Difference of the online and offline mean times