July 13, 2000

Time-of-Flight Electronics

Matthew Jones

University of Pennsylvania

- Overview of signal path
- Analog signal processing
- Transition board
- deCAF card

Overview

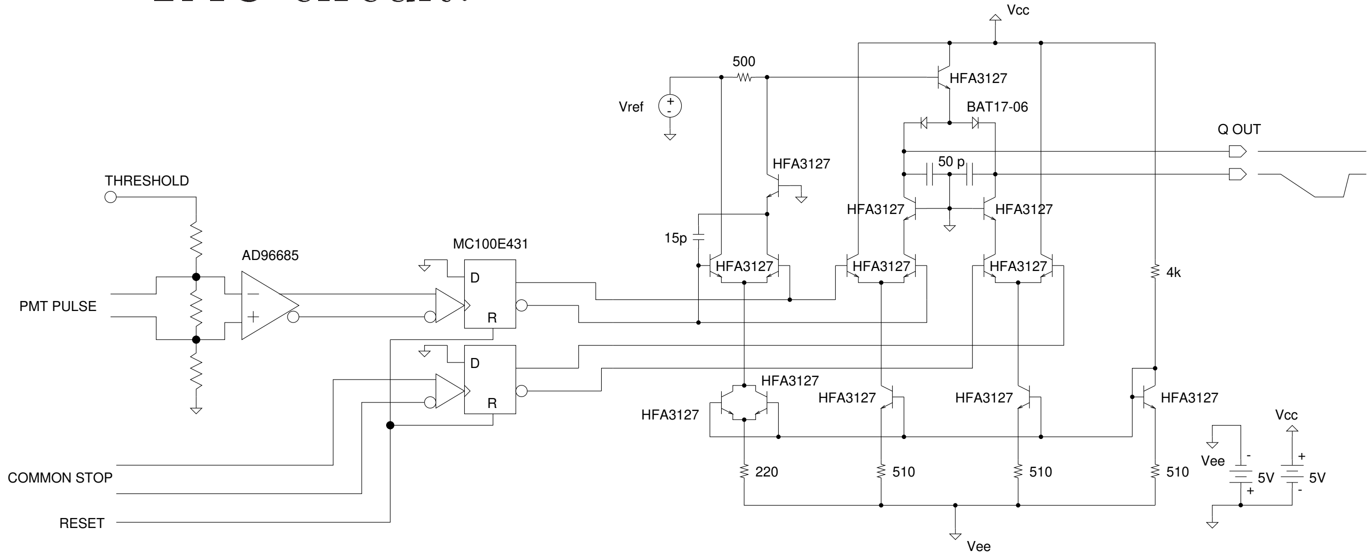
- Measure *time* and *charge* on 432 channels
- Use ADMEM to interface with datastream
  - One ADMEM reads out 9 PMT channels
  - Measure charge using CAFE cards (even channels)
  - Measure time using 12 bit ADC (odd channels)
- Signal path (analog daughter board):
  - Terminate signal cable
  - Pulse shaping, baseline restoration
  - Split between time and charge circuits
  - Time: Discriminator + TAC (common stop)
  - Charge: Gated current source onto CAFE
- Main transition board provides support services

Analog circuits

- Cable:
  - 3 shielded twisted pairs in overall jacket
  - Female DB-9 connector
- Receiver:
  - Prototyped:
    - Multi-stage transistor amplifier (gain=2)
    - Video op-amp (gain=2)
  - Proposed:
    - Transformer?
    - Emitter followers?
- Shaper
  - Condition signal for input to BLR
- Baseline Restorer
  - Diode bridge current switch?
  - Clamp gated with reset signal?

Analog circuits

- Discriminator
  - AD96685 with feedback
  - Threshold set by DAC on transition board
- TAC circuit:



  - Measure voltage with instrumentation amplifier
  - Drive voltage onto ADMEM board via P3 connector to deCAF card

Analog circuits

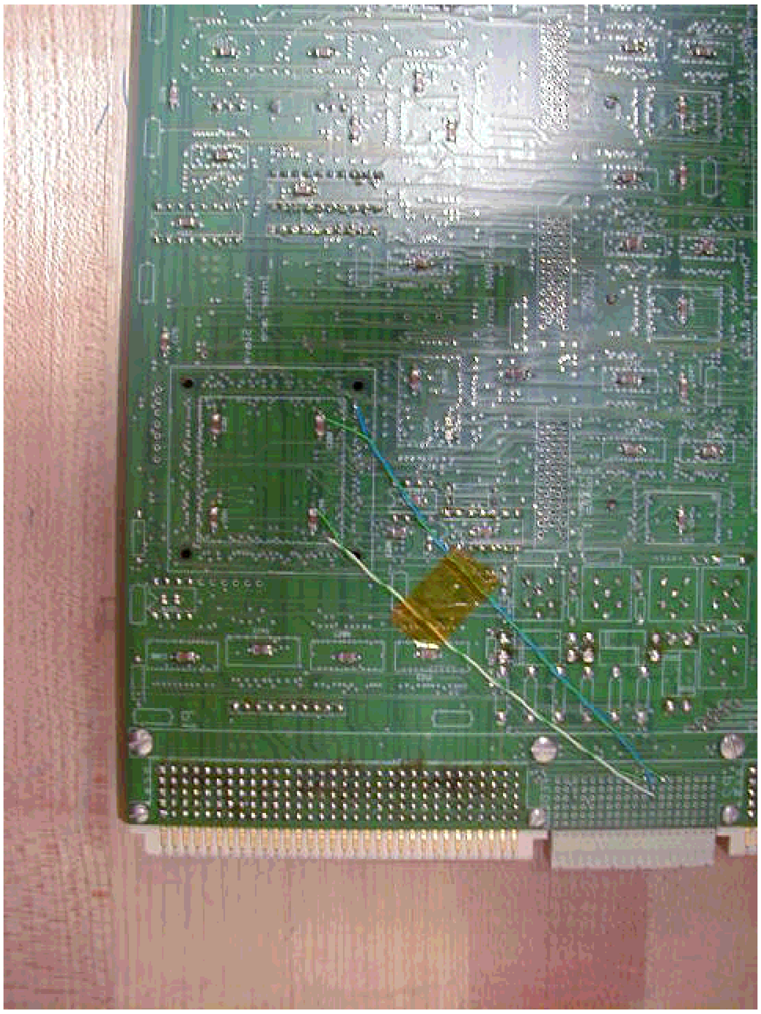
- Gated current source
  - Drive current proportional to pulse height onto CAFE card
  - Generate gate from discriminator output
    - Bipolar current switch?
    - FET switch?
- Calibration circuits
  - Differential ECL calibration signal fanned out with common stop
  - Charge injection into receiver for TAC and CAFE calibration
  - Fire discriminator with no input pulse for measuring pedestals

Transition Board

- Services provided:
  - DAC's (*e.g.* discriminator thresholds)
  - ADC's (DAC readback and remote monitoring)
  - Digital control voltages (channel inhibit, enable calibration,...)
  - Communication with crate clock fanout
  - Remote monitoring of clock and analog signals

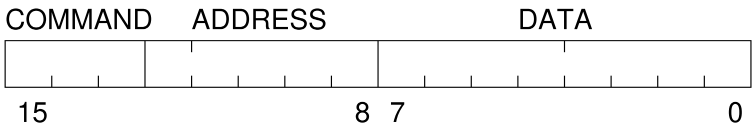
Transition Board

- Digital Interface
  - 16 bit bus via P0 connector
  - TRANS_PORT_RD and $\overline{\text{TRANS\_PORT\_WR}}$ brought out to P0(d12) and P0(e12) via wire mods:



Transition Board

- Digital Interface
  - Digital services in XC5200 series Xilinx
  - Programmed in “Express” mode via P0 bus.
  - Program size: 5302 bytes
  - Eventually switch to PROM or flash RAM?
- Command structure:



COMMAND:
<001> WRITE REGISTER
<010> READ REGISTER
<011> PROGRAM DAC
<100> CONVERT ADC
<111> PROGRAM XILINX

REGISTERS:

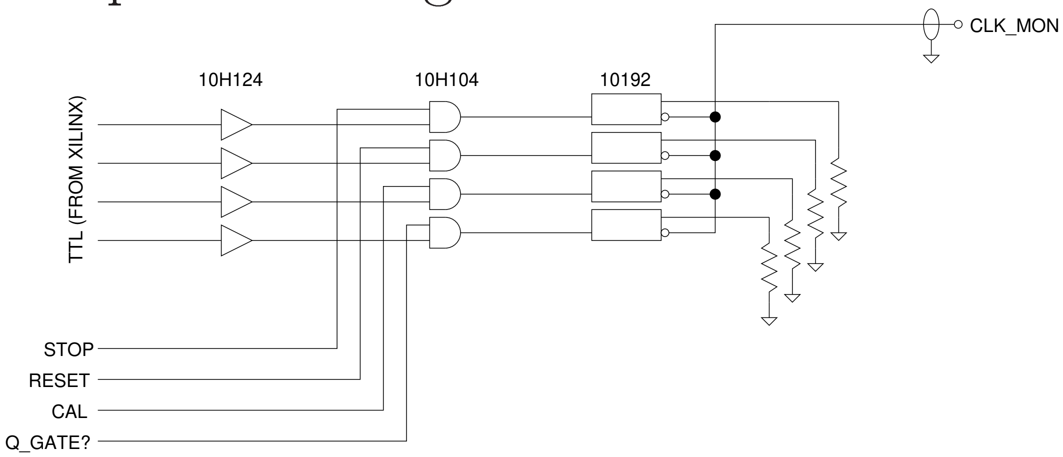
0	(RW)	DIAGNOSTIC REGISTER
1	(R)	TRANSITION BOARD SERIAL NUMBER
2	(R)	TRANSITION BOARD STATUS
3		<RESERVED>
4 ,5	(RW)	CHAN0..2 CONTROL (LOW, HIGH)
6,7	(RW)	CHAN3..5 CONTROL (LOW, HIGH)
8,9	(RW)	CHAN6..9 CONTROL (LOW, HIGH)
10	(RW)	TRANSITION BOARD CONTROL
11		<RESERVED>
12,13	(RW)	DAC SHIFT REGISTER (LOW, HIGH)
14,15	(R)	ADC SHIFT REGISTER (LOW, HIGH)
16-27		<UNUSED>
28	(RW)	AUX PORT 0 (RESET LEADING EDGE DELAY)
29	(RW)	AUX PORT 1 (RESET TRAILING EDGE DELAY)
30	(RW)	AUX PORT 2 <RESERVED>
31	(RW)	AUX PORT 3 <RESERVED>

Transition Board

- DAC's
  - Maxim MAX528 - 8 bit octal DAC
  - Serial programmable with 3 wires ($\overline{\text{CS}}$, DIN, CLK)
  - Programmed via shift register in Xilinx
  - Minimal number required: ~ 3.
  - Lots of spare voltages provided by 7.
  - Useful voltage ranges not clear yet
- ADC's
  - Maxim MAX1202 - 12 bit octal ADC (4.096 volt internal reference)
  - Serial programmable with 4 wires ($\overline{\text{CS}}$, DIN, DOUT, CLK)
  - Programming and readback via shift registers in Xilinx
  - Use n per board?

Monitoring

- Two RG-58 cables per transition board go to a patch panel in the counting room
- Monitor clock signals (particularly reset) and PMT pulses remotely
- Allow rapid commissioning (phasing of clocks) and problem diagnosis



- We would like a similar current sum for pulses out of BLR.
- Easily implemented with ADC's:
  - Temperature monitoring
  - Pulse rate (luminosity)
  - Voltages at sensitive nodes

DeCAF Card

- Motivation: 50 ns dynamic range, < 25 ps least count. Requires ≥ 11 bits.
- Replace 10-bit ADC with 12-bit ADC (*eg.* AD9225)
- Significant simplification of CAFE card:
  - no QIE chip
  - no current calibrator
  - no flash RAM
- Drive ADC with voltage from TAC on transition board
  - Single-ended signal - must use ground as reference
  - This may not work... build one and see.
  - Alternatively, drive a current onto deCAF card.

Conclusions

- Fairly mature overall design
- Almost all major features of main transition board prototyped (ADC interface remains)
- Could *start* laying out main transition board any time
- Unwise to submit a board before prototyping of analog circuits
- Next steps:
  - Prototype receiver, shaper, BLR
  - Rebuild discriminator, TAC
  - Hack a blank deCAF card
  - Measure widths of ADC distributions
  - If okay, lay out analog daughter-board and deCAF