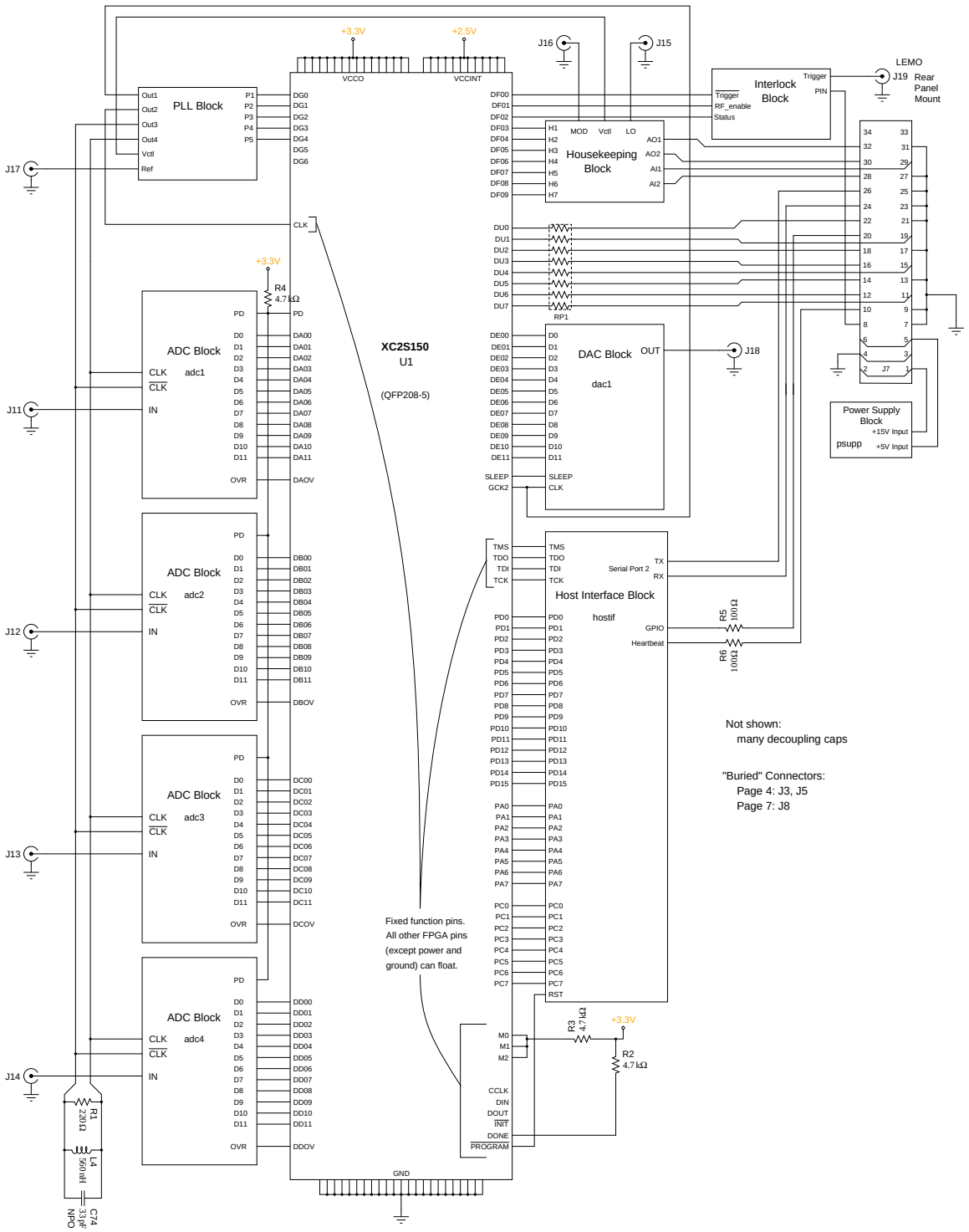
SNS MEBT LLRF Digital board V2

Top Level Schematic

SNS MEBT LLRF Digital Board V2 — Page 1/8
Larry Doolittle, LBNL — 9pm 10/08/02



ADC Block

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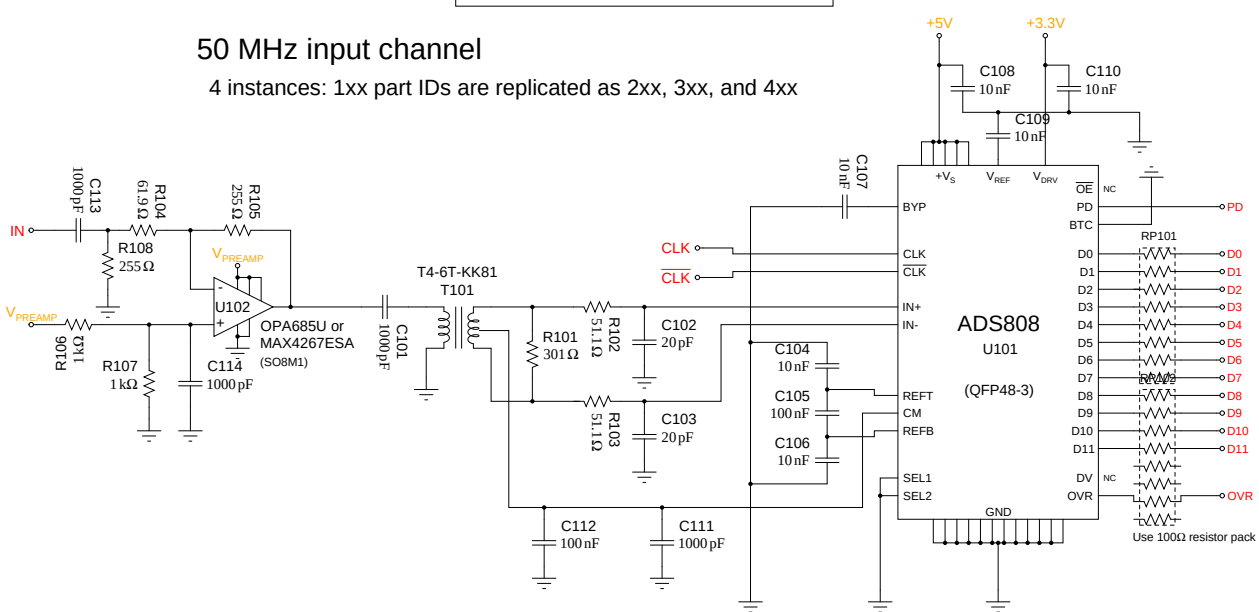
50 MHz input channel

4 instances: 1xx part IDs are replicated as 2xx, 3xx, and 4xx



50 MHz output channel

DAC Block

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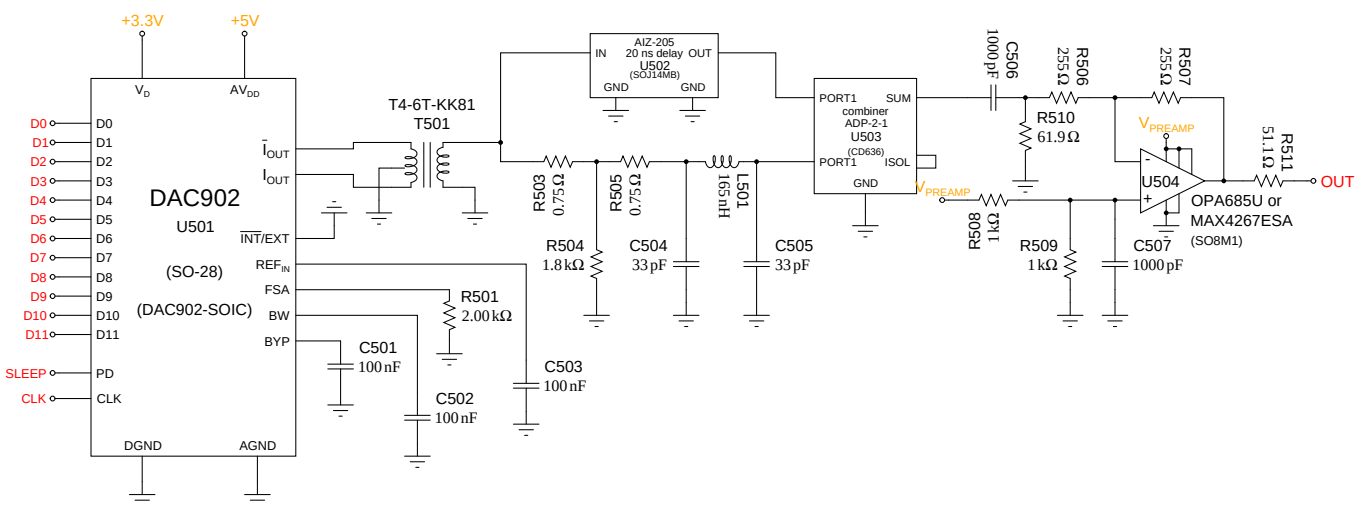

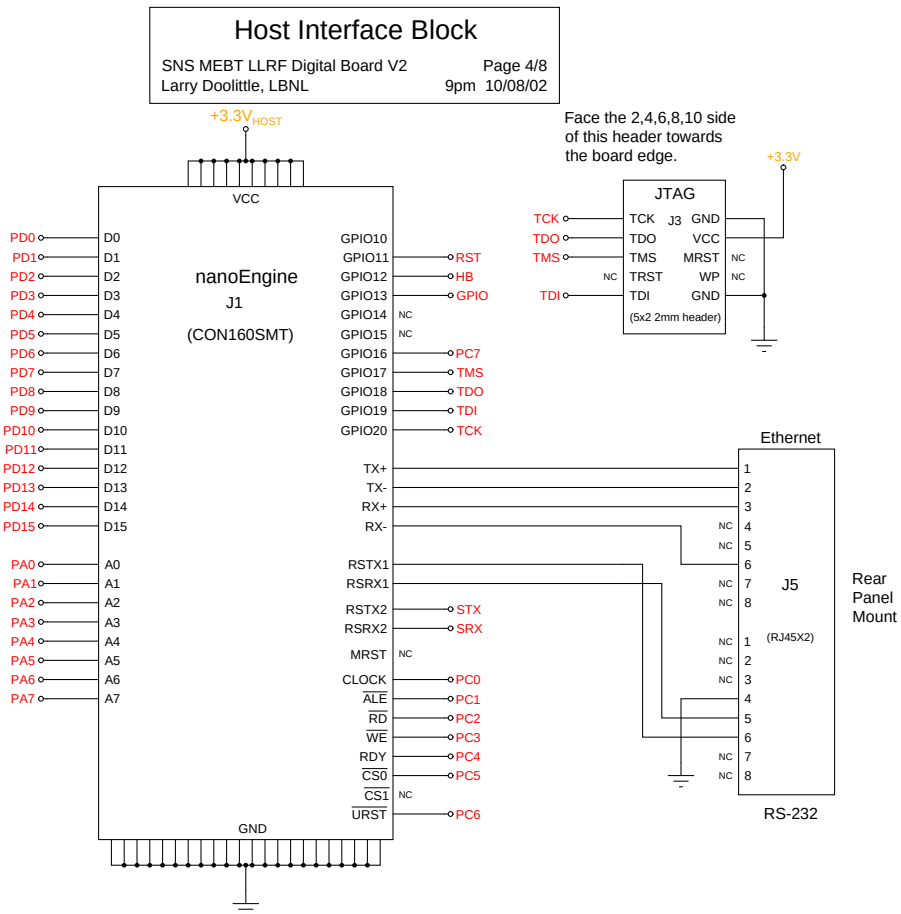
Host Interface Block
SNS MEBT LLRF Digital Board V2
Larry Doolittle, LBNL
Page 4/8
9pm 10/08/02
+3.3V HOST
VCC
nanoEngine
J1
(CON160SMT)
GND
PD0 D0
PD1 D1
PD2 D2
PD3 D3
PD4 D4
PD5 D5
PD6 D6
PD7 D7
PD8 D8
PD9 D9
PD10 D10
PD11 D11
PD12 D12
PD13 D13
PD14 D14
PD15 D15
PA0 A0
PA1 A1
PA2 A2
PA3 A3
PA4 A4
PA5 A5
PA6 A6
PA7 A7
GPIO10
GPIO11 RST
GPIO12 HB
GPIO13 GPIO
GPIO14 NC
GPIO15 NC
GPIO16 PC7
GPIO17 TMS
GPIO18 TDO
GPIO19 TDI
GPIO20 TCK
TX+
TX-
RX+
RX-
RSTX1
RSRX1
RSTX2 STX
RSRX2 SRX
MRST NC
CLOCK PC0
ALE PC1
RD PC2
WE PC3
RDY PC4
CS0 PC5
CS1 NC
URST PC6
Face the 2,4,6,8,10 side of this header towards the board edge.
+3.3V
JTAG
J3
TCK TCK GND
TDO TDO VCC
TMS TMS MRST NC
NC TRST WP NC
TDI TDI GND
(5x2 2mm header)
Ethernet
J5
(RJ45X2)
Rear Panel Mount
RS-232

Power Supply Block

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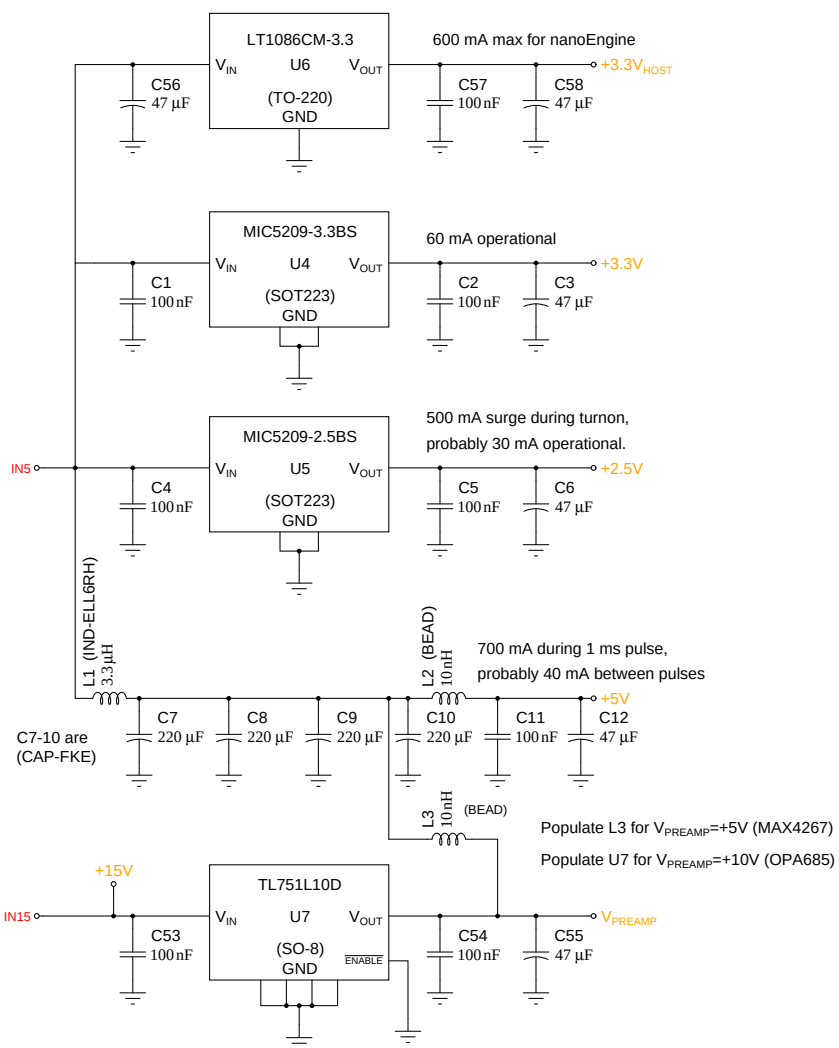

PLL Block

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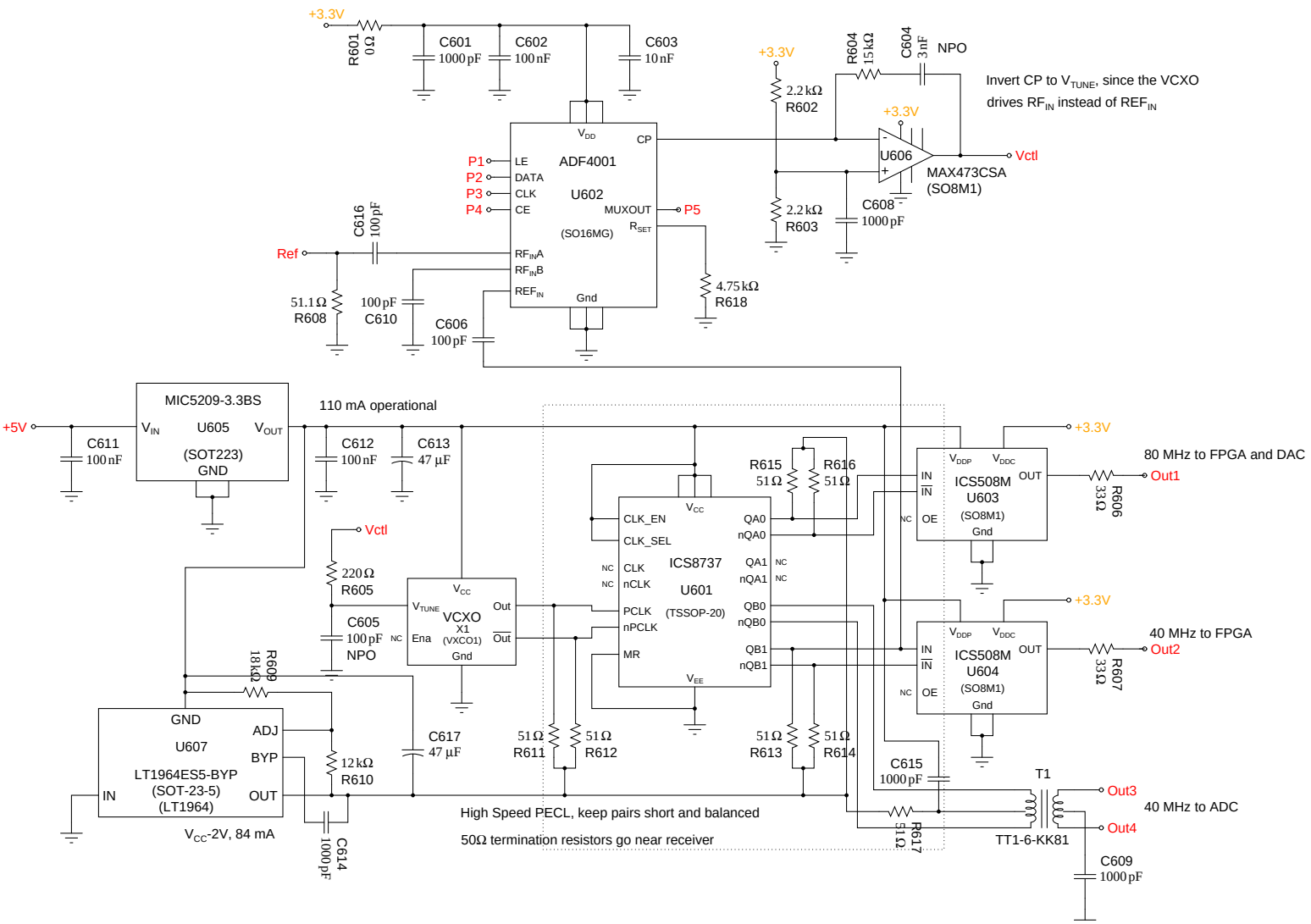
Phase Locked Loop



Interlock Block

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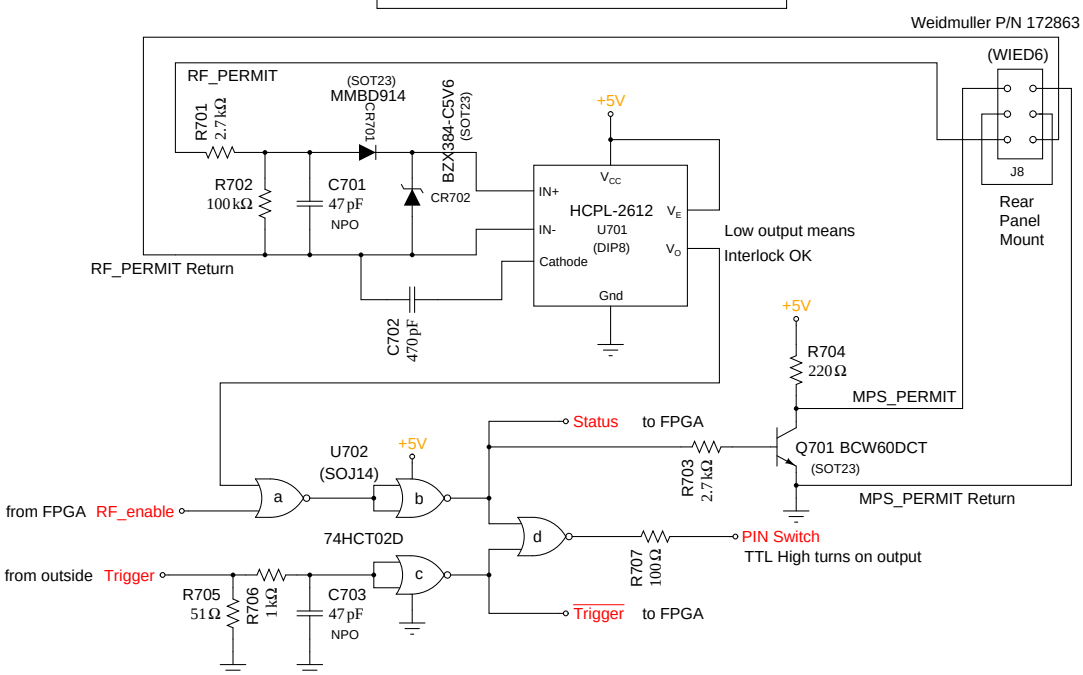

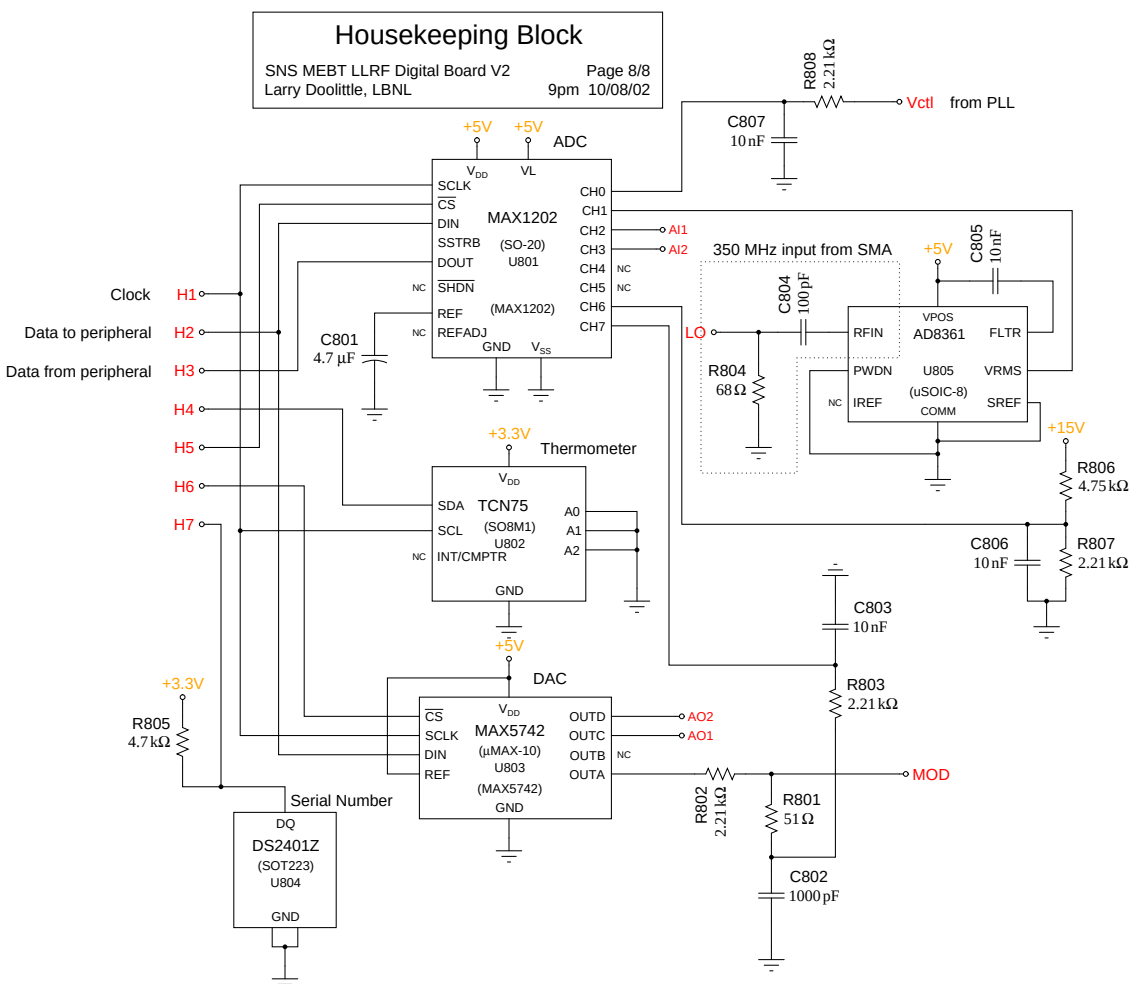
Housekeeping Block
SNS MEBT LLRF Digital Board V2
Page 8/8
Larry Doolittle, LBNL
9pm 10/08/02
R808
2.21 kΩ
Vctl
from PLL
C807
10 nF
+5V
+5V
ADC
MAX1202
(SO-20)
U801
(MAX1202)
SCLK
CS
DIN
SSTRB
DOUT
SHDN
REF
REFADJ
GND
VDD
VL
VSS
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
NC
AI1
AI2
Clock
H1
Data to peripheral
H2
Data from peripheral
H3
H4
H5
H6
H7
C801
4.7 µF
350 MHz input from SMA
+5V
C805
10 nF
C804
100 pF
LO
R804
68 Ω
VPOS
AD8361
U805
(uSOIC-8)
RFIN
PWDN
IREF
COMM
FLTR
VRMS
SREF
+15V
R806
4.75 kΩ
C806
10 nF
R807
2.21 kΩ
+3.3V
Thermometer
TCN75
(SO8M1)
U802
SDA
SCL
INT/CMPTR
GND
A0
A1
A2
C803
10 nF
+5V
DAC
MAX5742
(µMAX-10)
U803
(MAX5742)
CS
SCLK
DIN
REF
GND
OUTD
OUTC
OUTB
OUTA
AO2
AO1
R803
2.21 kΩ
+3.3V
R805
4.7 kΩ
R802
2.21 kΩ
R801
51 Ω
MOD
Serial Number
DQ
DS2401Z
(SOT223)
U804
GND
C802
1000 pF