Characterisation of Hybrid Pixel Detectors with capacitive charge division

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Abstract. In order to fully exploit the physics potential of the future high energy e^+e^- linear collider, a Vertex Tracker providing high resolution track reconstruction is required. Hybrid pixel sensors are an attractive technology due to their fast read-out capabilities and radiation hardness. A novel pixel detector layout with interleaved cells between the readout nodes has been developed to improve the single point resolution. The results of the characterisation of the first processed prototypes are reported.

INTRODUCTION

The physics programme at future high energy linear colliders, designed to deliver e^+e^- collisions at centre-of mass energies $\sqrt{s}$ = 0.3 - 3 TeV with luminosities in excess to 10^{34} cm^{-2} s^{-1}, largely relies on the ability to identify in a high track density environment the flavour of final state fermions with high efficiency and purity [1]. The target impact parameter resolution may be parametrised as $5\ \mu\mathrm{m} \oplus \frac{15\ \mu m}{p_t\ (GeV/c) sin^{1/2}(\theta)}$ and it requires single point resolution at the $5-7\ \mu m$ level and a material budget below $0.5\% X_o$ for each layer. This paper summarises the recent results on the development of a novel hybrid pixel sensor design, tailored to meet the Linear Collider specifications.

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HYBRID PIXEL SENSOR DESIGN

The main limitation of the existing pixel detectors is the achievable single point resolution. A resolution below 10 μm can be obtained by sampling the diffusion of the carriers generated along the particle path and adopting an analog read-out to interpolate the signals of neighbouring cells. Since the charge diffusion r.m.s. in 300 μm thick silicon is $\simeq$ 8 μm, its efficient sampling requires a pixel pitch below 50 μm. As the most advanced read-out electronics have a cell dimension of 50 $\times$ 300 μm^2, this is limiting the pixel pitch, hence of the resolution. Future developments in deep sub-micron VLSI electronics may help overcoming this limit. However, it is interesting to independently explore a sensor design reducing the current constraints.

The proposed pixel detector design exploits a layout, already successfully adopted in Silicon microstrip detectors, where only one-out-of-n implants is read-out. In such a configuration, charge carriers generated underneath one of the interleaved pixel cells induce a signal on the capacitively coupled read-out pixels, leading to a spatial accuracy improvement by a proper signal interpolation. Sampling of the charge carrier distribution is achieved by the fine implant pitch and the analog cell size has to fit the wider read-out pitch. The maximum number of interleaved pixels is constrained by the charge collection mechanism and the two track separation.

Prototypes of detectors with interleaved pixels have been designed and manufactured. Thirty-six test structures have been fit on a 4$''$ wafer, consisting of detectors with 0 to 3 interleaved pixels defining a VLSI cell size of either 200 $\times$ 200 μm^2 or 300 $\times$ 300 μm^2. Details of the layout, the technology and the results of the basic electrostatic tests may be found elsewhere [2]- [3].

DETECTOR MODELLING

In a simplified model, the detector may be reduced to a capacitive network. Each pixel is a node characterised by the backplane capacitance (C_{bkpl}) and the inter-pixel capacitances (C_{ip}), dominated by the couplings to the nearest and diagonal neighbours. The C_{ip}/C_{bkpl} ratio is crucial in the detector design, as it defines the signal amplitude reduction (an effective charge loss) at the output nodes.

The capacitances of the produced prototypes were measured and the procedure reported in [4]; the results are summarised in Table 1, where a comparison with a numerical estimate is also shown.

The capacitances were calculated solving the Laplace equation inside a 5x5 pixel matrix with a finite element analysis performed using the OPERA-3D package [5]. The comparison with the calculated values is fair for all of the structures but chip 4, where difficulties in the simulation were expected because of the small pitch. In particular, the maximum number of elements in OPERA-3D was preventing an optimal interpixel mesh and the extension to a larger pixel matrix, crucial for a proper interpixel capacitance evaluation for pixels with 50μm pitch in a 350μm thick de-

TABLE 1. *Interpixel (C_{ip}) and backplane (C_{bkpl}) capacitance values for different detector structures.*

	chip 1	chip 2	chip 3	chip 4
Implant width [μm]	100	60	50	34
Implant pitch [μm]	150	100	75	50
Readout pitch [μm]	300	200	300	200
No. of pixels in parallel	64	128	126	254
Measured C_{ip} $[fF]$	599$\pm$5	1038$\pm$11	958$\pm$5	2098$\pm$30
Calculated C_{ip} $[fF]$	630$\pm$60	880$\pm$67	690$\pm$70	980$\pm$40
Measured C_{bkpl} $[fF]$	447$\pm$5	368$\pm$5	218$\pm$5	185$\pm$5
Calculated C_{bkpl} $[fF]$	470$\pm$70	410$\pm$90	230$\pm$35	211$\pm$60
Total C_{ip} $[fF]$	26.2$\pm$4.0	13.4$\pm$0.9	13.8$\pm$2.0	9.6$\pm$1.0
$C_{nearest\ neighbour}$ $[fF]$	4.4$\pm$0.7	2.0$\pm$0.1	2.1$\pm$0.3	1.5$\pm$0.2
C_{bkpl} $[fF]$	7.3$\pm$1.1	3.2$\pm$0.7	1.9$\pm$0.7	0.8$\pm$0.2
Max. charge loss	35%	32%	77%	67%

tector. The numerical estimate is essential to break down the measurements in the single inter-pixel contributions, used to specify the capacitive network. The calculated single pixel main capacitances are also summarised in Table 1, together with the maximum charge loss estimated by a network analysis with a dedicated software based on the node potential method. The role of C_{ip} may be stressed referring to chip 4, where the maximum charge loss is reduced to 51% if the measured interpixel capacitances are assumed.

CHARGE COLLECTION STUDIES

The achievable resolution is proportional to the pixel pitch and the Noise over Signal ratio (N/S). If the implant pitch is comparable to the diffusion width, the collected charge at the output nodes will have both the contributions by the direct diffusion and the linear share by the capacitive coupling. In such a case, an improvement beyond the binary value given by the *implant pitch*$/\sqrt{12}$ may be expected. The N/S in pixel detectors can easily exceeds 1/100, due to the small detector capacitance. Because of this, an effective signal interpolation may be expected even with $\simeq$ 50% signal reduction.

The charge collection properties and the achievable resolution have been directly studied by shining an infrared diode spot on the backplane of a structure with 60 μm implant width, 100 μm implant pitch and 200 μm read-out pitch. At the diode wavelength of λ = 880 nm, the penetration depth in the silicon substrate corresponds to 10 μm. The IR light has been focused to a spot size of $\simeq$ 80 μm and its position in the detector plane controlled by a 2-D stage allowing to scan the pixel array with micro-metric accuracy. A sketch of the tested structure and the scan direction is displayed in Fig. 1

A matrix of 4 $\times$ 7 read-out pixels has been wire-bonded to a VA-1 chip [6]. For each spot position, 1000 events have been recorded. The common mode, pedestal and noise calculation has been initialised for the first 300 events. In the subsequent events light was injected every 10 events, allowing for continuous pedestal tracking. Because of the limited data volume, no on-line suppression has been applied and the data reduction and cluster search has been performed off-line. Results have been averaged over the 70 recorded light pulses, with a peak pulse height corresponding to N/S $\simeq$ 1/100 and a maximum charge loss of $\simeq$ 40%, in agreement with the network analysis. The charge sharing may be characterised by the η function, defined as $\eta = \frac{PH_i}{PH_{cluster}}$, where PH_i is the pulse height on the reference pixel i, normalised to the cluster pulse height. The η function by construction ranges in the [0;1] interval and it has a period equals to the readout pitch. The measured distribution is shown in Fig.2a, where the reference pixel for the first period has a centre at x = 100 μm. For the structure under test, the ratio between the spot size and the pitch $\simeq$ 0.8 and the experimental η curve can be understood as a superposition of the effects due to the diffusion of the charge carriers created by the IR spot on the neighbouring junctions and by the capacitive charge sharing. The η parametrisation allows a coordinate reconstruction on an event by event basis and the measurement of the resolution, obtained comparing the laser spot position by the micrometric stage to the reconstructed values. The results are shown in Fig. 2a and 2b. In the interleaved pixels, where the charge sharing is most efficient, the resolution approaches $\simeq$ 3 μm, irrespective of the $\simeq$ 40% charge loss. On the other hand, when the charge sharing is minimal the resolution degrades to $\simeq$ 10 μm, even with a peak pulse height. According to these results, the binary resolution defined by the *implant pitch*$/\sqrt{12}$ can be improved by about a factor 4 for a configuration where the ratio between the charge carrier cloud r.m.s. and the pixel pitch $\simeq$ 0.8.

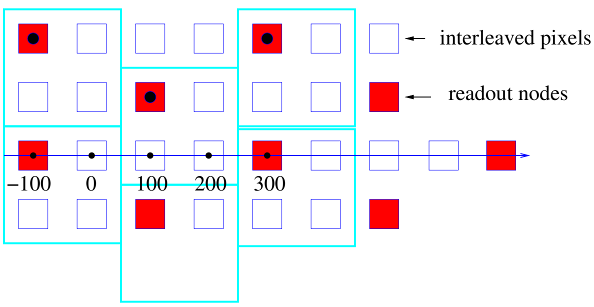

FIGURE 1. *A sketch of the tested structure, with 100 μm implant pitch and 200 μm read-out pitch. The horizontal line identifies the scan direction and defines the coordinate system. The frames define the footprint of an hypothetical VLSI cell.*

A similar scaling factor can be expected for a minimum ionising particle detected by a pixel sensor with $20-25\mu m$ pitch, as long as the peak $N/S \leq 1/100$ and the charge loss is $\leq 50\%$. This would lead to intrinsic resolutions $\simeq 2\mu m$, well within the specifications for an experiment at the future linear collider.

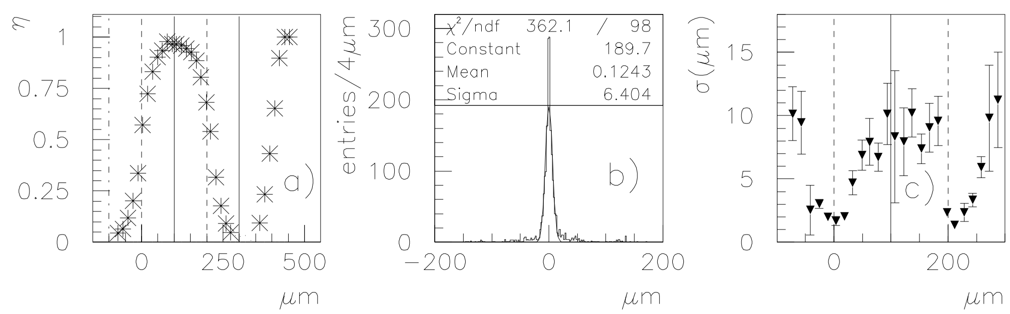

FIGURE 2. *The charge sharing among neighbouring read-out pixels, measured by* $\eta = \frac{PH_i}{PH_{tot}}$ *during the detector scan (a). The average resolution and the achieved resolution vs. the spot position are shown in b) and c). The vertical lines identify the centre of the pixels; the full line identify the reference pixel for the* η *calculation*

CONCLUSIONS

Prototype pixel detectors with interleaved pixel cells, aimed at improving their single point resolution to match the requirements for applications at the future linear collider, have been designed and manufactured. The results of their electrostatic characterisation and the preliminary charge collection studies have confirmed the validity of this detector concept. A second prototype production with $20-25\mu m$ pixel pitch is planned on a short time scale.

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