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SVX4 Test Chip User's Guide

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1 Introduction

This note contains basic information concerning the first test chip submission for the SVX4 chip. The SVX4 chip is currently being developed by FNAL, LBNL and Padova. It corresponds essentially to the transformation of the SVX3 chip to the TSMC 0.25μm process. The chips produced with this technology will be capable to withstand the radiation dose accumulated in Run IIb of the Tevatron collider. They will be used to equip the upgraded silicon detectors of CDF and D0.

The submission will yield 25 test chips. Each test chip consists of a 12-channel preamplifier, the preamplifier bias circuit and an isolated CMOS receiver.

2 Pad assignment and dimensions

The lateral chip dimensions are $2854 \times 2523\,\mu\text{m}^2$ (plus cutting tolerances of $\approx$ 200 μm). The chip thickness is $\approx$ 700 μm. The bonding pad assignment and location is shown in Figure 1. The description of the pads is given below:

1. **IN 0 - IN 11**: Twelve preamplifier input channels
2. **Out 0 - Out 11**: The corresponding preamplifier output channels
Note that these outputs are only designed to drive the input of the pipeline which is a ≈ 1.2 pF load.
3. **Outbuf 0 - Outbuf 11**: Buffered preamplifier output signal (needs external resistors, see section 5)
4. **VDDA**: Analog supply voltage of AVDD = 2.5 V
5. **GND**: Analog ground
6. **BGND**: Ground of output buffer. Can be used to measure substrate contact resistance.
7. **BW0 - BW1**: CMOS switches to select four values of bandwidth (preamplifier rise time). Setting BW1 (BW0) to AVDD, connects a capacitance of $\approx$ 200 fF (100 fF) to each amplifier dominant pole.

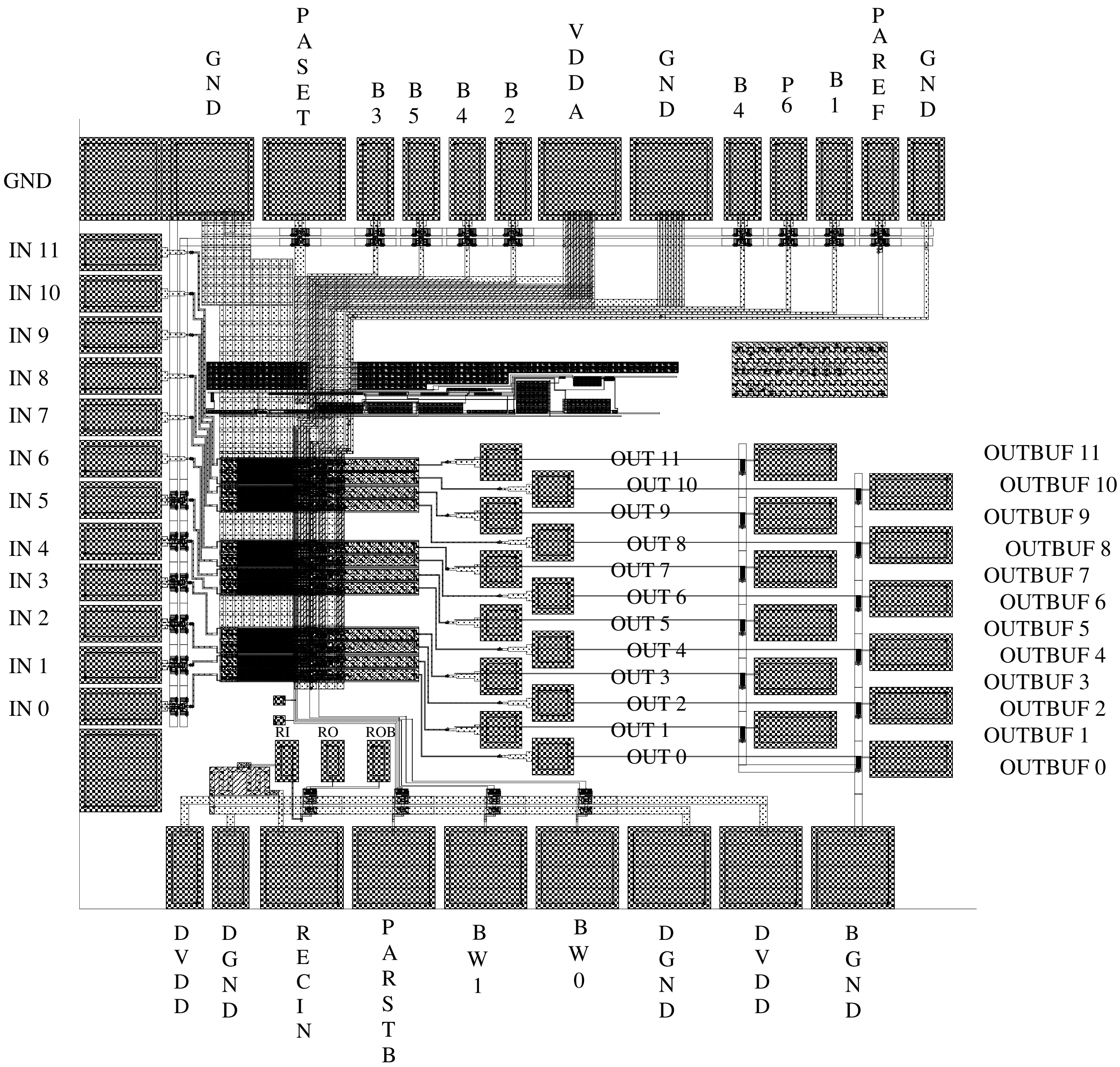

Figure 1: Pad assignment of the SVX4 preamplifier test chip

Note that these are nominal capacitance values. The actual capacitances will be determined by measurement.
8. **PAREF**: Sets DC level of preamplifier output and thus makes possible to maximize the dynamic range to either negative or positive charge. Should be set between 0.2 and 1 V.
9. **PASET**: Input to preamplifier bias circuit. Connected to ground via external resistor. Connected to AVVD via external capacitor.
10. **PARSTB**: Preamplifier (feedback capacitor) reset. Must be AVDD during charge injection. Setting PARSTB to ground initiates the reset.
11. **B1 - B5, P6**: Output of preamplifier bias circuit. Internally connected to preamplifier. These

lines have very high impedances and voltages cannot be sensed with a 10 MΩ DVM.

12. **RECIN**: isolated CMOS receiver input
13. **RI**: isolated CMOS receiver input after internal voltage division
14. **RO, ROB**: isolated CMOS receiver output (RO) and inverted output (ROB)
15. **DVDD, DGND**: Supply voltage for CMOS receiver. DVDD and DGND can be connected to VDDA and GND on the test chip board.

3 Test program

1. **Basic functionality tests**
2. **Rise time vs. input (detector) capacitance** C_{in}
C_{in} *is to be varied between 10 to 100 pF.*

3. **Rise time vs bandwidth setting**
The combinations of (BW1,BW0) = (0,0), (0,1), (1,0), (1,1) will be tested.

4. **Gain and rise time vs. supply voltage**
Vary supply voltage of 2.5 V by e.g. $\pm$ *0.1 and* $\pm$ *0.5 V.*

5. **Sensitivity to AVDD noise**
Inject pulses of e.g. $\pm$ *0.0001,* $\pm$*0.001,* $\pm$ *0.1 V to AVDD and measure rise time and gain changes. (No input pulse needed)*

6. **Dynamic Range**
Measure by keeping PAREF fixed at 0.7 V and varying input pulse magnitude, or by varying PAREF with a fixed small input pulse.

7. **Reset Stability**

8. **Output Noise**

9. **Comparison between different amplifiers** (no simulation)
Determine **yield**, **rise time** *and* **gain spread**.

10. **Test of radiation hardness** (no simulation)
Irradiation at the LBNL ^{60}*Co source is forseen.*

4 Simulated Output Waveforms

Default settings

The default settings for the simulations are:
IN 0 - IN 11: Coupled to *external* detector capacitor of 50 pF in series with *external* voltage divider of R1 = 2990 Ω and R2 = 10 Ω. A voltage step at the divider is chosen to inject a charge of 12 fC, corresponding to $\approx$ 3 mips.

Out 0 - Out 11: A load capacitor of 1340 fF is connected between **Out** and ground. (The bonding pad on each test chip output should provide a capacitance of this order.
Outbuf 0 - Outbuf 11: Connected to *external* 500 Ω resistor to AVDD in order to yield amplified and inverted signal with voltage gain of ≈ 6.8. To simulate the effect of the test measurement probe an *external* 20 pF capacitor is connected between **Outbuf** and ground.
VDDA = 2.5 V
BW0 - BW1: Both set to ground.
PAREF = 0.7 V
PASET: Connected to ground via external 1.8 kΩ resistor. Connected to AVVD=2.5 V via *external* 10 nF capacitor.

The temperature is set to 25°C. Except where stated otherwise, an *internal* capacitance of 40 fF is connected in parallel to the bandwidth adjusting capacitances. This is a guess as to the size of the parasitic capacitance present at this node of the test chip.

Results and Figures

Default waveforms

The input voltage (before R1/R2), reset signal and output signals **Out** and **Outbuf** are shown in Figure 2 for the default settings. For the default settings, the preamplifier rise time is ≈ 30 ns. The gain is ≈ 4.8 mV/fC. Note that the out signal cannot easily measured on the test chip because the preamplifier output cannot drive a large load.

The bias node voltages are given in Table 4. (Their measurement requires an internal DMV resistance of $> 1\text{G}\Omega$)

node	b1	b2	b3	b4	b5	p6	paset
voltage [mV]	592	529	743	1,510	1,524	1,881	66.57

Table 1: Bias voltages

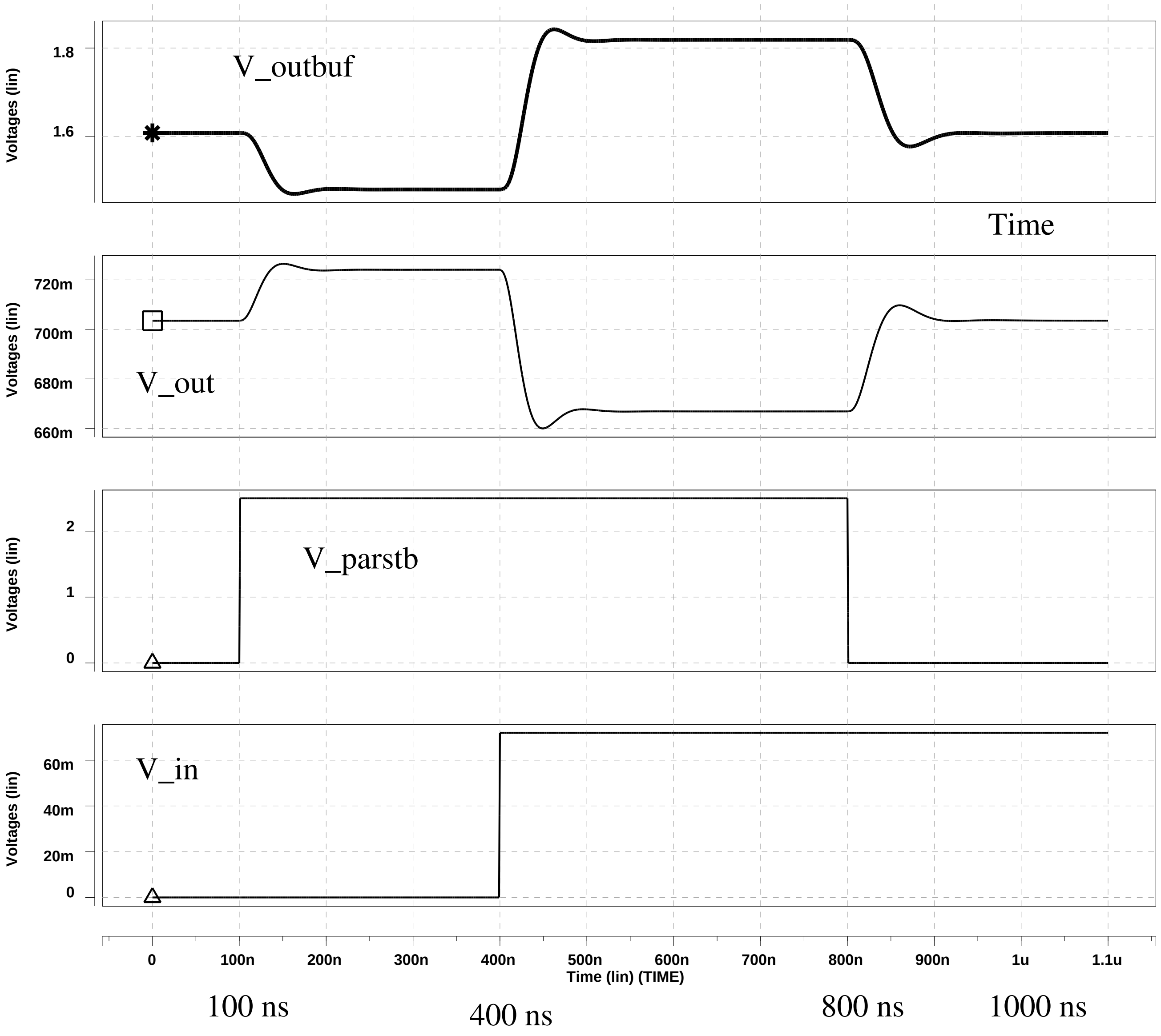

Figure 2: Input voltage, reset signal and output voltages.

Variation of detector capacitance

The effect of the detector capacitance is shown in Figure 3. For the simulated bandwidth combination (BW0,BW1) = (0,0) the 0-90% rise times are rather short and range between 20 and 100 ns. The rise times at the nodes Out and Outbuf differ due to the additional ‘probe’ capacitance of 20 pF connected to Outbuf.

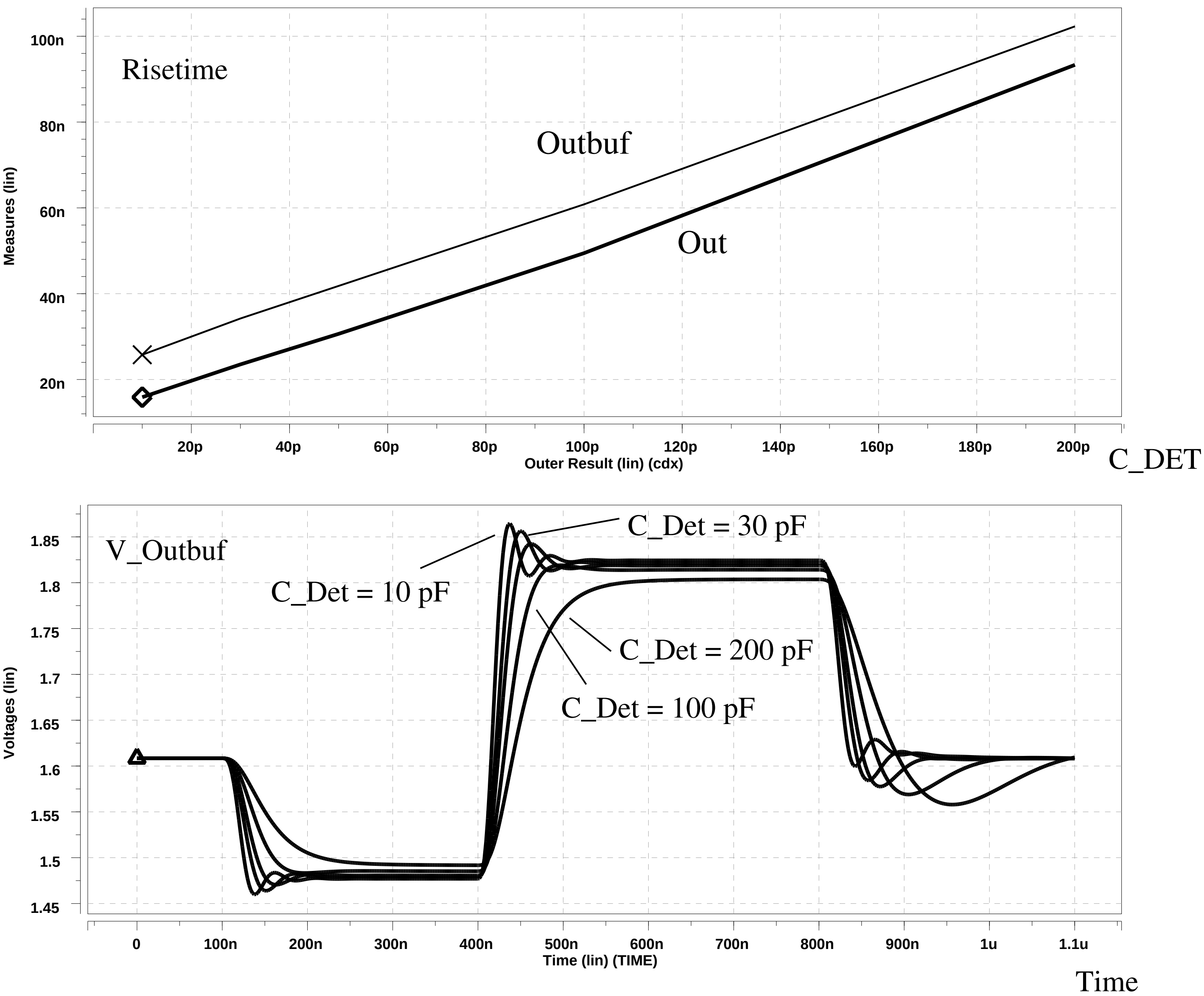

Figure 3: Variation of detector capacitance from 10 pF to 200 pF.

Variation of supply voltage

The effect of the supply voltage is shown in Figure 4. For the extreme variation of the supply voltage by ± 0.5 V, the simulated gain change is $\approx 1\%$. There is no significant change in rise time.

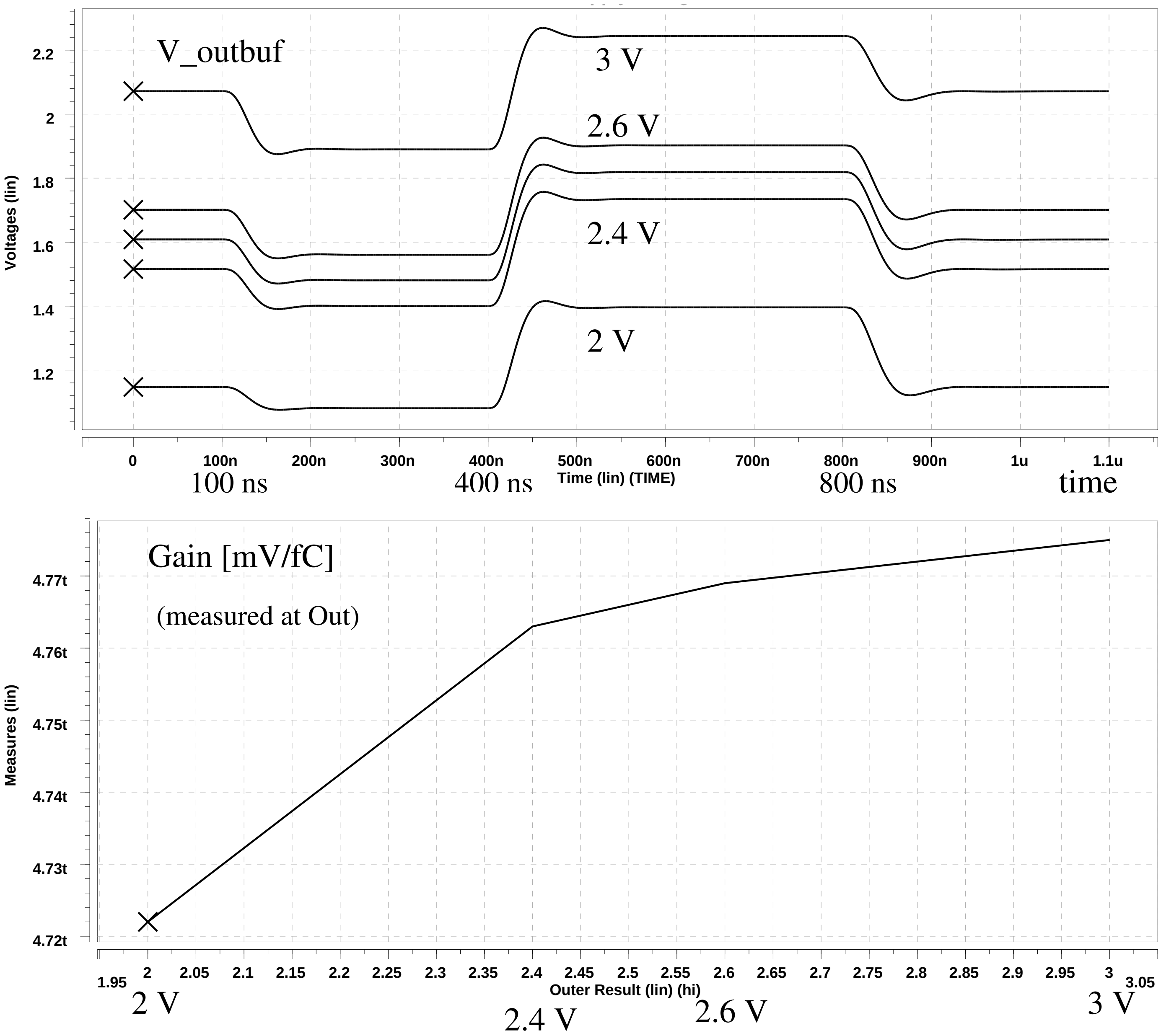

Figure 4: Variation of supply voltage from 2 to 3 V.

Variation of bandwidth setting

The effect of bandwidth bit selection is shown in Figure 5. For this simulation, we modified the preamplifier schematics by replacing the bandwidth transistors (M18,M19,M20 and M15,M16,M17) by a single capacitor $C_{bandwidth}$. This should allow an indirect measurement of the parasitic capacitances at the dominant pole of the preamplifier and of the size of the capacitances added by the bandwidth bits. The value of the input (detector) capacitor for these curves is 50 pF.

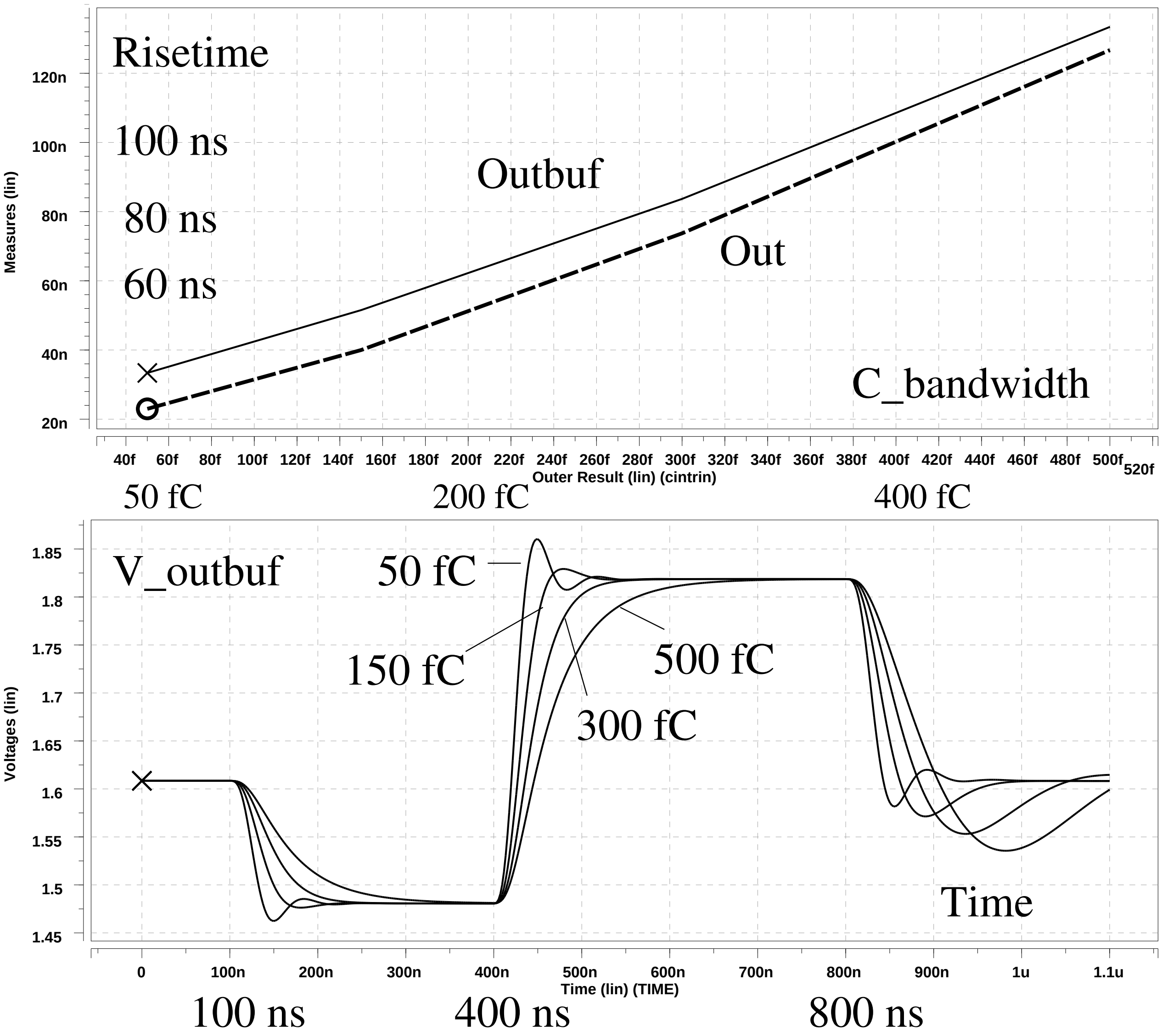

Figure 5: Variation of bandwidth capacitance from 50 fC to 500 fC.

Dynamic range

The dynamic range of the preamplifier is shown in Figure 6. The gain is constant within 1% for a range of ≈ 65 mips (260 fC). If only positive or negative charge is injected the value of PAREF must be shifted to small or large values to cover the maximum dynamic range.

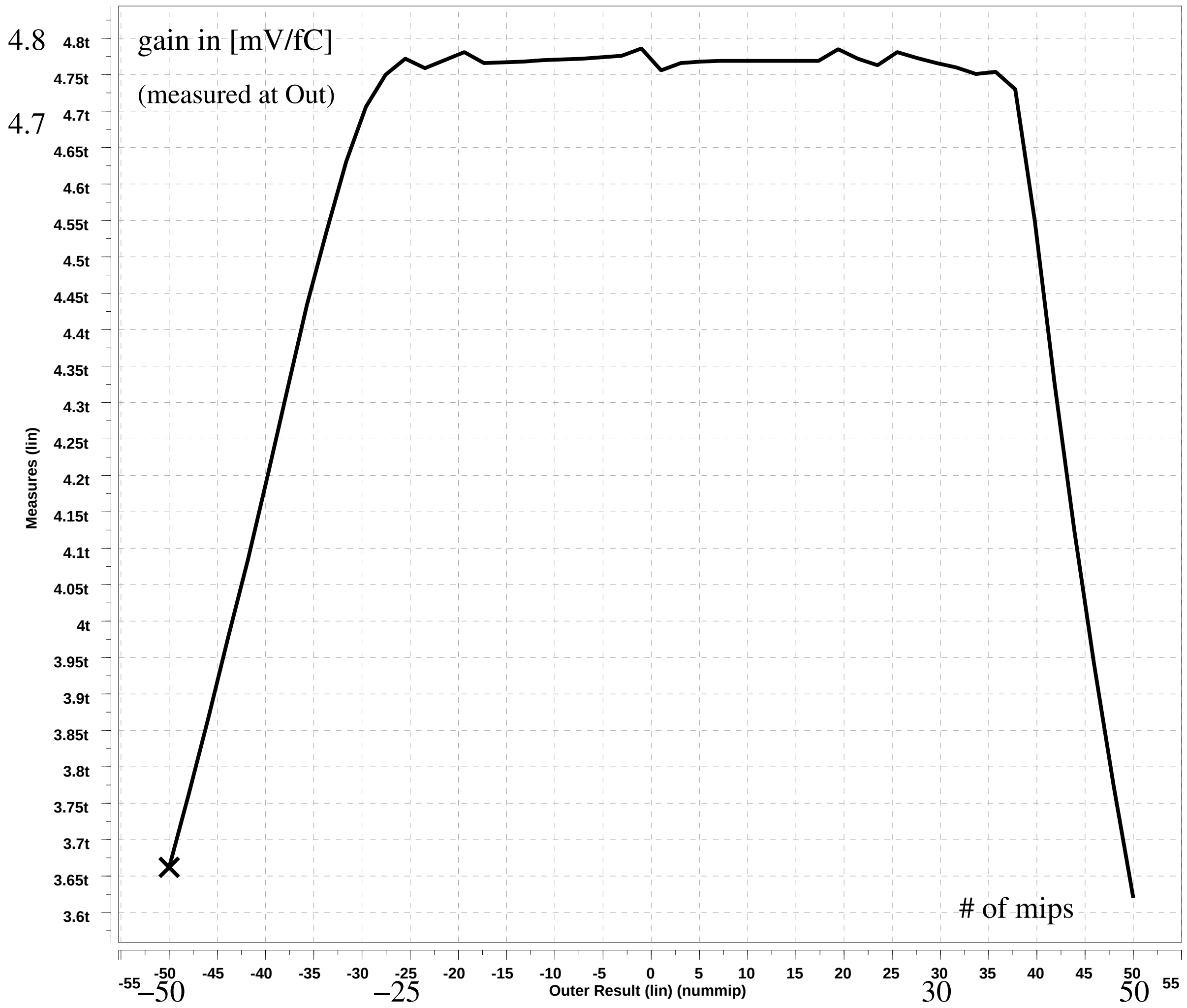

Figure 6: Preamplifier gain as function of injected charge (expressed in mips)

The corresponding output waveforms are shown in Figure 7 for injected charges of ± 1, ± 3, ± 6 and ±10 mips. (This corresponds to input voltages of ± 24, ± 72, ± 144 and ± 240 mV in our set-up).

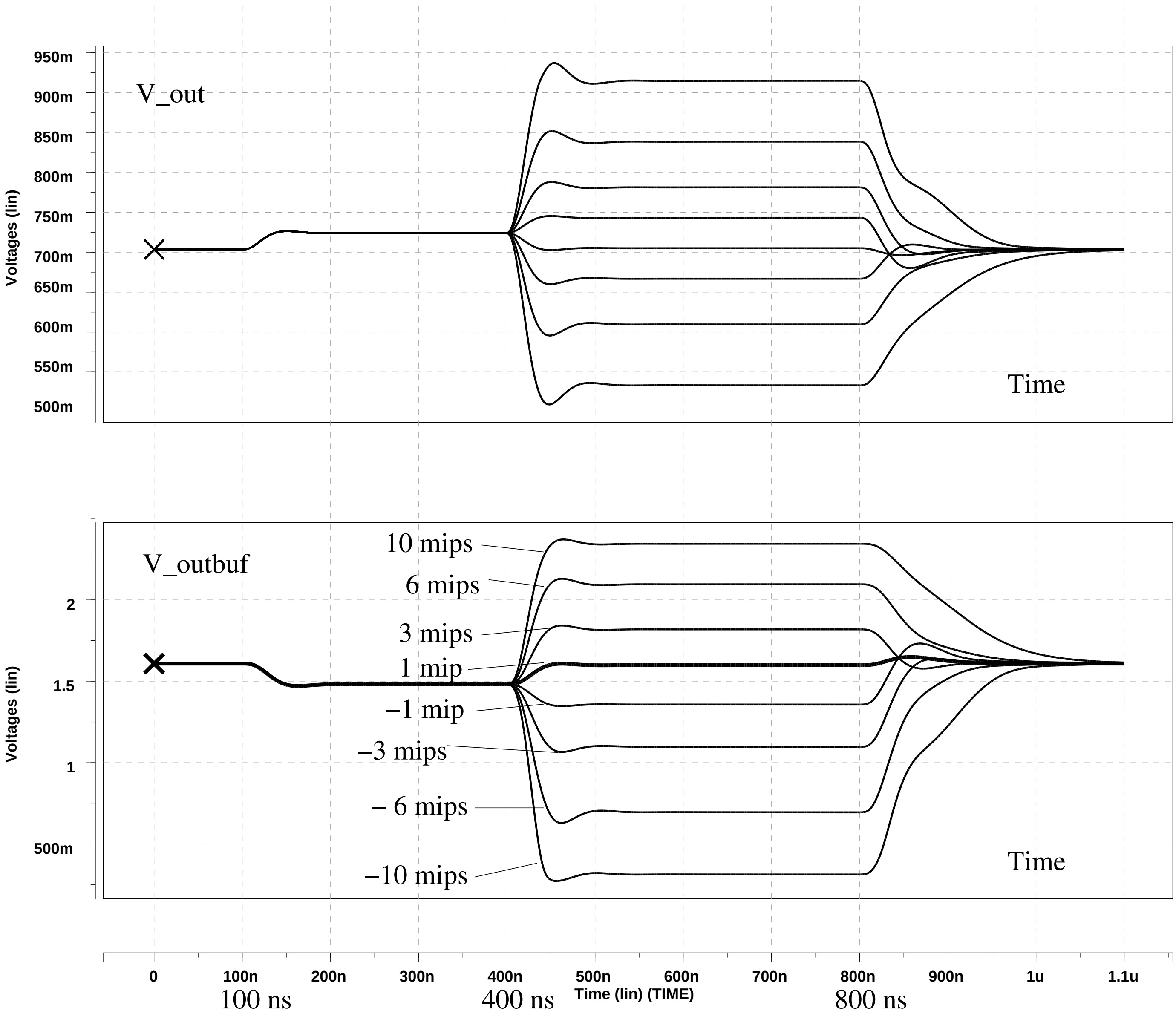

Figure 7: Variation of preamplifier output for different injected charges.

Reset stability

The reset time of the preamplifier depends on the stored charge, the detector (input) capacitance and the bandwidth capacitance. For the default scenario with 50 pF detector capacitance and 3 mips injected charge, the reset time is less than 100 ns.

In Figure 8 extreme scenarios are studied by setting the bandwidth capacitance to 400 fF and by injecting larger charges. (Here we replace the bandwidth transistors as for Figure 5, and PAREF is set to 1 V.) Reset times larger than 800 ns can be observed for an accumulated charge of 50 mips.

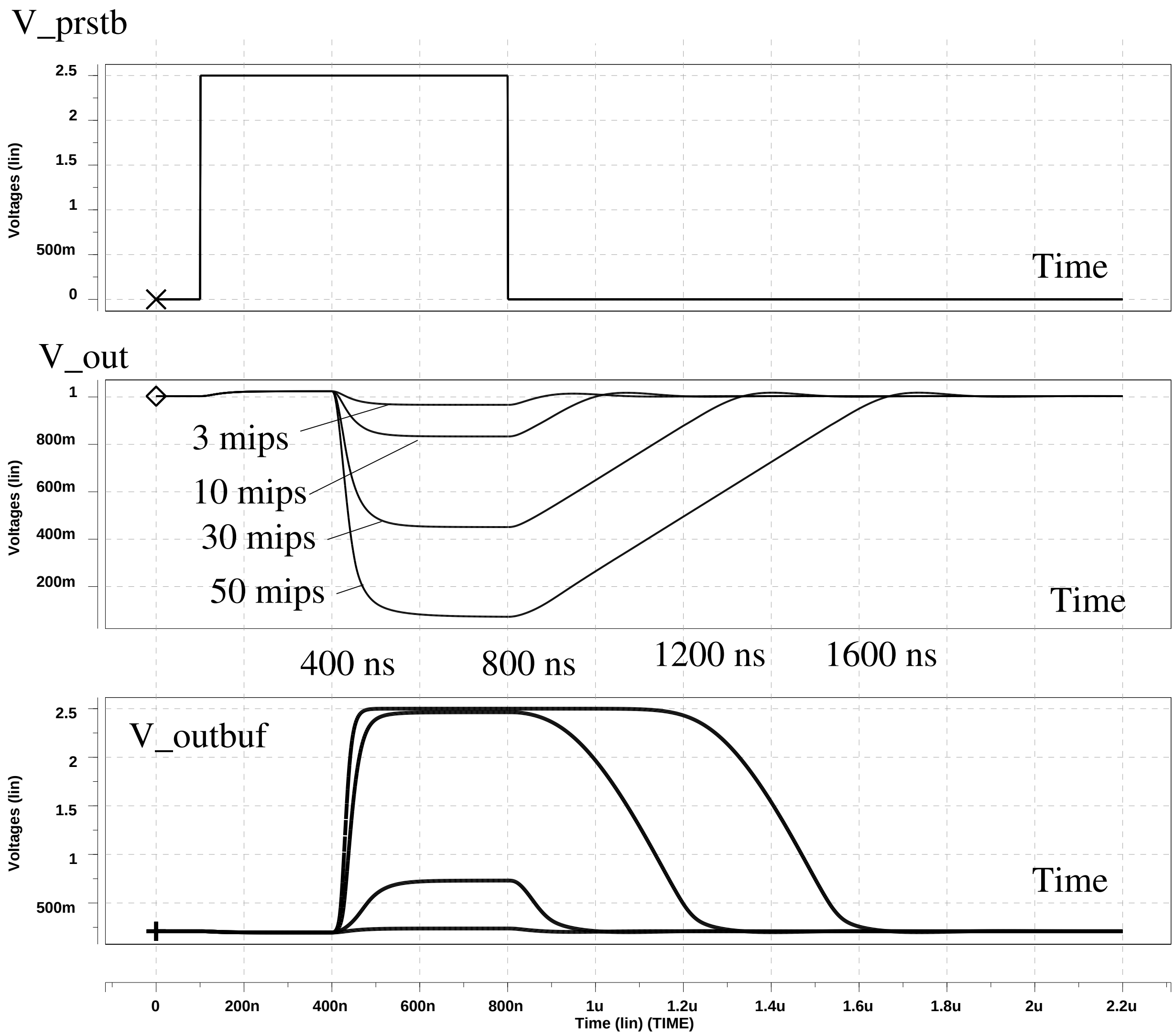

Figure 8: Reset time for different input charges.

Acknowledgements

We would like to acknowledge the work of Oren Milgrome (LBNL) and Andrea Neviani (Padova) who designed the preamplifier, and the contribution of Gerit Medeller (LBNL) to the submission of the test chip.

Appendix

The appendix contains the schematics of the preamplifier, the preamplifier bias circuit, the CMOS receivers and the output buffers. In addition, the SPICE net list is given.

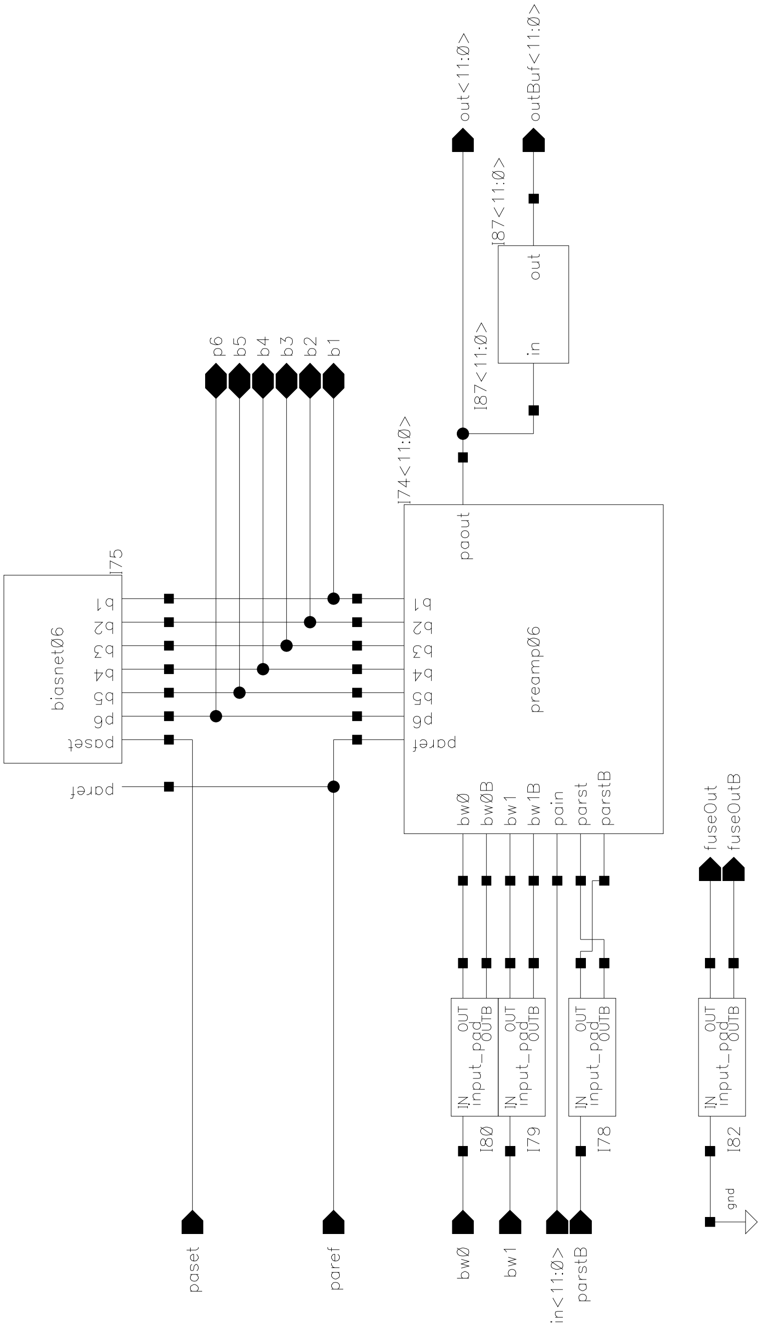

Figure 9: Overview of test chip schematics.

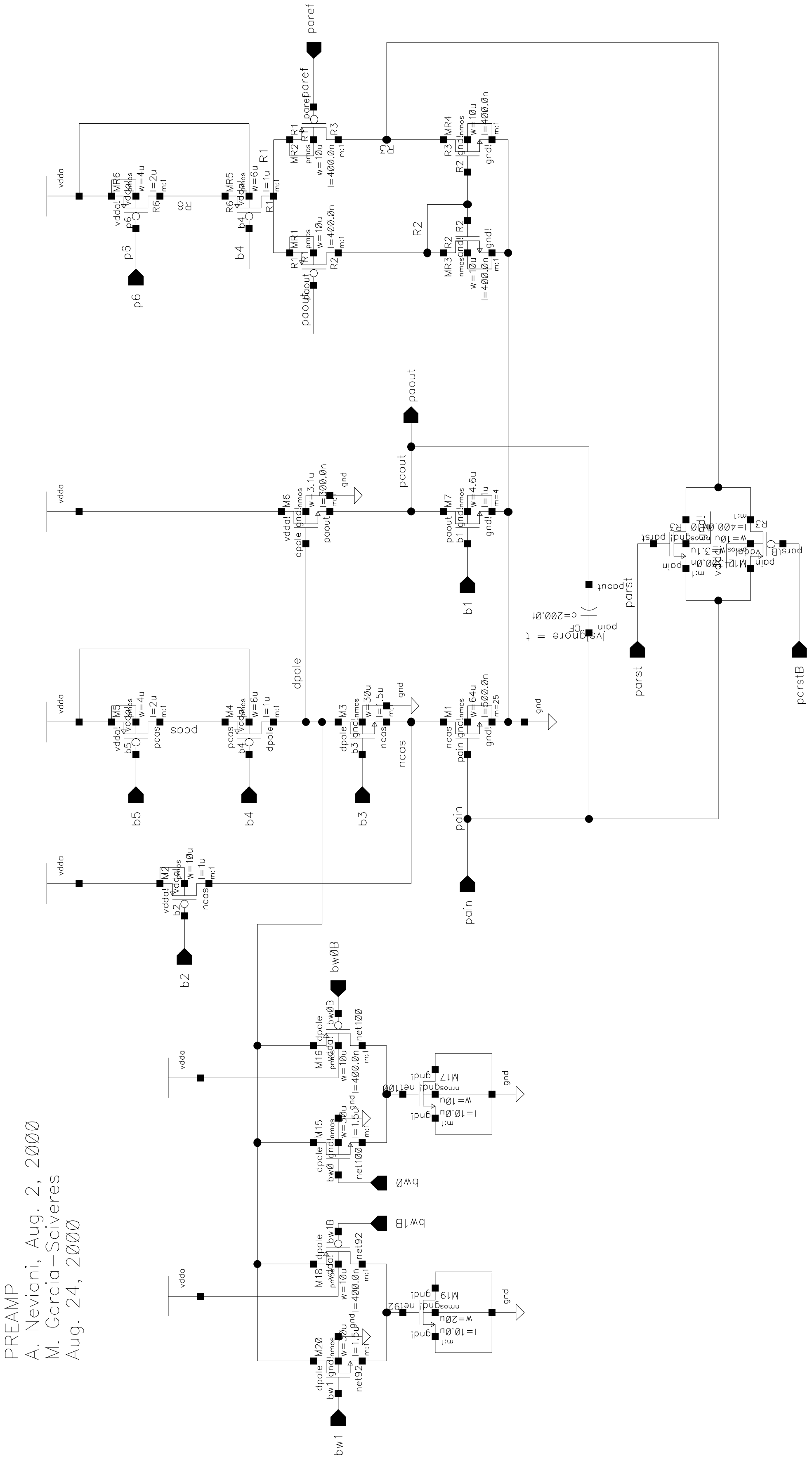

Figure 10: Schematics of preamplifier (1 channel).

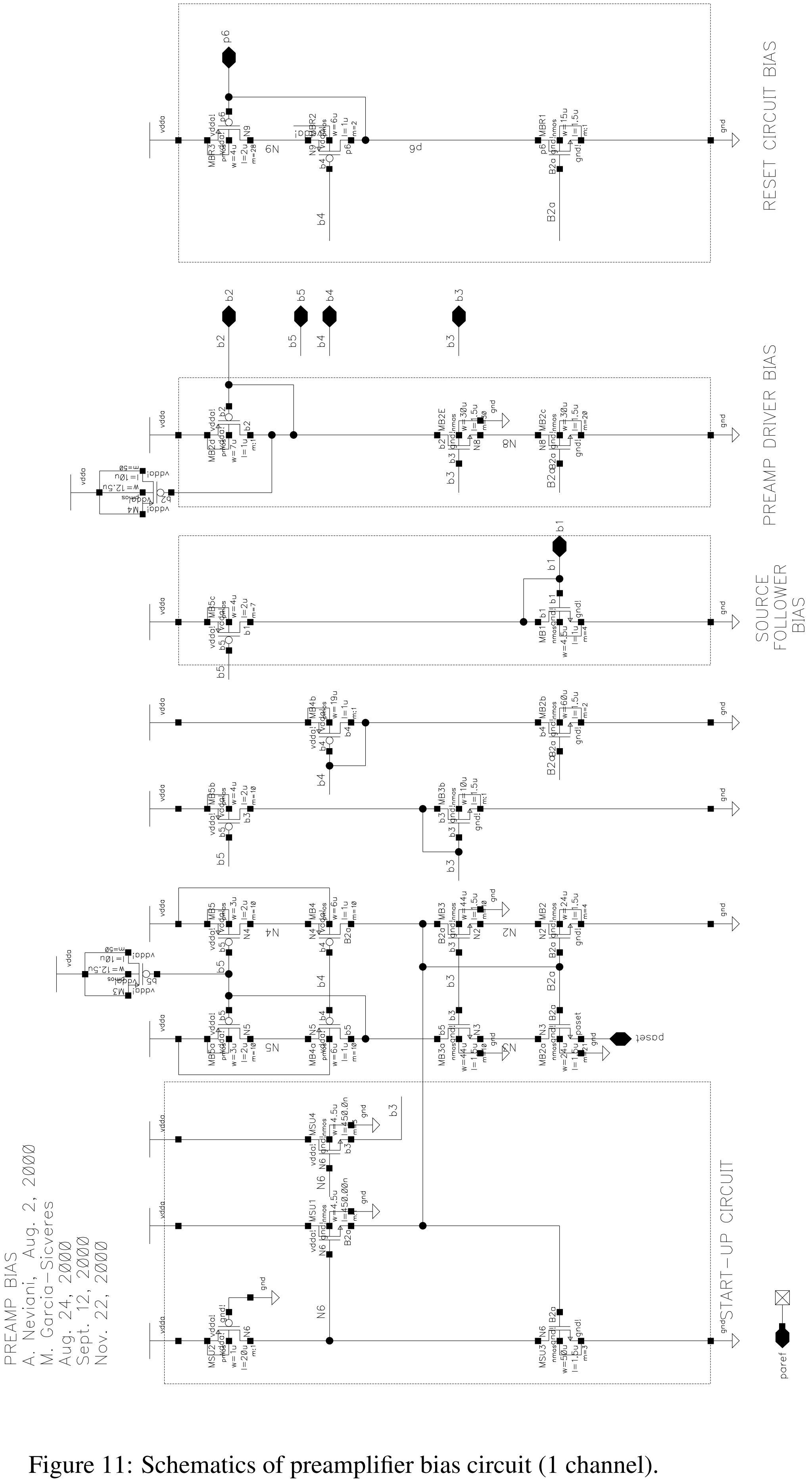

Figure 11: Schematics of preamplifier bias circuit (1 channel).

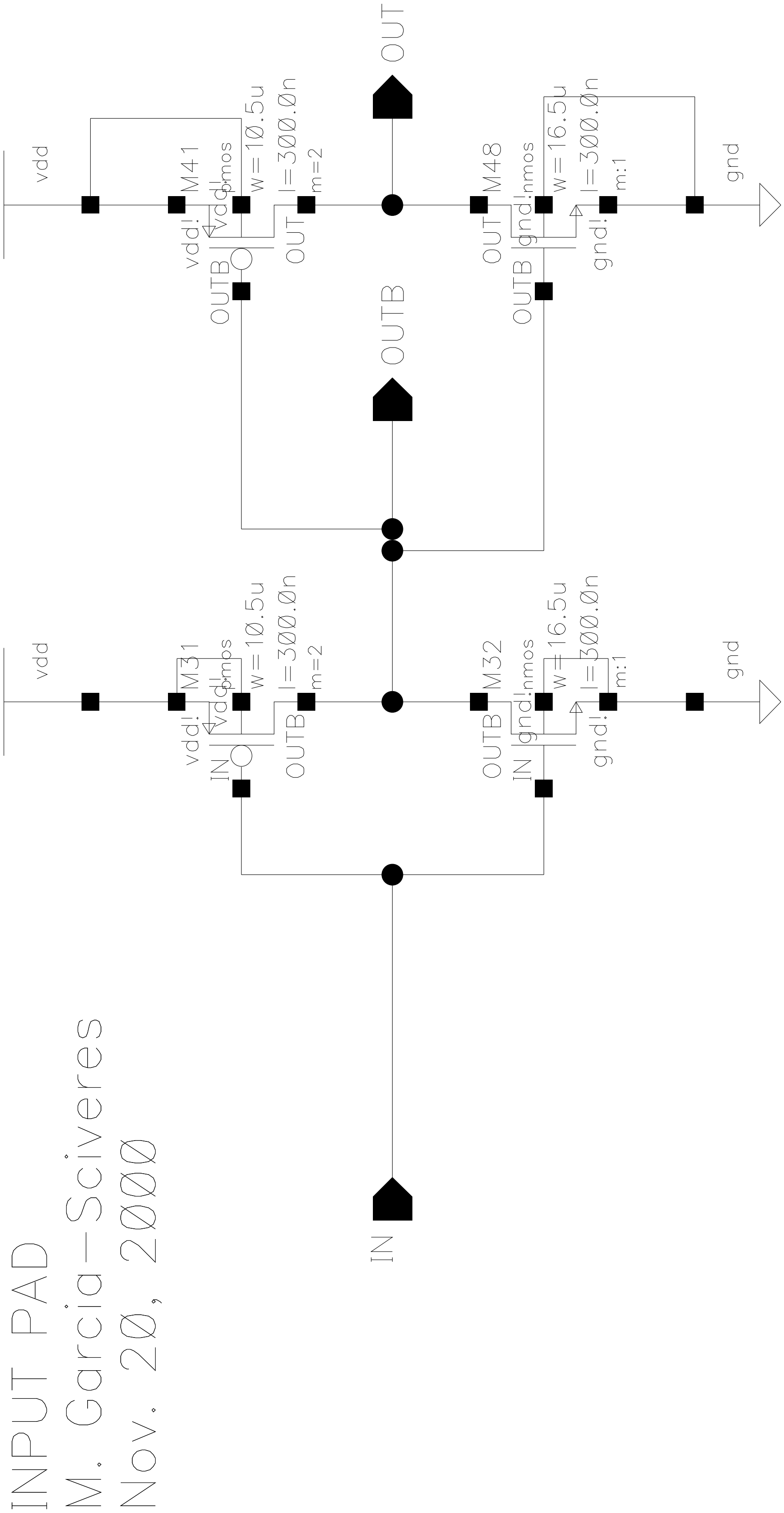

Figure 12: Schematics of CMOS receiver (1 channel).

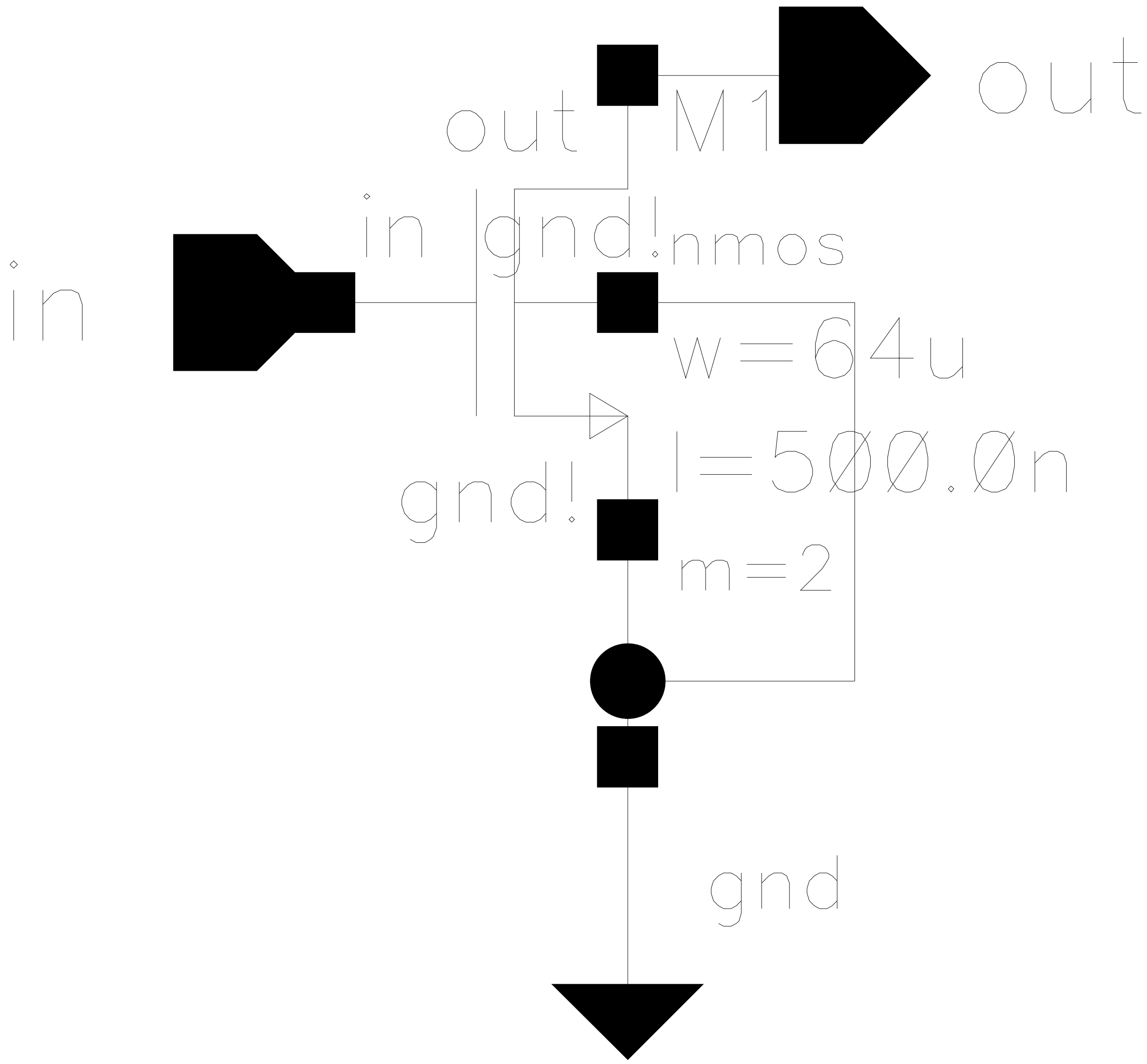

Figure 13: Schematics of output buffer (1 channel).

Test chip net list:

Preamp

.SUBCKT OPAG1 102 103 104 105 106 107 151 108 152 147 153 154 148 155 149

CF 153 154 200E-15
CDPOLE 157 0 CINTRIN
M18 156 152 157 AVDD! PCH L=400E-9 W=10E-6 M=1
M16 158 151 157 AVDD! PCH L=400E-9 W=10E-6 M=1
M12 159 149 153 AVDD! PCH L=400E-9 W=10E-6 M=1
MR6 160 147 AVDD! AVDD! PCH L=2E-6 W=4E-6 AD=2.96E-12 AS=2.96E-12 PD=5.48E-6 +PS=5.48E-6 M=1
MR5 161 105 160 AVDD! PCH L=1E-6 W=6E-6 AD=3.7E-12 AS=3.7E-12 PD=6.48E-6 +PS=6.48E-6 M=1
MR2 159 148 161 161 PCH L=400E-9 W=10E-6 M=1
MR1 162 154 161 161 PCH L=400E-9 W=10E-6 M=1
M2 163 103 AVDD! AVDD! PCH L=1E-6 W=10E-6 AD=4.44E-12 AS=4.44E-12 PD=7.48E-6 +PS=7.48E-6 M=1
M5 164 106 AVDD! AVDD! PCH L=2E-6 W=4E-6 AD=2.96E-12 AS=2.96E-12 PD=5.48E-6 +PS=5.48E-6 M=1
M4 157 105 164 AVDD! PCH L=1E-6 W=6E-6 AD=3.7E-12 AS=3.7E-12 PD=6.48E-6 +PS=6.48E-6 M=1
M19 0 156 0 0 NCH L=10E-6 W=20E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
M20 157 108 156 0 NCH L=1.5E-6 W=30E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
M17 0 158 0 0 NCH L=10E-6 W=10E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
M15 157 107 158 0 NCH L=1.5E-6 W=30E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
M10 159 155 153 0 NCH L=300E-9 W=3.1E-6 AD=600E-15 AS=8.2E-12 PD=2.9E-6 +PS=11.4E-6 M=1
MR3 162 162 0 0 NCH L=400E-9 W=10E-6 M=1
MR4 159 162 0 0 NCH L=400E-9 W=10E-6 M=1
M6 AVDD! 157 154 0 NCH L=300E-9 W=3.1E-6 AD=600E-15 AS=8.2E-12 PD=2.9E-6 +PS=11.4E-6 M=1
M7 154 102 0 0 NCH L=1E-6 W=4.6E-6 AD=600E-15 AS=18.2E-12 PD=2.9E-6 PS=17E-6 +M=4
M3 157 104 163 0 NCH L=1.5E-6 W=30E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
M1 163 153 0 0 NCH L=500E-9 W=64E-6 AD=24.3E-12 AS=102.4E-12 PD=63.7E-6 +PS=73.1E-6 M=25
.ENDS OPAG1

Input Pad (CMOS receiver)
.SUBCKT SUB1 165 166 167

M41 166 167 AVDD! AVDD! PCH L=300E-9 W=10.5E-6 AD=3.7E-12 AS=3.7E-12 PD=6.48E-6 +PS=6.48E-6 M=2
M31 167 165 AVDD! AVDD! PCH L=300E-9 W=10.5E-6 AD=3.7E-12 AS=3.7E-12 PD=6.48E-6 +PS=6.48E-6 M=2
M48 166 167 0 0 NCH L=300E-9 W=16.5E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
M32 167 165 0 0 NCH L=300E-9 W=16.5E-6 AD=10.12E-12 AS=91.94E-12 PD=27.33E-6 +PS=45.5E-6 M=1
.ENDS SUB1

OP BIAS
.SUBCKT SUB2 102 103 104 105 106 147 148 150

CB2 AVDD! 106 100p
CB5 AVDD! 103 100p
MBR3 168 147 AVDD! AVDD! PCH L=2E-6 W=4E-6 AD=2.96E-12 AS=2.96E-12 PD=5.48E-6 +PS=5.48E-6 M=28
MBR2 147 105 168 AVDD! PCH L=1E-6 W=6E-6 AD=3.7E-12 AS=3.7E-12 PD=6.48E-6 +PS=6.48E-6 M=2
MB5C 102 106 AVDD! AVDD! PCH L=2E-6 W=4E-6 M=7
MB2D 103 103 AVDD! AVDD! PCH L=1E-6 W=7E-6 M=1
MSU2 169 0 AVDD! AVDD! PCH L=20E-6 W=1E-6 M=1
MB5A 170 106 AVDD! AVDD! PCH L=2E-6 W=3E-6 M=10
MB5B 104 106 AVDD! AVDD! PCH L=2E-6 W=4E-6 M=10
MB5 171 106 AVDD! AVDD! PCH L=2E-6 W=3E-6 M=10
MB4B 105 105 AVDD! AVDD! PCH L=1E-6 W=19E-6 M=1
MB4A 106 105 170 AVDD! PCH L=1E-6 W=6E-6 M=10
MB4 172 105 171 AVDD! PCH L=1E-6 W=6E-6 M=10
MBR1 147 172 0 0 NCH L=1.5E-6 W=15E-6 M=1
MSU4 AVDD! 169 104 0 NCH L=450E-9 W=4.5E-6 M=3
MB1 102 102 0 0 NCH L=1E-6 W=4.5E-6 M=4
MB2C 173 172 0 0 NCH L=1.5E-6 W=30E-6 M=20
MB2E 103 104 173 0 NCH L=1.5E-6 W=30E-6 M=30
MSU3 169 172 0 0 NCH L=1.5E-6 W=50E-6 M=3
MSU1 AVDD! 169 172 0 NCH L=450E-9 W=4.5E-6 M=1
MB3B 104 104 0 0 NCH L=1.5E-6 W=10E-6 M=1
MB3 172 104 174 0 NCH L=1.5E-6 W=44E-6 M=10
MB3A 106 104 175 0 NCH L=1.5E-6 W=44E-6 M=10
MB2A 175 172 150 0 NCH L=1.5E-6 W=24E-6 M=21
MB2B 105 172 0 0 NCH L=1.5E-6 W=60E-6 M=2
MB2 174 172 0 0 NCH L=1.5E-6 W=24E-6 M=4

.ENDS SUB2

Preamp pad output buffer
.SUBCKT SUB3 182 183

M1 183 182 0 0 NCH L=500E-9 W=64E-6 AD=24.3E-12 AS=102.4E-12 PD=63.7E-6 +PS=73.1E-6 M=2
.ENDS SUB3

Full test chip (12 channels, output buffers etc.)
.SUBCKT SUB4 102 103 104 105 106 107 108 109 146 111 123 110 147 148 149 150

```
* INPUT (CMOS RECEIVER): standalone!, bw0, bw1, prstb
XI82 0 109 146 SUB1
XI80 107 176 177 SUB1
XI79 108 180 181 SUB1
XI78 149 178 179 SUB1
* OP BIAS
XI75 102 103 104 105 106 147 148 150 SUB2
* OUTPUT BUFFER
X15 123 110 SUB3
* PREAMP
X17 102 103 104 105 106 176 177 180 181 147 111 123 148 179 178 OPAG1
.ENDS SUB4
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