SILICON CARBIDE BURIED-GATE JUNCTION FIELD-EFFECT TRANSISTORS FOR HIGH-TEMPERATURE POWER ELECTRONIC APPLICATIONS

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Abstract

Discrete medium-power diodes and field-effect transistors are expected to be among the first high-temperature silicon carbide (SiC) electronic components incorporated into advanced aerospace propulsion systems. Using its recently developed site competition epitaxy technique, NASA Lewis Research Center has fabricated and characterized several batches of buried-gate junction field-effect transistors (JFET's) which exhibit very promising characteristics. Despite the severe device area limitations (of approximately 1 mm^2) imposed by present-day SiC wafer defect densities, 100 V 6H-SiC JFET's exhibiting peak drain currents in excess of 1 A at room temperature have been realized. Decreasing channel electron mobility substantially diminished the current-carrying capability of the depletion-mode JFET's at higher temperatures. However, all JFET's tested at high temperatures demonstrated excellent low-leakage turn-off characteristics through the 873 K (600 °C) peak measurement temperature employed in this work. The duration of 873 K functionality in air appeared to be limited by contact metal oxidation. Nevertheless, operation with minimal I-V degradation after 30 hours in air at 873 K was achieved in one batch of transistors.

INTRODUCTION

Silicon carbide (SiC) electronics are being developed for use in harsh conditions where silicon, the semiconductor used in nearly all of today's electronics, cannot function. Silicon carbide's demonstrated ability to function under extreme high-temperature, high-power, and/or high-radiation conditions will enable significant improvements to a far-ranging variety of applications and systems. These range from improved high-voltage switching for energy savings in public electric power distribution and electric vehicles to more powerful microwave electronics for radar and cellular communications to sensors and controls for cleaner-burning, more fuel-efficient jet aircraft and automobile engines. Silicon carbide electronics will also figure into a variety of NASA missions, from planetary probes needing to withstand high-radiation space environments and Venus's scorching 723 K (450 °C) atmosphere to advanced supersonic and hypersonic aerospace vehicles which will need advanced sensor and control electronics operating in excess of 823 K (550 °C). Along with small scale detector and amplification circuits, discrete medium-power diodes and field-effect transistors (FET's) are expected to be among the first SiC electronic components incorporated into these systems (Przybylko, 1993). This paper documents recent advancements that have been made on prototype high-temperature junction field-effect transistors (JFET's) at NASA Lewis Research Center.

APPROACH

The buried-gate JFET device structure was chosen for prototype development because of its straightforward design and fabrication simplicity and the fact that both source/drain (n-type) and gate (p-type) ohmic contacts could be made to epitaxially-grown degenerate material. The buried-gate JFET device structure shown in Fig. 1 was grown by atmospheric chemical vapor deposition on a substrate cut from commercially available Cree 6H-SiC wafers polished 3° to 4° off the (0001) basal plane. The system and general growth procedures are described elsewhere (Powell et al., 1992; Powell et al., 1991), but the key degenerately-doped ohmic n-type contact layer was produced using one aspect of the novel site-competition epitaxy process developed at NASA Lewis (Larkin et al., 1994). By growing the n^+ contact layer at a relatively high silicon to carbon atomic ratio, the amount of nitrogen incorporated into the growing SiC epilayer is greatly enhanced by the fact that there is little carbon species present in the reactor to "compete" with nitrogen for the carbon lattice sites that nitrogen normally occupies when it dopes SiC. This has enabled growth of epitaxial SiC contact layers so degenerate that a wide variety of metallizations form "ohmic-as-deposited" contacts to both n^+ and p^+ layers, needing no thermal annealing to show linear ohmic behavior (Petit et al., 1994). Because a wider variety of as-deposited and annealed metallization schemes are suitably ohmic on the degenerately doped material produced by site-competition epitaxy, our research was able to focus mostly on 1) achieving longer term contact metallization stability at 873 K (600 °C), and 2) achieving discrete devices with state-of-the-art (for SiC) turn-on currents. In contrast to previous SiC contact work in which high-temperature contact stability was tested in relatively inert vacuum environments (Crofton et al., 1994), it should be noted that our performance criteria included the extra difficulty of attaining the 873 K contact stability in the oxidizing environment of atmospheric air.

The fabrication process started by liftoff patterning an aluminum etch mask, after which JFET mesas were etched to a depth of approximately 1 μm using reactive ion etching (RIE) in 91 % CHF_3 : 9 % O_2. Once the mesa etch mask was stripped, source/drain contact metal etch masks were similarly applied and liftoff-patterned, and a second RIE was carried out to define the active channel by removing the n^+ ohmic contact layer. In the case of devices designed for higher-current operation, the RIE etch mask also served as the ohmic contact, resulting in a "self-aligned" device configuration. In other device samples, the metal recess etch mask was stripped, and specialized high-temperature ohmic contact metallizations (described below) were applied and patterned by liftoff in a non-self-aligned manner. Electrical measurements were carried out by wafer probing the JFET's on a heating stage using standard curve tracers and computer-controlled source-measure units.

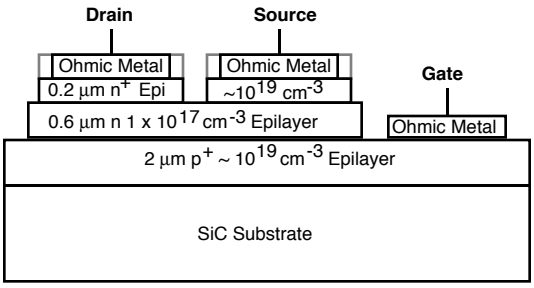

FIG. 1. 6H-SiC Buried-Gate JFET Cross-Section.

HIGH TEMPERATURE DEVICE RESULTS

Since SiC itself is chemically stable and electrically viable at 873 K, the key to achieving longer-term high-temperature JFET functionality is to prevent metallic reactions which degrade the ohmic property of the metal contacts. Previous work demonstrated that sputtered Mo, Ta, and Ti contacts to degenerate SiC epilayers grown by site competition epitaxy are ohmic-as-deposited. Moreover, these contacts demonstrated no detectable contact resistivity degradation over the course of 55-hour

873 K vacuum anneals (Petit et al., 1994). Unfortunately, these contact materials fail when subjected to the more stringent operational requirement of prolonged 873 K functionality in atmospheric air, as they readily took part in oxidizing reactions that greatly degraded the electrical properties of the contact. In an attempt to prevent these vacuum-stable ohmic contact materials from oxidizing in the high-temperature air environment, we employed multi-layer structures based on the general principle of applying non-oxidizing Pt cap layers to protect the more-readily oxidizable underlayers. This approach was largely unsuccessful, as deposited Pt layers failed to keep oxygen away from the ohmic underlayers. A multilayer contact of 500 Å Mo / 1000 Å Pt lost ohmic character in less than 1 hour in air at 873 K, while a 250 Å Ta / 500 Å TaN / 600 Å Pt metallization failed in less than 15 hours. In both cases the ohmic contacts became Schottky-like in nature, causing undesirable 5 V to 10 V "knee" turn-on voltages in the JFET drain current characteristics. Prior to the air anneals, both structures had demonstrated negligible degradation when subjected to 15-hour 873 K vacuum anneals. Auger analysis of the contacts following the air-related failures revealed the abundant presence of oxygen in the Ta and Mo underlayers, supporting the model that oxidation played the primary role in atmospheric high-temperature contact degradation.

The most successful high temperature contact investigated was a sputtered 900 Å Si / 700 Å Pt structure. Unlike the metallizations discussed above, this particular metallization scheme was not linearly ohmic in its as-deposited state; however, the contacts became ohmic following the first of two 15-hour 873 K vacuum anneal treatments (Fig. 2). As can be seen in Fig. 3, the contact remained sufficiently ohmic after two 15-hour 873 K air anneals that there was little change in the room-temperature drain current characteristics of the 10 μm (gate length) x 90 μm (gate width) Si/Pt-contact JFET. However, closer inspection revealed that some contact degradation through oxidation did take place during the air anneal, albeit at a much slower rate than in the previous metallization schemes. In addition to the slightly nonlinear I-V behavior shown in Fig. 3, a degradation in the visual appearance of the Si/Pt contact, believed to be the formation of metal oxide, was also observed. Furthermore, shorter gate-length devices (5 μm x 90 μm and 2.5 μm x 90 μm), whose lower channel resistances would make them more sensitive to changes in contact resistance, exhibited reduced drain currents following the air anneal.

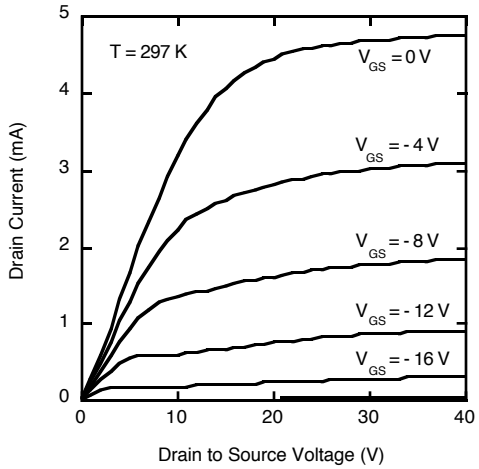

FIG. 2. 10 μm x 90 μm Si/Pt-Contact 6H-SiC JFET Drain Characteristics Measured at 297 K Following 30-hour 873 K Vacuum Anneal.

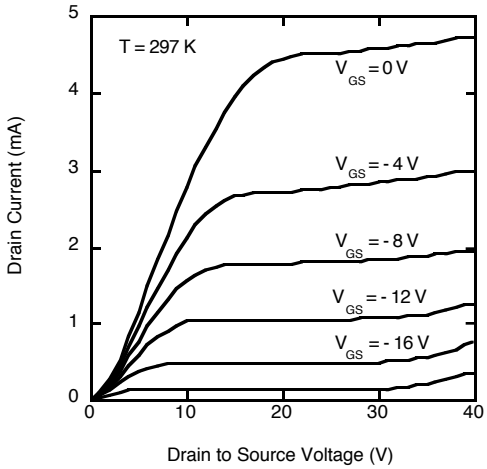

FIG. 3. 10 μm x 90 μm Si/Pt-Contact 6H-SiC JFET Drain Characteristics Measured at 297 K Following 30-hour 873 K Air Anneal.

The 873 K drain current characteristics of the Si/Pt-contact buried-gate JFET are shown in Fig. 4. The nearly four-fold reduction in drain current is somewhat larger than the nearly three-fold decrease reported by Dohnke et al. (1994) on similar 6H-SiC JFET devices over the same temperature spread. As illustrated by the subthreshold characteristics of Figure 5, the JFET's exhibited excellent low-leakage turn-off characteristics at room temperature and 873 K.

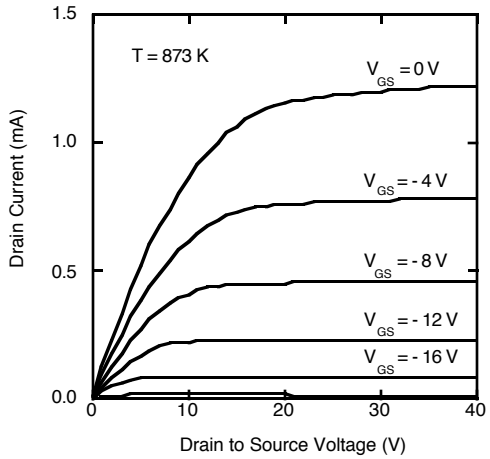

FIG. 4. 10 μm x 90 μm Si/Pt-Contact 6H-SiC JFET Drain Characteristics Measured at 873 K.

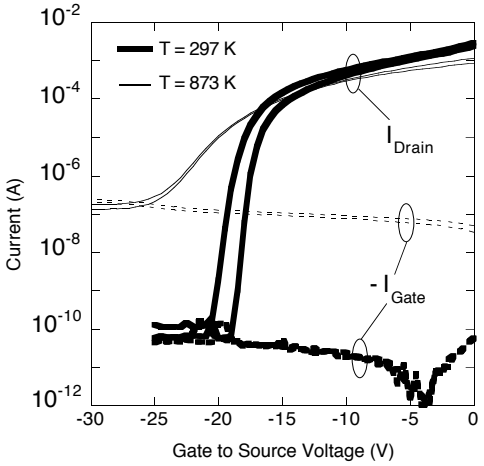

FIG. 5. 10 μm x 90 μm Si/Pt-Contact 6H-SiC JFET Turn-off Characteristics at 297 K and 873 K.

HIGH CURRENT DEVICE RESULTS

Though small-area SiC power devices reported to date have exhibited attractive current densities (Palmour et al., 1993), the defects present in commercial silicon carbide wafers confine functional SiC power device areas to around 1 mm^2 (Neudeck and Powell, 1994). This prevents high SiC current densities from being parlayed into high-current power devices. Despite this limitation, we nevertheless sought to realize a medium power SiC FET that could begin to approach more useful operating currents on the order of a few amps. Towards this end, we constructed highly compact self-aligned interdigitated finger buried-gate JFET's with ohmic-as-deposited aluminum contacts to highly degenerate cap layers produced by site competition epitaxy. Figure 6 shows the room temperature drain current characteristics of a 5 μm x 5.4 mm 6H-SiC JFET that occupies nearly 300 μm x 300 μm (9 x 10^{-4} cm^2) of chip area. The peak drain current (I_D) of 0.4 A at a drain voltage (V_{DS}) of 15 V translates into a peak current density of around 440 A/cm^2 for this 100 V device. However, since power FET's are typically used at low drain voltages, a more realistically applicable benchmark is the 0.1 A (110 A/cm^2)

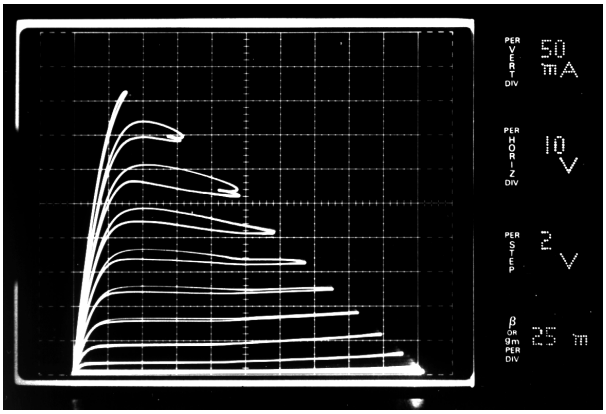

FIG. 6. 5 μm x 5.4 mm JFET Drain Characteristics at 297 K.

drain current at V_{DS} = 2 V. The measured room-temperature specific on resistance ($R_{DS(ON)}$) of this non-optimized 100 V lateral depletion-mode JFET is around 17 mΩ • cm^2.

The room-temperature drain current characteristics of a larger 2.5 μm x 21 mm self-aligned interdigitated finger 6H-SiC JFET which occupies a chip area of less than a third of a square millimeter (2.88 x 10^{-3} cm^2) is shown in Fig. 7. The drain current at V_{DS} = 2 V is 0.2 A (69 A/cm^2) leading to an apparent $R_{DS(ON)}$ of 29 mΩ • cm^2. However in contrast to the case when measuring smaller-area devices with higher total channel resistances, the 3 Ω probing resistance (as measured by shorting the probe tips to the same metal pad on the wafer) is significant compared to the 10 Ω measured total channel resistance. When this 3 Ω is subtracted, the $R_{DS(ON)}$ of the 100 V JFET becomes 20 mΩ • cm^2. Though not explicitly shown in Figure 7, these transistors were able to standoff 100 V drain-to-source voltages. To the best of the authors' present knowledge, the 1.2 A peak drain current exhibited in Figure 7 represents a record for any silicon carbide FET rated at 100 V or more with a less than 20 V switching gate voltage spread. The 100 V functional yield observed for these devices was less than 50 %.

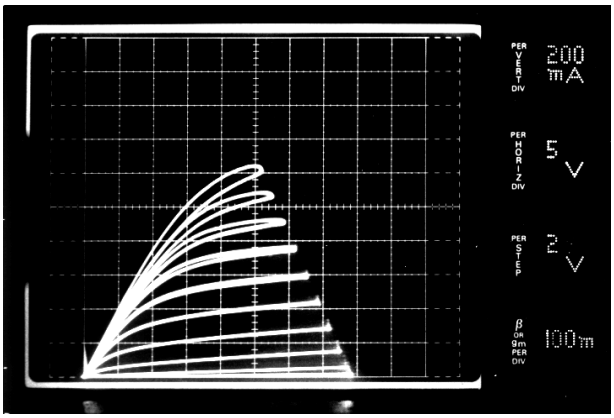

FIG. 7. 2.5 μm x 21 mm JFET Drain Characteristics at 297 K.

DISCUSSION & CONCLUSION

The lateral JFET device geometry (Fig. 1) is likely to have some application-specific advantages over other kinds of SiC power devices (MOSFET's, etc.) in terms of its ability to function reliably in high-temperature and high-radiation environments and its fabrication simplicity. However, it is clearly not the optimum configuration in which to implement a power FET, as vertical device geometries (in which the substrate serves as the drain contact) offer greatly superior performance. Therefore, it is no surprise that the performance of these lateral JFET's are orders of magnitude below the theoretical (vertical device) capabilities of SiC, and about an order of magnitude below highly optimized 100 V silicon power MOSFET's (Baliga, 1992). Nevertheless, the above results suggest that lateral SiC JFET's rated to around a few amps and several hundred volts are possible, despite the severe limitations imposed by present-day SiC wafer defect densities which effectively limit power devices to areas of around 1 mm^2 or less (Neudeck and Powell, 1994). By expanding the 0.4 A device design to an area of 1 mm^2 and implementing the device in 4H-SiC instead of 6H-SiC, peak room-temperature drain currents near 10 A (with 2 A operational currents at V_{DS} = 2 V) should be realizable.

In conclusion, 6H-SiC buried-gate JFET's demonstrating 1) stability for a duration of 30 hours in an 873 K (600 °C) air environment, and 2) 1.2 Amp/100-V operation have been reported in this communication. Process optimization is expected to yield further improvements in both high-temperature device stability and power performance, so that these devices can begin to meet the need for high-temperature electronic components in advanced aerospace systems.

Acknowledgments

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