SINGLE EVENT EFFECT PROTON AND HEAVY ION TEST RESULTS IN SUPPORT OF CANDIDATE NASA PROGRAMS

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Abstract

We present proton and heavy ion single event effect (SEE) ground test results for candidate spacecraft electronics. The variety of analog and digital devices tested includes ADCs, DC-DC converters, DRAMs, linear devices, and microprocessors.

I. Introduction

As spacecraft and spacecraft designers increasingly utilize increasing number of commercial technology devices versus the more traditional radiation hardened (RH) components in order to meet stringent spacecraft requirements in such areas as volume, weight, power, cost and schedule, SEE ground testing has become a key in many spaceflight programs.

The objective of this study was to determine the Linear Energy Transfer (LET) threshold (the minimum LET value to cause an effect at a fluence of 1E7 particles/cm2) and saturation cross section of candidate spacecraft electronics for Single Event Upset (SEU) and latchup (SEL) due

to protons and heavy ions.

II. Test Techniques and Setup

A. Heavy Ion Test Facility

The test facility used for heavy ion experiments was the Brookhaven National Laboratories (BNL) Single Event Upset Test Facility (SEUTF). The SEUTF utilizes a tandem Tandem Van De Graaf accelerator suitable for providing various ions and energies. Test boards containing the device under test (DUT) are mounted inside the vacuum chamber.

Ions used are listed in Table 1. Intermediate LETs were obtained by changing the angle of incidence of the DUT to the ion beam, thus changing the path length of the ion through the DUT.

Table 1 Test Ions

Ion	Energy, MeV	LET, MeV*cm2/mg
Cl-12	98	1.45
F-19	140	3.45
Cl-35	211	11.5
Ni-58	263	26.7
I-127	320	59.7
Au-197	341	181.9

Energies and LETs are nominal due to slight variances in the beam at multiple test dates during the calendar year. Particle fluxes for heavy ions were typically 1E3 - 1E5 particles/cm2.

B. Proton Test Facility

The test facility utilized for proton SEE testing was the University of California at Davis (UCD) cyclotron facility. Proton energies and fluxes were measured as those incident on the DUT package. Test energies ranged from 22 to 63 MeV incident upon the test device.

C. Test Method

Three modes of testing were used, depending on the DUT:

static	load device prior to beam irradiation, then retrieve data post-run counting errors (transients or bit flips)
dynamic	actively exercise a DUT during beam exposure while counting errors
biased (SEL only)	DUT is biased and clocked while Icc (power consumption) is monitored for SEL

All tests were performed at room temperature.

III. Test Results

A summary of devices and test results is seen in Table 3, following the paper.

Results and Discussion

Devices underwent full SEU/SEL characterization for heavy-ion only, unless otherwise stated.

A. FPGAs (Field Programmable Gate Arrays)

1. A1280A FPGA

The original objectives defined for this test were as follows
Mode 0: examines input buffer and serial shift register
Mode 1: examines output buffer and clock line

Each mode was to be tested with three patterns (all 1s, all 0s, and a checked pattern). During previous testing, this device displayed no clock dependency. However, Mode 0 was shown to be more SEU susceptible when the checked pattern was used. Examining this tendency was to be the main objective in this test. At 1 MHz, in Mode 0, with a checked pattern, this device drew a current of >40mA (as opposed to <5mA at the same speed and mode with a static pattern). The current was increased because the input to and output from the serial shift register was being toggled, this potentially causing the device to be more sensitive to SEUs.

Under this sensitive condition, the device was first exposed to an LET of 26.4, and was still functional after exposure to the beam. Next, an LET of 59.6 was used. Almost immediately the current soared to 80mA (double the original operating current) and a destructive condition occurred, rendering the device inoperable. Further testing and information concerning A1280 testing is available from R. Katz, et.al. [1]

B. EEPROMs (Erasable Electrically Programmable Read-Only Memory)

1. HN58C1001 Hitachi 1 Mbit (128Kx8) EEPROM

This device was tested for SEL only. Vcc, in standby mode, is 5V/4mA. SEL current was set to 50 mA. No sign of latchup was observed up to the maximum tested LET value of 90.

2. 28C256 SEEQ 256 kbit (32Kx8) EEPROM

This device was tested for SEL only. Nominal Vcc (in standby mode) is 5V/7mA. SEL current was set to 70mA. No sign of latchup was observed up to the maximum tested LET of 90.

C. Analog Devices

1. AD524 Precision Instrumentation Amplifier

The DUT was operated in-step with a reference device, with an input of a +5V peak to peak sine wave and an operating current of 3.6 mA. Output was compared at 10 kHz with ñ1V allowed for circuit noise. The devices were monitored for latchup (5mA). The SEU LETth was found to be ~ 11.5 with a maximum cross section of 1E-3 cm2/device. No SEL was observed for LETs up to 80.

2. AD565A High-Speed 12 bit DAC (Digital-to-Analog Converter)

Nominal Vcc was ñ12V at +4/-17mA. SEL current was set at +5mA/-20mA. The device was operated with an up-counter input for an analog sawtooth output. An SEU was defined as a difference of 0.5V or greater between DUT and a reference device. Under these test conditions, no SEUs or SEL were seen up to a maximum tested LET of 80. It is expected that transient errors of less than 0.5V may occur from heavy ions.

3. HS5212 12 bit ADC (Analog-to-Digital Converter)

For this test, the device's digital output was compared to an expected value. Any difference in the 7 most significant bits of output, equivalent to 160 mV at device input, was counted as an SEU. Noise in the test setup prevented higher resolution. LETth for zero upsets is ~ 1.44. The maximum device cross section is ~ 1.0E-3 cm2. The SEL LETth is > 80 at a cross section of < 1E-7 cm2.

4. 7820RP/372 8 bit ADC

This device was tested for SEL only. During irradiation, this device was supplied with +5V and a nominal Icc of 6mA, with latchup current set at 20mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 80, with cross section <1E-7 cm2/device.

5. DAC08AQ 8 bit DAC

This device is an 8 bit digital-to-analog converter where true current, not voltage, is output through dual complementary outputs. During irradiation, the DUT was operated in-step with a reference device. Output from the DUT was converted to voltage with a ñ10V output range. DUT and reference outputs were then compared via two analog comparators where any variance >50mA was counted as an SEU. Icc was a nominal 6mA with latchup current set at 8mA. SEU LETth was found to be ~ 3.5 with a maximum cross section of 1.9E-2 cm2/device. The device did not latch up for LET values up to 80.

Figure 1 shows device SEU cross section for several analog devices tested.

D. Power Devices [2]

1. SSP-21110-025 solid state power controller (SSPC)

The SSPC can be broken into two parts; a control section and a power section. The control section consists of densely populated proprietary ASICs and surface mount passive components. The ASICs are fabricated using bipolar technology. Control section operation was monitored by strip chart recorder, high-speed oscilloscope, and current limit checking, with no failures for LETs up to 80. The power section of the SSPC, consisting primarily of a number of NMOS power MOSFETs, was considered more susceptible to single event snapback (SES), single event burnout (SEB), and single event gate rupture (SEGR). Testing for SEB included operation of the devices with a highly capacitive source at maximum normal bus voltage (35V), maximum PPL derated current (19A), and angles of the ion beam ranging from normal to 22 degrees, while checking for uncommanded mode changes and

glitches in both static modes. No SEE, power or control, was detected for the devices for LETs up to 80 at a fluence of 1E7.

2. DC-DC Power Converters

The following six DC-DC power converters were all tested using the same test setup. Due to the constrictions of the beam diameter, the top and bottom portions of these devices were irradiated separately.

During irradiation, the DUT was operated in-step with a reference device while monitoring for four types of SEU. Steady state or level errors were discrepancies between reference and DUT outputs lasting longer than 1 microsecond. Glitch or transient errors were discrepancies between reference and DUT outputs lasting less than 1 microsecond. Destructive errors were indicated by high current conditions (SEL) and Single Event Gate Rupture (SEGR). Functional errors were device specific.

a. AHE2815 DC-DC power converter

This DC-DC power converter was tested with both normal input: 28V, 350mA (outputs 15V, 375mA), and also with 34V, 272mA input. Both glitch and steady state errors occurred, with an SEU LETth between 20 and 26. "Switchoff" errors sent the device into a non-functional mode, and required a power reset for the device to again function normally. This condition had an LETth between 20 and 26. The SEU LETth for PM errors was between 20 and 26.6. SEGR was seen at an LET of 59.6 on a single DUT sample with 28V input, and in another device at an LET of 26.6 with 34V input, but was not seen on other DUTs.

Figure 2 compares device SEU cross sections for the different types of SEU observed.

b. 2690R-D15F DC-DC power converter

This DC-DC power converter was tested both with nominal input 28V, 175mA (outputs 15V, 300mA), and also with 34V, 149mA input. Glitch and steady-state errors were not monitored. A spontaneous power reset error occured with LETth between 4 and 8. DUT output would drop from a nominal 15V down to 0V and back to 15V, with a typical reset hysteresis curve and a pulse width of approximately 10 msec. No destructive conditions were seen on any sample for LETs up to a max tested of 72, even with 34V input.

c. MFL2805S DC-DC power converter

This device is a DC-DC power converter with nominal inputs of 28V at 125mA, with a single output of 5V. No transient output errors or destructive conditions were seen on this device type, at LETs up to a max tested of 72.

d. MFL2812S DC-DC power converter

This device is a DC-DC power converter with nominal inputs of 28V at 180mA, and output of 12V. Steady state errors occurred, with LETth ~ 50, but glitch errors were not seen.

Device cross section for the steady-state error was 5E-6 cm2/device. No destructive conditions were seen on any sample at LETs up to a max of 72.

e. MFL2815D DC-DC power converter

This DC-DC power converter was tested both with normal input 28V, 410mA (dual 15V outputs), and also with 34V, 360mA input. A special condition of a steady-state error occurred which required a power reset. The condition had an LETth between 45 and 59.7. No destructive conditions were seen on any sample at LETs up to a max tested of 72.

f. MFL2815S DC-DC power converter

This DC-DC power converter was tested both with normal input 28V, 240mA (single 15V output), and also with 34V, 230mA input. No transient errors or destructive conditions were seen on this device type, up to a max LET tested of 72.

Figure 3 displays device SEU and SEL cross sections for several DC-DC Converters. Further information concerning SEE testing of these devices is available from LaBel, et.al. [2]

E. Linear Devices

1. LM119 Linear Comparator

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of +5V, 4mA, with latchup current set at 10mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 110, with cross section <1E-6 cm2/device.

2. LM139 Comparator

This device was tested for latchup only. At +8V with an operating current of 0.6mA, the DUT was input with a +5V square wave. Latchup current was 2mA. The device was found to be SEL immune for LETs up to 80.

3. LM193H Comparator

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of 5V, 0.4mA with a latchup current set at 1.5mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 100, with cross section < 1E-6 cm2/device.

4. LM108 Op amp

During testing, this device was operated in-step with a reference device. The device was supplied with ñ8V, with an operating current of 0.3mA. Latchup current was set at 0.6mA. The SEU LETth was ~ 24, with a maximum cross section of 5E-4 cm2/device. The SEL LETth was ~ 60. Note that only one sample of this device saw latchup, the other simply stopped functioning during testing at an LET of 60.

5. LM124 Op amp

This device was tested for latchup only. The DUT was supplied with +5V, and had an operating current of 0.7mA. Latchup current was set at 1.2mA. This device was found to be latchup immune for LETs up to 90. During irradiation, small decreases in current were observed.

6. LM158 Op amp

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of ñ12V, ñ10mA, with latchup current set at ñ25mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 100, with cross section <1E-6 cm2/device.

7. OP07AJ Op amp

Operating in-step with a reference device, input was a +5V peak-to-peak sine wave with an operating current of 1mA. Output was compared at 10 kHz with ñ 1V allowed for circuit noise. The devices were monitored for latchup (3mA). SEU LETth was between 11.5 - 13. Although latchup was not seen, both samples of the device were no longer functional after testing at an LET of 50. During irradiation, current decreases were observed which could be a result of Total Ionizing Dose (TID).

8. OP97 Op amp

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of +5V, 0.3mA, with latchup current set at 10mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 110, with cross section <1E-6 cm2/device.

9. PA10 Power Op amp

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of ñ40V, ñ10mA, with latchup current set at 45mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 100, with cross section <1E-6 cm2/device. Fluctuations on Icc were seen, potentially due to total dose placed on the device. No device failures were seen.

10. SMP11 Op amp

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of ñ12V, ñ10mA, with a latchup current set at ñ20mA. No SEL was seen on any runs up to an LET of 80. SEL was seen with an SEL LETth of 81.9, and cross section >1E-4 cm2/device. None of the three device samples were functional post-irradiation.

11. SE5521F Linear Signal Conditioner

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of 10V, 12.9mA, with a latchup current set at 18.0mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 100, with cross section <1E-6 cm2/device.

12. LM117H Linear Voltage Regulator

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of +5V, 3mA, with latchup current set at 25mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 110, with cross section <1E-6 cm2/device.

13. LM120H-12/883C Linear Voltage Regulator

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of +5V, 1.5mA, with latchup current set at 18mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 110, with cross section <1E-6 cm2/device.

14. LM136AH Linear Voltage Regulator

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of +5V, 1mA, with latchup current set at 15mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 110, with cross section <1E-6 cm2/device.

15. LP2951 Voltage Regulator

This device was tested for SEL only. a Vcc for this device was 7V, 50mA with SEL current set for 70 mA. Output for testing was set to 5.0V. No SEL was seen on this device up to the maximum tested LET of 90.

16. REF-02-373J Linear Voltage Reference

This device was tested for SEL only. During irradiation, the DUT was supplied with a Vcc of 15V, 1.0mA, with latchup current set at 2.0mA. No SEL was seen at the highest tested LET. Therefore, the SEL LETth is > 100, with cross section <1E-6 cm2/device.

F. DRAM (Dynamic Random Access Memory), Dual-Port RAM

1. KM44C4000AJ-7 16 Mbit Samsung DRAM

During irradiation, the DUT was supplied with 5V and an Icc of 14mA, with a latchup current of 100mA. It was operated in dynamic mode (read/write during irradiation) with a 4K refresh cycle. Most test runs used a checkerboard pattern input, but several used an all 0s and/or all 1s pattern. Test objectives were device characterization, gathering an angular data set, and identifying stuck bits and their addresses. Errors were seen at the initial LET of 1.46. The SEU LETth was < 1.46, with a cross section of 1.7E-7 cm2/bit. No pattern sensitivity or multiple upsets in a single word were seen. No latchup was seen at any time during testing.

Stuck bits, as well as single event functionality interrupt (SEFI - device goes into a test or standby mode and requires a reset or power reset to clear condition) were seen starting at normal incidence with an LET of 59.6. Devices along with stuck bit information and their addresses were given to Gary Swift of Jet Propulsion Laboratory, who is performing analysis on this phenomena.

2. TC5117400J-6 16 Mbit Toshiba DRAM

During irradiation, this device was supplied with a Vcc of 5V, 18mA, with a latchup current of 100mA. It was operated with a checkerboard pattern input, in dynamic mode (read/write during irradiation) with a 2K refresh cycle. Test objectives were device characterization, gathering an angular data set, and identifying stuck bits and their addresses. Errors were seen at the initial LET of 1.46. The SEU LETth was < 1.46, with a cross section of 1.8E-7 cm2/bit. No latchup, stuck bits or multiple upsets in a single word were seen at any time during testing.

3. 16 Mbit (4Mbitx4) DRAMs

The following six DRAMs were tested using the same setup. Tests used a checkerboard data pattern in Read/Modified Write mode; refresh cycle duration was device-dependent. Devices were run at a speed of 900 nsec. An SEU was defined as a noncompare in the data during the Read from one of the four data lines being monitored (one line for each 4MBit).

a. 8116400-60PJ 16 Mbit Fujitsu DRAM

This device was tested for both heavy ion and proton effects. Tests used a 4K refresh cycle (65.6 msec). Devices operated with a Vcc of 5V, 17mA. Latchup current was set at 100mA. During heavy-ion testing, the SEU LETth was found to be <1.41 with a cross section of ~3.5 cm2/device. It should be noted that SEFI, characterized by an anomalous increase in the SEUs counted/displayed in real-time during the test run, was seen at LET 50, after which the device was fully operable. The SEL LETth was > 80 with a cross section < 1E-7 cm2/device. Total dose failure was seen at > 30 kRad(Si).

During proton testing, both lidded and delidded samples were tested. The two types of samples show little difference with the maximum cross section > 1E-7 cm2/device. Cross section showed a slight linear increase with energy, but no significant angular dependency. During total dose testing, significant permanent increases in device Icc were seen (from an original 17mA to 25mA at 38.4 kRad), while the device remained fully functional. Total dose failure was observed at ~ 42 kRad(Si), rendering the device inoperable, with device current of 50mA.

b. HM5117400RR7 16 Mbit Hitachi DRAM

This device was tested for proton effects only. Tests used a 2K refresh cycle (32 msec). Devices operated with a Vcc of 5V, 17mA. Only lidded samples were tested. The cross section shows a slight linear increase with energy to a maximum cross section of ~ 3.8E-7 cm2/device. The device was total dose tested to ~ 50 kRad(Si), during which time permanent increases in device current were observed (from an original 17mA to 24mA at 50 kRad), while the device remained fully functional.

c. MCM516400J60 16 Mbit Motorola DRAM

This device was tested for proton effects only. Tests used a 4 K refresh cycle (65.6 msec). Devices operated with a Vcc of 5V, 17mA. Only lidded samples were tested. The cross

section increases slightly with energy to a maximum cross section of ~ 1.5E-6 cm2/device. This device has the same die as the Toshiba TC5117400FT-70, and the results are very similar.

d. MCM517400J60 16 Mbit Motorola DRAM

This device was tested for proton effects only. Tests used a 2K refresh cycle (32 msec). Devices operated with a Vcc of 5V, 17mA. Only lidded samples were tested. The test results were very similar to the Motorola MCM516400J60.

e. MT4CM4B1DW 16 Mbit Micron DRAM

Tests used a 2K refresh cycle (32 msec). Devices operated with a Vcc of 5V, 7mA. Latchup current was set at 80mA. The SEU LETth for this device is < 1.41. The SEL LETth lies between 12 - 26.6 with a maximum cross section > 2E-4 cm2/device.

f. TC5117400FT-70 16 Mbit Toshiba DRAM

This device was tested for both heavy ion and proton effects. Devices used a Vcc of 5V, 17mA. Latchup current was set at 90mA. Cross section showed a slight linear increase with energy and a maximum cross section ~ 1.8E-6 cm2/device. The device was total dose tested to ~ 100 kRad(Si) and although permanent increases in device current were observed (from an original 18mA to 19mA at 100 kRad), the device remained fully functional.

Figure 4 displays device SEU and SEL cross sections for several DRAMs tested.

4. 70324L Dual Port RAM

A single sample of this device was tested by NRL using a custom PC-based test setup. No SEL was seen at the highest tested LET (90), with a fluence of 5E7 particles/cm2. The device, however, appears fairly sensitive to SEUs.

5. 70V25 16 bit Dual Port SRAM

This device was tested in two modes:

static - device was written to prior to irradiation and read after irradiation

dynamic - device was written to/read from simultaneously during irradiation

The device was tested with four patterns: all 1s, all 0s, checkerboard, and toggle (dynamic mode only). For the toggle pattern, the input was AC (as opposed to the other patterns in steady state), changing with the clock cycle.

Though the static mode shows a slightly higher cross section, both modes displayed a similar SEU LETth of <3.46 with a maximum cross section of 5E-7 cm2/bit. The variance between static mode results and dynamic mode is partially due to multiple bit upsets per word in static mode, caused by the longer dwell time. No pattern dependency exists for static mode. No

latchup was seen for LETs up to 80. An equilibrium test was performed on the device in support of work by NRL. More information concerning this theory is available from article by Weatherford, et al.[3]

G. FIFOs

1. 7201T 512x9 Split Epi FIFOs

These devices were tested using an all 1s pattern in Read/Write mode at a 50% duty cycle, at a frequency of 1 MHz. An SEU was defined as a noncompare in the data read. Normal operating current was 13mA, with monitoring for latchup conditions (maximum current 28mA). The vendor provided special samples with varying epi thickness, each of which showed distinct SEE characteristics:

12m This device experienced SEL at initial LET of 26.6
10m This device experienced SEL at initial LET of 26.6
8m This device had an SEL LETth between 50 - 60
6m Device SEU LETth was < 3.36 with ssat ~ 5E-3
cm2/device. SEL LETth was > 80 with ssat < 1E-6 cm2/device.

The 6m device was also tested for proton effects, and were not easily upset by protons. During total dose testing, permanent significant increases in device current occurred (from an original 12mA to 27mA at 108 kRad), while the devices remained fully functional to > 100 kRad(Si).

Device SEU and SEL cross sections are displayed in Figure 5. Further information concerning testing is available from LaBel, et.al. [4]

2. 7203ERP 9x2048 FIFO

The devices were tested in dynamic mode (DUT being Write/Read continuously) at a 1 MHz frequency. Device Vcc was 5V, 13mA, with a latchup current of 30mA. Testing was performed using an all 1s or an all 0s pattern. No statistical difference was seen between the two test patterns. An error was defined as a non-compare between output data values and expected data values on a bit basis. The SEU LETth is between 8 and 11.6. Due to the onset of SEL, no ssat was determined. The SEL LETth is 35. An additional error condition was also observed: large bursts of output errors were observed, most likely due to SEU hits to control areas of the DUT. This condition has an LETth of 20.

3. 7203L40DB 9x2048k FIFO

SEUs were defined as noncompares between DUT output and an expected pattern. Test circuitry ran at 20 MHz, using a 5V supply with an operating current of 13mA. Latchup current was set at 120mA. The SEU LETth was ~ 3.4 with a maximum ssat of 5.5E-3 cm2/device. The SEL LETth was between 15 - 22. During irradiation, regular current fluctuations (ñ1mA) were observed.

4. 7204 9x4096 FIFO

The devices were tested in dynamic mode (DUT being Write/Read continuously), at a 1 MHz frequency. Vcc was 5V, 13mA with latchup current set at 30mA. Testing was performed using an all 1s or an all 0s pattern. No statistical difference was seen between the two test patterns. An error was defined as a non-compare between output data values and expected data values on a bit basis. The SEU LETth is between 8 and 11.6. Due to the onset of SEL, no cross section was determined. The SEL LETth is 16.

H. Microprocessors & Peripherals [5]

1. 80386 Microprocessor

The 80386, 80387, and 82380 were all tested using a single-board computer. Device was exercised using a software routine which performs addressing, memory reads and writes, and other operations. External clock speed was 16 MHZ. Failure of the device to write to a test address, incorrect data, or device lock-up was counted as an SEU. If lockup occurred, the test run was halted, and a reset was issued to the device. Figure 6 displays SEU and SEL device cross sections for 80386 tests.

a. MG80386-20/B

The SEU LETth is ~ 3.38. Traditional SEL (Icc > maximum for the device) was not seen on any test run. However, microlatch, a self-limiting latchup localized to an area of the device, was observed. With microlatch, Icc < the maximum for the device, but the device requires a power reset to reboot. The LETth for microlatch was between 37.1 and 59.9.

b. 80386DX-25

This device was tested for SEL only. Microlatch threshold was between LET 29 and 37.8. Devices were tested at both 5V and 5.25V.

2. MG80387-20/B Math Coprocessor

The 80387 test software was continually performing mathematical operations and checking for incorrect calculations. Incorrect data or device lock-up was counted as an SEU. If lockup occurred, the test run was halted, and a reset was issued to the device. SEU LETth for the 80387 was 3.38. A stuck bit was seen twice during the test, but was cleared both times by a soft reset. Lockup was first observed at an LET of 26.2. LETth for traditional SEL was between 37.1 and 59.9. Microlatch was not observed.

3. 82380 Integrated Peripheral

The 82380 test software was continually performing memory accesses and transfers. Incorrect or incomplete accesses or data, unexpected interrupts, and device lockup were all counted as SEUs. If lockup occurred, the test run was halted, and a reset was issued to the device.

a. 82380-20/B

Device SEUs were seen at the lowest LET tested of 3.38.Traditional SEL threshold was between 12.2 and 26.2. The 82380 also experienced possible microlatch conditions as well.

b. 82380-16

This device was tested for SEL only. Traditional latchup was observed at the lowest LET tested of 12. A dwell test was performed, allowing the device to operate for two minutes at a higher SEL current (2850 mA). The 82380 recovered fully, following a power reset.

The 82380 experienced several unusual effects. In several tests, the operating current jumped above device rated limits, but the condition was cleared completely by a soft reset; power reset was not required, so the event was not SEL. In another test, following SEL, the operating current decreased (by ~20 mA in 2 minutes) of its own accord.

4. 80486 Microprocessor

During irradiation, the 80486 was exercised using one of several software routines (System test, paging, coprocessor, external memory access, interrupts, or software performance). Tests were run both with and without cache. Clock speed was 25 MHz (50 MHz internal to the DX2 device). A failure of the device to write to a test address, or lockup, was defined as an SEU. A watchdog timer allowed the device 425 msec to complete the write before issuing a reset. Figure 7 displays 80486 SEU and SEL device cross sections.

a. 80486DX-33

With cache enabled, SEUs were seen at the lowest tested LET of 3.53; the LETth appears to be ~ 3. With cache disabled, SEUs were not seen at the lowest LET tested of 3.53; the LETth is between 3.83 and 8.27, and appears to be around 5-6. In general, the more "cache-intensive" programs showed a higher SEU sensitivity. This device saw traditional destructive single events (Icc > than maximum specified for the device) starting at an LET of 20. Two (of two) samples of this device failed after occurrence of SEL.

b. 486DX2-66

SEUs were not seen at the lowest LET tested of 3.53, either with or without cache enabled. The SEU LETth is between 3.83 and 8.27 and appears to be ~ 5-6 in either case. This device saw a mix of microlatch and traditional SEL conditions, starting at an LET of 59.6. It should be noted that only one sample saw SEL at an LET of 59.6, and not all runs with LET > 59.6 saw SEL; the other two samples did not see SEL until an LET >80. No device failures were seen post any SEL event. Total dose exposure was near 20 kRad(Si) for these samples.

More information concerning the testing of the 80486 and the 80386 set is available from Moran,et. al. [5].

I. Other

1. 49C460 EDAC controller

Vcc for this device was 5V, 4mA with latchup current set at 10mA. The device was tested in normal operational mode (memory scrub) at a frequency of 1 MHz. The test pattern used was a checkerboard with one bit error (either 1-to-0 or 0-to-1) inserted. The operation flowed as follows:

- data always has a single bit error
- DUT corrects error
- single bit error line is active, multiple bit error line is inactive
- syndrome is formed

Four typical error conditions were monitored during testing, plus a "special condition" and SEL. The standard error conditions were: data errors, syndrome errors, single bit error detection fail, and multiple bit errors in a word. The special condition was discovered during testing: Icc dropped to 1mA with continuous errors on all standard error lines. These errors continued even after the beam was stopped until a power reset was issued to the device. An SEU to the control region of the DUT is suspected, causing it to switch modes (possibly to a diagnostic mode).

The LETth for the device is between 20-25, based on curve fitting. Control errors were seen sporadically starting with an LET of 26.6, but occurred infrequently enough to hinder statistical data collection for control error cross section. No sign of SEL was seen up to the highest LET tested (80).

2. 74FCT163374 Dual 8 bit Register

This device was tested by loading and verifying a checkerboard pattern at a speed of 1 MHz. An SEU was defined as a noncompare during pattern verification. The device was operated at a Vcc of 5V, 1mA.

The SEU LETth was found to be ~ 20. However, the SEL LETth was ~ 25, with a maximum ssat > 5E-4 cm2/device.

3. 74FCT163245 16 bit Bidirectional Transceiver

This device was tested by loading a checkerboard pattern to the transmitter (side A) and verifying the output at the receiver (side B) at a speed of 1 MHz. An SEU was defined as a noncompare during pattern verification. The device was operated at 5V with a 1mA operating current.

No SEUs were seen for LETs < 25.2. The SEL LETth was ~ 25.2 with a maximum cross section > 5.0E-4 cm2/device.

4. HR2340 Test Metal Chip

The HR2340 is a sea of transistors gate array, based on the RICMOS IV process. This device

was tested in support of the MONGOOSE III program, a commercially-compatible R3000-based processor. There are many functions in this test chip of which, for SEE purposes, we tested the following:

Test chip areas: (soft latch design)	register type	# of stages or bits
	JK	150
	D	200
	RS	150

Test chip areas: (RH design)	32x23 asynch RAM, 1Kx1 synch RAM

A custom test board used an 8051 microcontroller along with the DUTs and support logic on a PCB. This allowed a low-noise test setup, providing reliable results. Test results for soft latch areas (Xsections are per flip-flop):

Mode, Pattern, Vcc	LETth, MeV*cm2/mg	cross section, cm2
Dynamic, Mixed, 4.5V	~ 14	2E-6
Dynamic, Mixed, 5V	16	2E-6
Dynamic, All 0s, 5V	16	1.2E-6
Dynamic, All 1's, 5V	16	1.2E-6
Static Mixed, 5V	~ 19	8.4E-7

Test conditions:	Temperature 25 deg C
	Vcc for SEU 5V and 4.5 V
	Vcc for SEL 5.5V

Test modes:	Static	device pre-loaded, then irradiated, then checked for errors post-beam
	Dynamic	continuous Read/Write at a 1 MHz frequency

Test patterns:	all 0s, all 1s, and mixed 0s and 1s

The soft latch areas are approximately 10-25% more sensitive using a mixed test pattern than an all 1s or 0s pattern.

Figure 8 displays HR2340 SEU cross sections per flip-flop.

IV. SUMMARY

We typically divide SEE test results into the following four categories:

Category 1 Recommended for usage in all spaceflight applications
Category 2 Recommended for usage in spaceflight applications, but may require some SEE mitigation techniques
Category 3 Recommended for usage in some spaceflight applications, but requires extensive SEE mitigation techniques or SEL recovery mode.
Category 4 Not recommended for use in any spaceflight applications.

Table 2 summarizes device recommendations.

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