CLASS 326, ELECTRONIC DIGITAL LOGIC CIRCUITRY

SECTION I - CLASS DEFINITION

BASIC SUBJECT MATTER OF CLASS

This is the generic class for electronic digital logic devices, circuitry and subcombinations thereof, wherein non-arithmetical operations are performed upon discrete electrical signals representing a value normally described by numerical digits.

COMBINATION WITH BASIC SUBJECT MATTER INCLUDED IN THIS CLASS:

Included in this class (326) is subject matter relating to:

1. digital circuits which perform basic logic functions such as AND, OR, NAND, NOR, EX-OR, or NOT;

2. decoder, inhibitor, multifunctional, or programmable logic circuits, etc., which perform basic logic functions and are used in an environment that is not related to any particular art provided for by other classes;

3. circuits that are used to control the performance of digital logic circuits, such as accelerating, switching, reliability, transmission integrity, etc.;

4. circuits that are used to control the functioning or to interface logical devices or circuitry, such as driving, clocking, or synchronizing.

SECTION II - NOTES TO THE CLASS DEFINITION

(1) Note. An electronic device is a device in which conduction is principally by the movement of electrons through a vacuum, gas, semiconductor or superconductor. This definition excludes inductors, capacitors, resistors, and similar components which deal primarily with the conduction of large currents of electricity through metals.

(2) Note. Logic is a science dealing with the basic principles and applications of truth tables, Boolean algebra, etc. and is also called symbolic logic which is a mathematical approach to the solution of complex situations by the use of symbols to define basic concepts. The three basic logic symbols are AND, OR, and NOT. When used in Boolean algebra, these symbols are somewhat analogous to addition and multiplication.

(3) Note. Examples of non-arithmetical operations are selecting, searching, sorting, or matching. Half-adder circuits in this class accepting two binary inputs are also considered non-arithmetic.

(4) Note. Discrete signals are discontinuous signals which can only assume a finite number of states.

(5) Note. Numerical digits are symbols that represent a specific quantity or amount of units.

(6) Note. The value described may include a value represented by a pulse repetition rate.

(7) Note. A full adder circuit, which is a half adder circuit with look ahead carry (three binary inputs), is considered arithmetic and is classified elsewhere. See References to Other Classes, below, for an electric digital calculating computer.

SECTION III - LINES WITH OTHER CLASSES AND WITHIN THIS CLASS

COMBINATION WITH BASIC SUBJECT MATTER EXCLUDED FROM THIS CLASS:

The combination of the subject matter of this class and another art environment is generally classified with the art device where the environment is significant by virtue of the claimed relationship. Examples include: Logic devices combined with memory systems; Logic devices in arithmetical calculators; Logic circuits in signal discriminators using coincidence function.

See References to Other Classes for the above art areas and to complete the search for subject matter of Class 326.

DIGITAL LOGIC DEVICES EXCLUDED FROM THIS CLASS:

Some particular types of digital logic devices are not classified in this class (326), such as:

Fluidic logic devices

Saturated non-linear reactor logic circuits

Detailed flip-flops, per se, generally are classified elsewhere; however, a multifunctional or programmable logic having a flip-flop is found in this class (326) and redundant logic having a flip-flop is also found in this class (326). See Subclass References to the Current Class, below.

Pulse counters, pulse dividers, or shift registers are classified elsewhere.

Optical logic gates are excluded from this class.

Laser logic systems are excluded from this class.

Neuron circuits are excluded from this class.

See References to Other Classes for the above art areas and to complete the search for subject matter of Class 326.

SECTION IV - SUBCLASS REFERENCES TO THE CURRENT CLASS

SEE OR SEARCH THIS CLASS, SUBCLASS:

12, for redundant logic having a flip-flop.

37+, for a multifunctional or programmable logic having a flip-flop.

SECTION V - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

102, Ammunition and Explosives, subclass 215 for ignition devices and systems including a logic circuit.

123, Internal-Combustion Engines, subclass 444 having fluidic logic control means.

180, Motor Vehicles, subclass 65.8 for electric power control circuit including an electronic digital logic device.

235, Registers, subclasses 200+ for a fluidic logic device.

250, Radiant Energy, subclass 209, 213, and 214 for logic circuits which control a photocell.

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for non-linear, active solid-state devices, per se, without any significant external electrical circuitry.

307, Electrical Transmission or Interconnection Systems, particularly subclass 404 and 407+ for saturated non-linear reactor logic circuit.

324, Electricity: Measuring and Testing, subclass 73.1 for testing of electrical device parameters in printed circuits.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, especially subclasses 1+ for signal discriminating, comparing, or selecting circuits that use logic circuits; subclasses 23+ for logic circuits in signal discriminators using coincidence function; subclasses 185+ for detailed flip-flops, per se, generally; however, a multifunctional or programmable logic having a flip-flop is found in this class (326), See Lines With Other Classes, above; subclasses 199+ for signal converting, shaping, or generating circuits that use detailed flip-flops; and subclasses 365+ for miscellaneous gating circuits.

329, Demodulators, subclass 303, 309, 310, and 343 for demodulators using logic gate, flip-flop, or digital logic circuitry.

331, Oscillators, subclasses 1+ and digest 3 for an oscillator having logic elements.

332, Modulators, subclasses 101 through 104 for a modulator having a logic element or discrete semiconductor device.

340, Communications: Electrical, subclass 146.2 for digital comparator systems and subclass 14.4 for a crosspoint decoder matrix switch with logic function.

341, Coded Data Generation or Conversion, subclass 134 for analog to or from digital conversion with an integrated injection logic device.

359, Optics: Systems and Elements, subclass 108 for an optical computing device using logic gate.

361, Electricity: Electrical Systems and Devices, subclasses 397+ for printed circuit boards having diverse electrical devices.

365, Static Information Storage and Retrieval, subclass 5 for magnetic bubbles including a logic device; subclass 89 for magnetic shift registers including a logic device; subclass 189.08 for read/write circuits including plural element logic arrangement; and subclass 167 for read/write systems which use a simulating biological cell as a storage element.

365, Static Information Storage and Retrieval, subclass 189.08 for logic devices in combination with memory systems

372, Coherent Light Generators, subclass 8 for a laser logic system.

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclass 73 and 74 for shift register including an input logic circuit; subclass 81 for shift register transfer means with logic circuit; and subclasses 116 and 117 for master-slave transfer means including logic circuit.

438, Semiconductor Device Manufacturing: Process, appropriate subclass for methods of making semiconductor barrier layer-type logic circuits.

439, Electrical Connectors, subclasses 55+ for a printed circuit assembly with detachable connectors.

505, Superconductor Technology: Apparatus, Material, Process, subclass 858 and 859 for cross-reference art collections relating to electrical transmission or interconnection using digital logic circuitry.

706, Data Processing: Artificial Intelligence, subclasses 15+ for neural circuits.

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ for logic devices in arithmetical calculators.

711, Electrical Computers and Digital Processing Systems; Memory, subclasses 100+ for logic devices in combination with memory systems.

714, Error Detection/Correction and Fault Detection/Recovery, subclasses 724+ for testing of information content of a digital logic signal.

SECTION VI - GLOSSARY

DIGITAL SIGNAL

An electrical signal with discrete, well-defined logic levels or states. Digital normally means binary or two-state.

DIGITAL CIRCUIT

A circuit which operates at two or more discrete well-defined logic levels or states, in the manner of a switch, such as either “on” or “off” or “high” or “low” (i.e., high voltage or low voltage).

ELECTRONIC

Pertaining to that branch of science which deals with the motion, emission, and behavior of currents of free electrons, especially in vacuum, gas, or phototubes and special conductors or semiconductors. The term electronic is contrasted with electric, which pertains to the flow of large currents in metal conductors.

ELECTRONIC DEVICE

A device in which conduction is principally by the movement of electrons through a vacuum, gas, or semiconductor. This definition excludes inductors, capacitors, resistors, and similar components.

LOGIC

The science dealing with the basic principles and applications of truth tables, Boolean algebra, etc.

SOLID-STATE

(a) Technology utilizing solid semiconductors in place of vacuum tubes for amplification, rectification, or switching. (b) Pertaining to circuits and components using semiconductors.

SOLID-STATE DEVICE

An electronic device which operates by virtue of the movement of electrons within a solid piece of semiconductor material.

SUBCLASSES

1 SUPERCONDUCTOR (E.G., CRYOGENIC, ETC.):

This subclass is indented under the class definition. Subject matter including one or more logic circuits having at least one element whose electrical resistance becomes essentially zero at a very low temperature (e.g., 30 degrees Kelvin, etc.).

(1) Note. This class includes superconductive devices operating at “low” temperature (i.e., 30 K or lower); however, Class 505 includes superconductive devices operating at “high” temperature (i.e., higher than 30 K).

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 186 for superconductive stable state circuits, subclasses 366+ for superconductive switching circuits,

and subclasses 527+ for miscellaneous superconductive devices.

505, Superconductor Technology: Apparatus, Material, Process, subclass 1 for a superconductive material, process, or apparatus operating above 30 K.

2 Tunneling device:

This subclass is indented under subclass 1. Subject matter including an electronic device whose operation is based on an ability (i.e., quantum mechanical nature) of certain atomic particles to pass through a barrier that they cannot pass over because of a required energy level.

3 Josephson tunneling device:

This subclass is indented under subclass 2. Subject matter including an electronic fast-switching device, known as a Josephson junction device, which permits conduction through a thin dielectric insulating layer by quantum mechanical tunneling.

(1) Note. The operation of a Josephson tunneling device is based on a theoretical consideration, that if two superconductors are brought close enough together, a current will flow across the gap between them. Under certain conditions, a voltage appears across the gap, and a high frequency radiation emanates from the gap.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 367 for Josephson junction gating circuits.

4 Plural devices (e.g., distributive device, etc.):

This subclass is indented under subclass 3. Subject matter including more than one Josephson junction device.

5 Interference device (i.e., SQUID):

This subclass is indented under subclass 3. Subject matter including a device which controls or modulates electrical currents based on the quantum wave properties of a current carrying electrons in solids.

(1) Note. A superconductive interference device is also called a superconductive quantum interference device or SQUID.

(2) Note. A SQUID may obtain the control or modulation of electrical currents by, for example, causing a relative phase displacement between at least two currents flowing through a superconductor and combines these two currents after the phase displacement has been achieved, etc.

6 Function of AND, OR, NAND, NOR, or NOT:

This subclass is indented under subclass 2. Subject matter wherein the logic operations are limited to those defined by the Boolean algebraic operations of AND, OR, NAND, NOR, or NOT.

SEE OR SEARCH THIS CLASS, SUBCLASS:

104+, for functions of AND, OR, NAND, NOR, or NOT in general.

7 Function of AND, OR, NAND, NOR, or NOT:

This subclass is indented under subclass 1. Subject matter wherein the logic operations are limited to those defined by the Boolean algebraic operations of AND, OR, NAND, NOR, or NOT.

SEE OR SEARCH THIS CLASS, SUBCLASS:

6+, for a function of AND, OR, NAND, NOR, or NOT by a superconducting tunneling device.

104+, for functions of AND, OR, NAND, NOR, or NOT in general.

8 SECURITY (E.G., ACCESS OR COPY PREVENTION, ETC.):

This subclass is indented under the class definition. Subject matter including an intentional disabling circuit which conceals or prevents obtaining stored data or designed integrated circuit structure.

(1) Note. In this class (326), the security is performed by disabling or masking the circuit structure, while in Class 380, the

security is performed by encrypting data information.

SEE OR SEARCH THIS CLASS, SUBCLASS:

37, for multifunctional or programmable logic circuitry.

SEE OR SEARCH CLASS:

705, Data Processing: Financial, Business Practice, Management, or Cost/Price Determination, subclass 57 and 58 for preventing access to or copying of stored information in a distributed data file.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclass 200 for generic access locking in digital data processing systems.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 163+ for memory access limiting.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

9 RELIABILITY:

This subclass is indented under the class definition. Subject matter having a device for improving the operational quality of a logic circuit, such that an operational procedure yields the same results on repeated trials.

(1) Note. For increasing the operational reliability, a circuit may include a fault detection, a warning signal indication, or an operational isolation such that a component failure in one channel does not affect the operation of the remaining channel, etc.

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, appropriate subclasses for circuit fault detection and testing, per se.

361, Electricity: Electrical Systems and Devices, appropriate subclasses for a voltage or current responsive fault sensor, which may include semiconductor devices.

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 530+ for error detection/correction or fault/recovery in the performance of arithmetic operations.

714, Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses for subject matter limited to particular transmission loss or recovery of information content (e.g., pulse coded data, etc.).

10 Redundant:

This subclass is indented under subclass 9. Subject matter wherein the logic circuit comprises at least one duplicate logic stage which will assume operation upon failure of an original logic stage.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 526 for miscellaneous redundant circuits.

11 Voter circuit (e.g., majority logic, etc.):

This subclass is indented under subclass 10. Subject matter including a logic level switching circuit having a plurality of inputs which actuate the duplicate logic stage whenever one of the following conditions is obtained (a) More than half, but less than all inputs are "fault" (i.e., majority); (b) More than one, but less than half of all the inputs are "fault" (i.e., minority); or (c) Various predetermined combinations, together or in predetermined sequence, of the inputs are "fault" (i.e., weighted).

SEE OR SEARCH THIS CLASS, SUBCLASS:

35+, for threshold (e.g., majority, etc.) logic in general.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 23 for pulse coincidence discriminating.

12 With flip-flop:

This subclass is indented under subclass 10. Subject matter comprising a logic circuit which has two or more distinct current-conductive

stable states and which toggles from one state to the other in response to an external stimulus.

(1) Note. A flip-flop is the most common memory element in a sequential circuit which requires a storage of previous input information.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 185+ for miscellaneous detailed flip-flop circuits.

13 With field-effect transistor:
This subclass is indented under subclass 10. Subject matter including a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

14 Fail-safe:
This subclass is indented under subclass 9. Subject matter including a device which prevents generating a valid output upon an operational failure of the logic circuitry.

(1) Note. The fail-safe condition can be, for example, an automatic shut down of the logic circuitry or a predetermined, unchanging logic voltage output level.

(2) Note. The fail-safe condition may be actuated, for example, by invalid logic input signals or loss of such signals to the input as well as circuit breakdown or component malfunction which traverses the desired logic action.

15 Parasitic prevention in integrated circuit structure:
This subclass is indented under subclass 9. Subject matter wherein the logic device is part of a monolithic integrated circuit, and is intended to prevent an unwanted interaction between circuit components in the monolithic integrated circuit.

(1) Note. A monolithic integrated circuit is a device in which all components are fabricated on a single chip of silicon. Interconnections among components are provided by means of metallization patterns on the surface of the chip structure, and the individual parts are not separable from the complete circuit. External connecting wires are taken out to terminal pins or leads.

16 WITH TEST FACILITATING FEATURE:
This subclass is indented under the class definition. Subject matter wherein the logic circuit includes a specific circuit or device to enable a testing function to be performed (e.g., a bypass circuit that connects a signal input directly to an output, thus bypassing the logic circuit for a testing purpose, etc.).

(1) Note. This subclass comprises the testing facilitation of digital logic circuits; however, when the information content of a digital logic signal is involved, classification is elsewhere, see SEE OR SEARCH CLASS, below.

(2) Note. Class 324 is the residual class for any test that involves the testing of electrical device parameters.

SEE OR SEARCH THIS CLASS, SUBCLASS:
37, for multifunctional or programmable logic circuitry.

SEE OR SEARCH CLASS:
324, Electricity: Measuring and Testing, subclasses 73.1+ for automatic sequential testing of electrical parameters.
714, Error Detection/Correction and Fault Detection/Recovery, subclasses 724+ for testing of information content of a digital logic signal.

17 ACCELERATING SWITCHING:
This subclass is indented under the class definition. Subject matter including a circuit to minimize the time delay at the turn-on or turn-off period of the switch, therefore increasing the switching speed.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 374+ for gating or switching acceleration in general.

18 Bipolar transistor:
This subclass is indented under subclass 17. Subject matter including a semiconductor device of the type having at least three electrodes (emitter, base, and collector), two potential barriers and having a controlled current flow of both majority and minority carriers (i.e., holes and electrons).

(1) Note. A conventional bipolar transistor has three electrodes which include npn or pnp type materials (in the npn type, current flows from a collector terminal to an emitter terminal and in the pnp type transistor, current flows from an emitter terminal to a collector terminal).

19 With Schottky device:
This subclass is indented under subclass 18. Subject matter including a semiconductor device which operates on the principle of injecting very highly concentrated (i.e., "hot") majority carriers across a potential difference barrier which is formed by the junction of a metal layer deposited on a lightly doped semiconductor crystal.

20 Complementary transistors:
This subclass is indented under subclass 19. Subject matter including at least two bipolar transistors of opposite conductivity types (i.e., npn and pnp).

21 SIGNAL SENSITIVITY OR TRANSMISSION INTEGRITY:
This subclass is indented under the class definition. Subject matter including a device to improve the reception of input signals at the logic circuit, or a device to maintain without distortion the logic signals produced at either (a) an output for coupling or interfacing to another stage or stages or (b) an intermediate location of the logic circuit to preclude signal or transmission deterioration (e.g., by power dissipation or by reflection, etc.).

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 379+ for signal transmission integrity or spurious noise override in a switching circuit.

22 Input noise margin enhancement:
This subclass is indented under subclass 21. Subject matter having a circuit to reduce the possibility of switching due to noise input instead of signal input.

(1) Note. An example of reducing noise in the time domain is using a low pass filter at the input to filter out high frequency noise.

(2) Note. An example of reducing noise in the amplitude domain is using a Schmitt trigger which uses a feedback mechanism to eliminate noise.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 72+ for an input signal compared to reference derived therefrom, subclasses 74+ for an input sig-

nal compared to plural fixed references, and subclasses 205+ for miscellaneous hysteresis circuits (including a Schmitt trigger).

23 With field-effect transistor:
This subclass is indented under subclass 22. Subject matter including a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

24 Complementary FET's:
This subclass is indented under subclass 23. Subject matter including at least a unit of two field-effect transistor elements connected in series with their gate terminals tied together, each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel).

25 Depletion or enhancement:
This subclass is indented under subclass 23. Subject matter wherein the logic circuit includes a depletion type which has its channel conductivity on for a zero or a negative gate-source voltage, or an enhancement type which is normally off with a zero or a negative applied gate-source voltage.

26 Output switching noise reduction:
This subclass is indented under subclass 21. Subject matter having a circuit to reduce noise in a power supply line which is a function of parasitic inductance and the switching current.

27 With field-effect transistor:
This subclass is indented under subclass 26. Subject matter including a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

28 With clocking:
This subclass is indented under subclass 27. Subject matter wherein the logic circuit is responsive to a predetermined time-related signal or a periodic signal in addition to an input logic signal.

SEE OR SEARCH THIS CLASS, SUBCLASS:
93+, for clocking or synchronizing of logic stages or gates in general.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems subclasses 291+ for miscellaneous clock generating circuits.

29 Pulse shaping (e.g., squaring, etc.):
This subclass is indented under subclass 21. Subject matter including a circuit to alter the waveform of an output pulse signal, for example, steepening the edges of a pulse.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 100+ for miscellaneous signal converting or shaping.

30 Bus or line termination (e.g., clamping, impedance matching, etc.):
This subclass is indented under subclass 21. Subject matter having a circuit to preclude signal or transmission deterioration by (a) using an impedance element to eliminate the reflective wave energy caused by impedance differences between the network and a connected circuit or (b) using a diode circuit to clamp or to clip the reflective wave riding on the top of an incident wave.

31 Signal level or switching threshold stabilization:
This subclass is indented under subclass 21. Subject matter having a circuit to keep relatively constant the DC output signal levels, or the DC switching voltage levels.

32 Temperature compensation:
This subclass is indented under subclass 31. Subject matter wherein the output signal levels or the switching threshold levels are kept relatively constant in an environment having temperature changes.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 513 for miscellaneous temperature compensation.

33 Bias or power supply level stabilization:
This subclass is indented under subclass 31. Subject matter wherein the output signal levels or the switching threshold levels are compensated for fluctuations in voltage or current supply.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 538+ for miscellaneous bias stabilization circuits.

34 With field-effect transistor:
This subclass is indented under subclass 31. Subject matter including a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel or electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carri-

ers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

35 THRESHOLD (E.G., MAJORITY, MINORITY, OR WEIGHTED INPUTS, ETC.):
This subclass is indented under the class definition. Subject matter including a logic level switching circuit which has a plurality of inputs which actuate the output to switch to one of at least two logic levels whenever one of the following conditions is obtained: (a) More than half, but less than all of the inputs are "on" (i.e., majority); (b) More than one, but less than half of all the inputs are "on" (i.e., minority); or (c) Various predetermined combinations, together or in predetermined sequence, of the inputs are "on" (i.e., weighted).

SEE OR SEARCH THIS CLASS, SUBCLASS:
11, for redundant logic in which a duplicate logic stage is actuated in response to a fault condition determined by a voter circuit.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 50+ for signal amplitude comparators which utilize at least one threshold.

36 With field-effect transistor:
This subclass is indented under subclass 35. Subject matter including a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel or electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

37 MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.):
This subclass is indented under the class definition. Subject matter including (a) a logic circuit capable of either producing different logic function operations from the same logic element or providing a particular, selected (i.e., programmed) logic operation from plural logic elements (e.g., an array, etc.) or (b) details related to the actual setting or programming of the desired logic functions in such a logic circuit.

(1) Note. A multifunctional logic element is, for example, a single element capable of being changed by a control signal from an "AND" to a "NOT" logic function.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, appropriate subclass for electromagnetic storage systems, and subclasses 185.01+ for floating gate memory storage (e.g., flash memory).

38 Having details of setting or programming of interconnections or logic functions:
This subclass is indented under subclass 37. Subject matter which includes specific procedures which establish the desired overall logic circuit operation.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 128+ and 598+ for methods of selectively interconnecting semiconductor barrier layer-type device arrays.

39 Array (e.g., PLA, PAL, PLD, etc.):
This subclass is indented under subclass 37. Subject matter having a group of many similar logic elements connected in series or in parallel (row or column) to form a matrix of two or three dimensions wherein the interconnection between rows or columns can be selectively connected to perform a logical function.

(1) Note. Programmable logic array (PLA), programmable array logic (PAL), or programmable logic device (PLD) are common terms to indicate devices included in this subclass which may be, for example, a combination of a programmable AND array and a programmable OR array, or all other possible combinations of logic functions.

SEE OR SEARCH CLASS:
340, Communications: Electrical, subclasses 825+ for matrix switch with programmable logic circuits.
365, Static Information Storage and Retrieval, subclass 189.08 for read/write circuit including plural elements logic arrangement to handle information signal.
708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 230+ for programming logic circuits with computational means (i.e., arithmetical operation).

40 With flip-flop or sequential device:
This subclass is indented under subclass 39. Subject matter comprising a logic circuit which has two or more distinct current-conductive stable states which toggles from one state to the other in response to an external stimulus or comprising a series connection of such circuits.

(1) Note. A flip-flop is the most common memory element in a sequential circuit which requires storage of previous input information.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 185+ for miscellaneous detailed flip-flop circuits.

41 Significant integrated structure, layout, or layout interconnections:
This subclass is indented under subclass 39. Subject matter including an arrangement of components fabricated in a semiconductor material or integrated circuit chip with significant design emphasis on the topological arrangement of the components and their circuit connectors.

SEE OR SEARCH THIS CLASS, SUBCLASS:
47, for multifunctional or programmable logic circuits with significant integrated structure, layout, or layout interconnections.
101, for logic circuits with significant integrated structure, layout, or layout interconnections, per se.

SEE OR SEARCH CLASS:
257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), subclasses 499+ for specific integrated circuit structure with electrically isolated components.
324, Electricity: Measuring and Testing, subclasses 73.1+ for integrated circuit chip structural arrangements/layouts including monitoring or testing means.
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 564+ for miscellaneous integrated structure, layout, or layout interconnections.
365, Static Information Storage and Retrieval, subclasses 63+ for interconnection arrangements of storage elements and subclasses 94+ for specific integrated circuit layout of read-only memory systems.
716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, subclasses 1 through 18 for the design of circuit systems and integrated circuit structure by data pro-

cessing and computer programming techniques.

42 Bipolar transistor:
This subclass is indented under subclass 39. Subject matter including a semiconductor device of the type having at least three electrodes (emitter, base, and collector), two potential barriers and having a controlled current flow of both majority and minority carriers (i.e., holes and electrons).

(1) Note. A conventional bipolar transistor has three electrodes which include npn or pnp type materials (in the npn type, current flows from a collector terminal to an emitter terminal; and in the pnp type transistor, current flows from an emitter terminal to a collector terminal).

43 Emitter-coupled logic or emitter-follower logic:
This subclass is indented under subclass 42. Subject matter wherein the logic function unit includes either (a) an emitter-coupled arrangement which has the emitters of plural input transistors connected to the emitter and the base of a referenced transistor and commonly grounded (biased) through a current source for performing a nonsaturated, differential logic operation or (b) an emitter-follower arrangement which has a plurality of transistors with the emitters commonly coupled as an output and which produces, as an output, a signal which is in phase with the input logic signals.

44 Field-effect transistor:
This subclass is indented under subclass 39. Subject matter wherein the logic circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

45 Complementary FET's:
This subclass is indented under subclass 44. Subject matter wherein the logic function unit includes at least two field-effect transistor elements connected in series with their gate terminals tied together, each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

46 Sequential (i.e., finite state machine) or with flip-flop:
This subclass is indented under subclass 37. Subject matter comprising a logic circuit which has an output state dependent on a previous input state or which has two or more distinct current-conductive stable states and which toggles from one state to the other in response to an external stimulus.

(1) Note. A flip-flop is the most common memory element in a sequential circuit which requires a storage of previous input information.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 185+ for miscellaneous detailed flip-flop circuits.

47 Significant integrated structure, layout, or layout interconnections:

This subclass is indented under subclass 37. Subject matter including an arrangement of components fabricated in a semiconductor material or integrated circuit chip with significant design emphasis on the topological arrangement of the components and their circuit connectors.

SEE OR SEARCH THIS CLASS, SUBCLASS:

41, for a programmable logic array with significant integrated structure, layout, or layout interconnections.

101, for logic circuits with significant integrated structure, layout, or layout interconnections, per se.

SEE OR SEARCH CLASS:

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), subclasses 499+ for specific integrated circuit structure with electrical isolated components.

324, Electricity: Measuring and Testing, subclasses 73.1+ for integrated circuit chip structural arrangements/layouts including monitoring or testing means.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 564+ for miscellaneous integrated structure, layout, or layout interconnections.

365, Static Information Storage and Retrieval, subclasses 63+ for interconnection arrangements of storage elements and subclasses 94+ for specific integrated circuit layout of read-only memory systems.

716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, subclasses 1 through 18 for the design of circuit systems and integrated circuit structure by data processing and computer programming techniques.

48 Bipolar transistor:

This subclass is indented under subclass 37. Subject matter including a semiconductor device of the type having at least three electrodes (emitter, base, and collector), two potential barriers, and having a controlled current flow of both majority and minority carriers (i.e., holes and electrons).

(1) Note. A conventional bipolar transistor has three electrodes which include npn or pnp type materials (in the npn type, current flows from a collector terminal to an emitter terminal, and in the pnp type transistor, current flows from an emitter terminal to a collector terminal).

49 Field-effect transistor:

This subclass is indented under subclass 37. Subject matter wherein the logic circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

50 Complementary FET's:
This subclass is indented under subclass 49. Subject matter wherein the logic function unit includes at least two field-effect transistor elements connected in series with their gate terminals tied together, each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

51 INHIBITOR:
This subclass is indented under the class definition. Subject matter wherein the logic circuit includes plural input terminals and operates in a manner such that when a digital "on" signal is present at a particular input (known as the inhibit input) to the logic circuit, the logical output from the logic circuit is blocked; and when the inhibit input signal is absent, the logical output from the logic circuit is affected only by signals at the remaining inputs.

SEE OR SEARCH THIS CLASS, SUBCLASS:
104+, for functions of AND, OR, NAND, NOR, or NOT.

52 EXCLUSIVE FUNCTION (E.G., EXCLUSIVE OR, ETC.):
This subclass is indented under the class definition. Subject matter including a logic circuit which produces an output signal which is a function of whether or not the inputs are uniformly identical.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 22 or 23+ for analogous pulse coincidence or anticoincidence detecting or discriminating versus the exclusive type processing of logical signals contained herein.

53 Half-adder or quarter-adder:
This subclass is indented under subclass 52. Subject matter comprising a logic circuit which has two input and two output channels for binary signals, and which operates to produce an output signal (i.e., sum) on one of the output channels when one, but not both, of the input signals is present and an output (i.e., carry) on the other output channel when both of the input signals are present.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 361 for miscellaneous circuits producing the algebraic sum of two or more input voltages.
708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 670+ for the complete arithmetic operation of addition or subtraction, for example, full adders.

54 Exclusive NOR:
This subclass is indented under subclass 52. Subject matter comprising a logic circuit which produces an output signal only if all logic input signals are identical (i.e., all are logically true or all are logically false).

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 23+ for pulse coincidence detecting or discriminating.

55 With field-effect transistor:
This subclass is indented under subclass 52. Subject matter including a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly

doped regions (e.g., n+ type material, etc.) are diffused for forming source/ drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

56 TRI-STATE (I.E., HIGH IMPEDANCE AS THIRD STATE):

This subclass is indented under the class definition. Subject matter wherein the logic device produces any of three conditions on one line: (a) a definite high voltage (logic 1); (b) a definite low voltage (logic 0); or (c) a high impedance or open-circuit condition (i.e., a floating state or undefined state) which permits another part of the circuit to determine whether the line will be high or low.

57 With field-effect transistor:

This subclass is indented under subclass 56. Subject matter wherein the logic circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type material channel and electrons in an n-type material channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/ drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

58 Complementary FET's:

This subclass is indented under subclass 57. Subject matter including at least a unit of two field-effect transistors connected in series with their gate terminals tied together, each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

59 THREE OR MORE ACTIVE LEVELS (E.G., TERNARY, QUATENARY, ETC.):

This subclass is indented under the class definition. Subject matter wherein the logic circuit is responsive to three or more input logic signal states, or it produces three or more different output logic signal states.

SEE OR SEARCH THIS CLASS, SUBCLASS:

56, for tri-state circuits where logic signals are represented by two definite states (high or low), and a high impedance (undefined) state.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems subclasses 185+ for miscellaneous multiple stable state circuits.

60 With conversion (e.g., three level to two level, etc.):

This subclass is indented under subclass 59. Subject matter wherein the logic circuit can be readily modified between varieties having a differing number of active states.

61 INSULATED GATE CHARGE TRANSFER DEVICE:

This subclass is indented under the class definition. Subject matter wherein the logic circuit includes a semiconductor device having plural control electrodes separated from the conducting body by an insulating layer which control the electrostatic potential of the surface of the body in response to timely applied signals to effect a sequential transferring of charge.

(1) Note. Subject matter in this subclass includes a device having plural control electrodes over a conducting body (e.g., charge-coupled devices (CCD), etc.) or plural single control electrode devices connected as a unit (e.g., bucket- brigade devices (BBD), etc.).

SEE OR SEARCH CLASS:
257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes) subclasses 215+ for an FET charge transfer device.
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems subclass 271, 277, and 284 for a miscellaneous signal delay circuit utilizing a charge transfer device.
333, Wave Transmission Lines and Networks, subclass 165 for frequency or time domain filters and delay lines utilizing charge transfer devices.

62 INTERFACE (E.G., CURRENT DRIVE, LEVEL SHIFT, ETC.):
This subclass is indented under the class definition. Subject matter comprising an intermediate circuit or a coupling circuit for providing an operational compatibility between noncommon logic function devices or between a logic function device and its circuit environment.

(1) Note. The noncommon logic function device may be logic devices of different logic families which require a conversion of parameters for operational compatibility.

(2) Note. Drive circuits, including buffer arrangements which convert logic signals between diverse logic devices (e.g., TTL and MOS interfacing), which develop appropriate level signals for broadly addressing electrical memory storage in conjunction with logic decoding arrangements but not specifically disclosed for the purpose of retrieving stored information from a memory are also found here.

(3) Note. Circuits for addressing specific memory storage locations are classified in Class 365, subclasses 230.01+.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 108+ for miscellaneous current drivers, subclasses 318+ for miscellaneous amplitude control in input or output circuits, and subclass 333 for miscellaneous interstage coupling.

63 Logic level shifting (i.e., interface between devices of different logic families):
This subclass is indented under subclass 62. Subject matter comprising an intermediate circuit or a coupling circuit for providing an operational compatibility between devices of different logic families, wherein conversion of parameters is required (e.g., input logic levels, logic signal pulse widths (duty cycle), power supply biasing levels, etc.).

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 333 for miscellaneous amplitude control for interstage coupling.

64 Bi-CMOS:
This subclass is indented under subclass 63. Subject matter wherein the interfacing circuit includes a bipolar transistor and a complementary metal-oxide transistor device.

(1) Note. A bipolar transistor is a semiconductor device having at least three electrodes (emitter, base, and collector), two potential barriers, and wherein a controlled current flow comprising both majority and minority carriers (i.e., holes and electrons).

(2) Note. A CMOS or complementary metal-oxide semiconductor device is a device having a p-channel and an n-channel enhancement type metal-oxide field-effect transistor (MOSFET) which are connected in series across a power supply with their gates tied together.

(3) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.). A MOSFET is either

enhancement-type (normally turned off) or depletion-type (normally turned on).

65 TTL to/from CMOS:
This subclass is indented under subclass 64. Subject matter comprising the interfacing between a transistor-transistor logic device and a complementary metal-oxide semiconductor device.

(1) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in saturation region when the circuit is in either the "on" or "off" condition.

(2) Note. A CMOS or complementary metal-oxide semiconductor device is a device having a p-channel and an n-channel enhancement type metal-oxide field-effect transistor (MOSFET) which are connected in series across a power supply with their gates tied together.

(3) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.). A MOSFET is either enhancement-type (normally turned off) or depletion-type (normally turned on).

66 ECL to/from CMOS:
This subclass is indented under subclass 64. Subject matter comprising the interfacing between an emitter-coupled logic device and a complementary metal-oxide semiconductor device.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A CMOS or complementary metal-oxide semiconductor device is a device having a p-channel and an n-channel enhancement type metal-oxide field-effect transistor (MOSFET) which are connected in series across a power supply with their gates tied together.

(3) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.), A MOSFET is either enhancement-type (normally turned off) or depletion-type (normally turned on).

67 ECL to/from TTL:
This subclass is indented under subclass 64. Subject matter comprising the interfacing between an emitter-coupled logic circuit and a transistor-transistor logic circuit.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in the saturation region when the circuit is in either the "on" or "off" condition.

68 Field-effect transistor (e.g., JFET, MOSFET, etc.):
This subclass is indented under subclass 63. Subject matter wherein the interfacing circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e, holes in a p-type channel and electrons in an n-type channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

69 ECL to/from GaAs FET (e.g., MESFET, etc.):

This subclass is indented under subclass 68. Subject matter comprising the interfacing between an emitter-coupled logic device and a logic device from a family of GaAs material semiconductor field-effect transistor.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A MESFET is a junction field-effect transistor having a gate junction formed by a metallic layer deposited on a lightly doped semiconductor material channel. A MESFET is either made of silicon or gallium-arsenide material; however, GaAs type is most commonly used.

70 TTL to/from MOS:

This subclass is indented under subclass 68. Subject matter comprising the interfacing between a transistor-transistor logic device and a metal-oxide semiconductor device.

(1) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in the saturation region when the circuit is in either the "on" or "off" condition.

(2) Note. A MOS device is a field-effect transistor that has a metallic gate insulated by an oxide layer from the semiconductor channel.

71 TTL to/from CMOS:

This subclass is indented under subclass 70. Subject matter comprising the interfacing between a transistor-transistor logic device and a complementary MOS device.

(1) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in the saturation region when the circuit is in either the "on" or "off" condition.

(2) Note. A CMOS or complementary metal-oxide semiconductor device is a device having a p-channel and an n-channel enhancement type metal-oxide field-effect transistor (MOSFET) which are connected in series across a power supply with their gates tied together.

(3) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2). A MOSFET is either enhancement-type (normally turned off) or depletion-type (normally turned on).

72 Using depletion or enhancement transistors:

This subclass is indented under subclass 71. Subject matter which includes either a depletion type which is normally on for zero or neg-

ative voltage bias or an enhancement type which is normally off with zero or negative voltage bias applied.

73 ECL to/from MOS:
This subclass is indented under subclass 68. Subject matter comprising the interfacing between an emitter-coupled logic device and a complementary MOS device.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A MOS device is a field-effect transistor that has a metallic gate insulated by an oxide layer from the semiconductor channel.

74 ECL to/from TTL:
This subclass is indented under subclass 68. Subject matter comprising the interfacing between an emitter-coupled logic device and a transistor-transistor logic device.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in saturation region when the circuit is in either the "on" or "off" condition.

75 Bipolar transistor:
This subclass is indented under subclass 63. Subject matter wherein the interfacing circuit includes a semiconductor device having at least three electrodes (emitter, base, and collector), two potential barriers, and a controlled current flow of both majority and minority carriers (i.e., holes and electrons).

76 TTL to/from MOS:
This subclass is indented under subclass 75. Subject matter comprising the interfacing between a transistor-transistor logic device and a metal-oxide semiconductor device.

(1) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in saturation region when the circuit is in either the "on" or "off" condition.

(2) Note. A MOS device is a field-effect transistor that has a metallic gate insulated by an oxide layer from the semiconductor channel.

77 ECL to/from MOS:
This subclass is indented under subclass 75. Subject matter comprising the interfacing between an emitter-coupled logic device and a metal-oxide semiconductor device.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A MOS device is a field-effect transistor that has a metallic gate insulated by an oxide layer from the semiconductor channel.

78 ECL to/from TTL:
This subclass is indented under subclass 75. Subject matter comprising the interfacing between an emitter-coupled logic device and a transistor-transistor logic device.

(1) Note. An emitter-coupled logic device is a nonsaturated bipolar logic device in which the emitters of the input logic transistors are coupled to the emitter of a reference transistor.

(2) Note. A transistor-transistor logic device has a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in saturation region when the circuit is in either the "on" or the "off" condition.

79 Integrated Injection Logic (I^2L):

This subclass is indented under subclass 75. Subject matter including either a complementary bipolar transistor pair merged on the same substrate, incorporating; (a) a vertical, inverse mode npn (conversely pnp) transistor, which can have isolated multicollector regions, and (b) a pnp (conversely npn) lateral transistor which serves as a current injector to inject charge current directly into the vertical, inverse mode transistor base; OR a bipolar or FET transistor pair merged on the same substrate wherein; (a) the base of an inverse mode bipolar transistor is injected with charge current by a FET current injector, or (b) the inverse mode transistor is a FET device (e.g., enhancement-mode junction field-effect transistor (enhancement JFET) with bipolar or FET charge current injection.

SEE OR SEARCH THIS CLASS, SUBCLASS:

100, for integrated injection logic circuits, in general.

80 Supply voltage level shifting (i.e., interface between devices of a same logic family with different operating voltage levels):

This subclass is indented under subclass 62. Subject matter comprising a circuit for translating signal data from one device to another device of the same logic family but which operate at differing voltage supply levels.

(1) Note. For example, since read and write voltages for a programmable memory have different levels, it is necessary to provide a circuit which can deal with voltage of two levels and control the supply of the two level voltages to the memory. Whenever such a circuit is claimed with a memory circuit (PROM, EPROM, etc.), classification is in Class 365. If a memory circuit is not claimed, classification is in Class 326.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 333 for miscellaneous interstage coupling (e.g., level shift, etc.).

81 CMOS:

This subclass is indented under subclass 80. Subject matter including a device having a p-channel and an n-channel enhancement type metal-oxide field-effect transistor (MOSFET) which are connected in series across a power supply with their gates tied together.

(1) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2). A MOSFET is either enhancement-type (normally turned-off) or depletion-type (normally turned-on).

82 Current driving (e.g., fan in/out, off chip driving, etc.):

This subclass is indented under subclass 62. Subject matter comprising a current converting circuit to provide an operating compatibility between a logic function device and its circuit environment which may be a higher current load device (off chip driving), or a series connection of plural small loads which result in higher current drawing (fan in/out).

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 108+ for miscellaneous current drivers.

83 Field-effect transistor:

This subclass is indented under subclass 82. Subject matter wherein the current driving circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type channel and electrons in an n-type channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

84 Bi-CMOS:
This subclass is indented under subclass 83. Subject matter wherein the current driving circuit includes both bipolar and complementary metal-oxide semiconductor transistors.

(1) Note. A bipolar transistor is a semiconductor device having at least three electrodes (emitter, base, and collector), two potential barriers, and wherein a controlled current flow comprises both majority and minority carriers (i.e., holes and electrons).

(2) Note. A CMOS or complementary metal-oxide semiconductor device is a device having a p-material channel and an n-material channel enhancement type metal-oxide field-effect transistor (MOSFET) which are connected in series across a power supply with their gates tied together.

(3) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2). A MOSFET is either enhancement-type (normally turned-off) or depletion-type (normally turned-on).

85 Having plural output pull-up or pull-down transistors:
This subclass is indented under subclass 84. Subject matter wherein multiple transistors at the circuit output help maintain the output at logic high (pull-up) or logic low (pull-down) levels as needed.

86 Bus driving:
This subclass is indented under subclass 83. Subject matter including a common path for connecting a number of devices in a digital system.

(1) Note. For example, in a computer system, a data bus line transmits data between a central processing unit and several memories.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 297 for miscellaneous clock bus generating circuits.

87 Having plural output pull-up or pull-down transistors:
This subclass is indented under subclass 83. Subject matter wherein multiple transistors at the circuit output help maintain the output at logic high (pull-up) or logic low (pull-down) levels as needed.

88 With capacitive or inductive bootstrapping:
This subclass is indented under subclass 83. Subject matter wherein the logic circuit includes discrete, capacitive or inductive elements or uses its inherent capacitance or inductance to enhance its operating condition, to achieve full driving switching capabilities in response to logic input signals.

(1) Note. Enhancement of the performance of the logic circuit includes boosting the DC level of the gating signals for one or more semiconductor devices, as well as boosting the attained DC levels of individual circuit nodal locations, usually by, for example, either a feedforward/feed-

back connection or a separate time-related, pulse signal coupled via the boosting element to a particular circuit location.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 589 for generic bootstrapping devices.
330, Amplifiers, subclass 156 for amplifiers which use a bootstrap coupling to the input of the circuit where the input is linearly related to the output.
363, Electric Power Conversion Systems, subclass 59 and 60 for circuits for input/output power level conversions (e.g., voltage multiplication, etc.).

89 Bipolar transistor:
This subclass is indented under subclass 82. Subject matter wherein the current driving circuit includes a semiconductor device having at least three electrodes (emitter, base, and collector), two potential barriers (npn or pnp), and having a controlled current flow of both majority and minority carriers (i.e., holes and electrons).

90 Bus driving:
This subclass is indented under subclass 89. Subject matter including a common path for connecting a number of devices in a digital system.

(1) Note. For example, in a computer system a data bus line transmits data between a central processing unit and several memories.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 297 for miscellaneous clock bus generating circuits.

91 Having plural output pull-up or pull-down transistors:
This subclass is indented under subclass 89. Subject matter wherein multiple transistors at the circuit output help maintain the output at logic high (pull-up) or logic low (pull-down) levels as needed.

92 With capacitive or inductive bootstrapping:
This subclass is indented under subclass 89. Subject matter wherein the logic circuit includes discrete, capacitive, or inductive elements or uses its inherent capacitance or inductance to enhance its operating condition, to achieve full driving switching capabilities in response to logic input signals.

(1) Note. Enhancement of the performance of the logic circuit includes boosting the DC level of the gating signals for one or more semiconductor devices, as well as boosting the attained DC levels of individual circuit nodal locations, usually by, for example, either a feedforward/feedback connection or a separate time-related, pulse signal coupled via the boosting element to a particular circuit location.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 589 for miscellaneous bootstrapping devices.
330, Amplifiers, subclass 156 for amplifiers which use a bootstrap coupling to the input of the circuit where the input is linearly related to the output.
363, Electric Power Conversion Systems, subclass 59 and 60 for circuits for input/output power level conversions (e.g., voltage multiplication, etc.).

93 CLOCKING OR SYNCHRONIZING OF LOGIC STAGES OR GATES:
This subclass is indented under the class definition. Subject matter wherein individual logic stages or gates are responsive to predetermined time-related signals or periodic signals in addition to an input logic signal.

(1) Note. Plural clock signals are usually phase-sequenced for synchronized stage operation.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 41 for the detection of synchronization of frequencies, subclasses 141+ for miscellaneous

synchronizing, and subclasses 291+ for miscellaneous clock generating.

331, Oscillators, subclass 1 for frequency responsive synchronization with logic elements and appropriate subclasses for free-running signal generators.

94 Metastable state prevention:

This subclass is indented under subclass 93. Subject matter including a circuit to prevent the occurrence of an undecided condition at a logic state transition.

(1) Note. A metastable state can occur when a logic voltage output level is between the logic 0 and logic 1 levels.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 198+ for initializing, resetting or protecting a steady state condition of a stable state circuit such as a flip-flop.

95 Field-effect transistor:

This subclass is indented under subclass 93. Subject matter wherein the logic circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type channel and electrons in an n-type channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

96 Two or more clocks (e.g., phase clocking, etc.):

This subclass is indented under subclass 95. Subject matter wherein the logic circuit is responsive to two or more predetermined time-related signals or periodic signals in addition to the input logic signal.

(1) Note. The clocking signals, if more than one, are usually synchronously phase-controlled for sequential activation/deactivation of logic elements or logic control elements (e.g., biasing voltages, etc.).

97 MOSFET:

This subclass is indented under subclass 96. Subject matter includes a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.).

98 MOSFET:

This subclass is indented under subclass 95. Subject matter includes a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.).

99 HAVING LOGIC LEVELS CONVEYED BY SIGNAL FREQUENCY OR PHASE:

This subclass is indented under the class definition. Subject matter wherein the logic circuit receives or produces digital signals which are different in the number of periodic cycles in a unit of time (frequency), or in the relative timing of a signal in relation to another signal (phase).

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 2+ for phase discriminators, subclasses 39+ for frequency discriminators, subclasses 113+ for

frequency control, and subclasses 231+ for phase shift control.

100 INTEGRATED INJECTION LOGIC:

This subclass is indented under the class definition. Subject matter including either a complementary bipolar transistor pair merged on the same substrate, incorporating (a.) a vertical, inverse mode npn (conversely pnp) transistor, which can have isolated multicollector regions, and (b.) a pnp (conversely npn) lateral transistor which serves as a current injector to inject charge current directly into the vertical, inverse mode transistor base; OR a bipolar or FET transistor pair merged on the same substrate wherein; (a.) the base of an inverse mode bipolar transistor is injected with charge current by a FET current injector, or (b.) the inverse mode transistor is a FET device (e.g., enhancement-mode junction field-effect transistor (enhancement JFET, etc.) with bipolar or FET charge current injection.

SEE OR SEARCH THIS CLASS, SUBCLASS:

79, for IIL in logic level interfacing circuits.

101 SIGNIFICANT INTEGRATED STRUCTURE, LAYOUT, OR LAYOUT INTERCONNECTIONS:

This subclass is indented under the class definition. Subject matter including an arrangement of components fabricated in a semiconductor material or integrated circuit chip with significant design emphasis on the topological arrangement of the components and their circuit connectors.

SEE OR SEARCH THIS CLASS, SUBCLASS:

41, for multifunctional or programmable logic circuits with significant integrated structure, layout, or layout interconnections.

47, for multifunctional or programmable logic array circuits with significant integrated structure, layout, or layout interconnections.

SEE OR SEARCH CLASS:

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for specific nonlinear solid-state devices with significant integrated structure.

324, Electricity: Measuring and Testing, subclasses 73+ for integrated circuit chip structural arrangements/layouts including monitoring or testing means.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 564+ for miscellaneous integrated structure, layout, or layout interconnections.

365, Static Information Storage and Retrieval, subclasses 63+ for interconnection arrangement of storage elements; subclasses 94+ for specific integrated circuit layout or read-only memory systems.

438, Semiconductor Device Manufacturing: Process, particularly subclasses 128+ and 598+ for methods of selectively interconnecting semiconductor barrier layer-type device arrays.

716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, subclasses 1 through 18 for the design of circuit systems and integrated circuit structure by data processing and computer programming techniques.

102 Field-effect transistor:

This subclass is indented under subclass 101. Subject matter wherein the logic means includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type channel and electrons in an n-type channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

SEE OR SEARCH THIS CLASS, SUBCLASS:

44, for multifunctional or programmable logic circuits using field-effect transistors.

103 Complementary FET's:

This subclass is indented under subclass 102. Subject matter wherein the logic function unit includes at least two field-effect transistor elements connected in series across a power supply with their gates linked together, each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

SEE OR SEARCH THIS CLASS, SUBCLASS:

50, for multifunctional or programmable logic circuits using complementary FET's.

104 FUNCTION OF AND, OR, NAND, NOR, or NOT:

This subclass is indented under the class definition. Subject matter wherein the logic operations are limited to those defined by the Boolean algebraic operations of AND, OR, NAND, NOR, or NOT.

(1) Note. Miscellaneous electron space discharge systems which perform the logic functions of this subclass are classified here or in the appropriate indented subclass.

(2) Note. For the "exclusive" logic functions, search this class, subclasses 52+.

(3) Note. Multifunctional logic elements where, for example, a single element is capable of being changed from an "AND" to a "NOT" logic function, are classified in this class, subclasses 37+.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 23+ for pulse coincidence discriminators or detectors.

365, Static Information Storage and Retrieval, appropriate subclass for electromagnetic storage systems, and subclasses 185.01+ for floating gate memory storage (e.g., flash memory).

105 Decoding:

This subclass is indented under subclass 104. Subject matter wherein logic gates are selectively responsive to particular binary combinations of logic signals to provide a binary output command signal.

(1) Note. Usually all the outputs of the plurality of gates except the selected logic gate remain at a particular binary level.

SEE OR SEARCH CLASS:

340, Communications: Electrical, subclasses 825+ for selective systems which may be code responsive.

341, Coded Data Generation or Conversion, subclasses 50+ for converting signals encoded in a first code to signals encoded in a second code.

365, Static Information Storage and Retrieval, subclasses 230.06+ for storage systems addressing by information signals especially in the selection of specific memory locations.

106 With field-effect transistor:
This subclass is indented under subclass 105. Subject matter wherein the logic circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type channel and electrons in an n-type channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material, etc.), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material, etc.) to form a pn junction, and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material, etc.) into which two highly doped regions (e.g., n+ type material, etc.) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2, etc.) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

107 Depletion or enhancement:
This subclass is indented under subclass 106. Subject matter wherein the decoder includes either a depletion type which has channel conductivity on for zero or negative gate-source voltage or an enhancement type which is normally off with zero or negative gate source voltage bias applied.

108 CMOS:
This subclass is indented under subclass 106. Subject matter wherein the logic function unit includes at least two metal-oxide field-effect transistors (MOSFET), each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

(1) Note. A MOSFET is a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.).

(2) Note. Opposite channel conductivity type, as used above, characterizes the induced channel majority carrier conduction (i.e., holes for p-channel and electrons for n-channel).

109 Bipolar and FET:
This subclass is indented under subclass 104. Subject matter wherein the logic circuit includes two types of transistors: (a) a bipolar transistor having at least three electrodes (emitter, base, and collector), two potential barriers, and wherein a controlled current flow comprises both majority and minority carriers (i.e., holes and electrons) and (b) a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type channel and electrons in an n-type channel).

110 Bi-CMOS:
This subclass is indented under subclass 109. Subject matter wherein the logic function circuit comprises a bipolar transistor and a unit of two enhancement type metal-oxide field-effect transistor elements connected in series with their gates tied together, each element has a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

111 Space discharge device (e.g., vacuum tube, etc.):
This subclass is indented under subclass 104. Subject matter including an electronic device having an electrical current flow of charged particles (e.g., ions or electrons) in an area between two spaced electrodes and with at

least part of that area being constituted by a gas, vapor, or vacuum.

112 Field-effect transistor (e.g., JFET, etc.)
This subclass is indented under subclass 104. Subject matter wherein the logic circuit includes a unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electrical field applied to the semiconductor from a control electrode (gate).

(1) Note. In a unipolar transistor, the source to drain current involves only one type of charge carrier (i.e., holes in a p-type channel and electrons in an n-type channel).

(2) Note. Two types of FET structures are prevalent: (a) an all-junction device, known as a junction FET or JFET characterized by having heavily doped impurity regions of one type (e.g., p-type material), known as gate regions, on both sides of a second type semiconductor bar (e.g., n+ type material) to form a pn junction, and (b) a device such as a MOSFET/IGFET, consisting of a lightly doped substrate (e.g., p-type material) into which two highly doped regions (e.g., n+ type material) are diffused for forming source/drain regions with the area therebetween becoming the channel for current carriers (i.e., holes or electrons) and with a layer of insulating material (e.g., SiO_2, etc.) grown over the channel surface for separating the channel from a control (i.e., gate) electrode.

113 Pass transistor logic or transmission gate logic:
This subclass is indented under subclass 112. Subject matter wherein a field-effect transistor performs a logic function using power from two signal inputs which feed through a gate and a source (or drain) terminals with an output taken at the drain (or source) terminal which is an AND function of the two signal inputs.

(1) Note. The use of pass transistor logic saves power and reduces transistor numbers, but lowers the operational speed.

(2) Note. Transmission gate logic includes at least two field-effect transistor elements used as pass transistors, each having a channel of conductivity type opposite that of the other (i.e., complementary FET's).

114 Wired logic (e.g., wired-OR, wired-AND, dotted logic, etc.)
This subclass is indented under subclass 112. Subject matter which includes a logic family having their output gates eliminated simply by wiring the outputs of some basic logic circuits together, the resultant circuit is called wired-OR or wired-AND depending on the type of logic, and the joint output is in turn input to other logic gates for performing additional logic functions.

(1) Note. Wired logic is used in source-coupled logic where source channel outputs are wired together. Special FET gates, such as open-drain gates, can be directly wired together.

(2) Note. Circuits implemented using wired logic save space by reducing devices in number, and increasing operational speed by eliminating some delays due to multiple level gating.

115 Source-coupled logic (e.g., current mode logic (CML), differential current switch logic (DCSL), etc.):
This subclass is indented under subclass 112. Subject matter wherein the logic function unit includes an arrangement in which the source channel of plural input transistors are connected to the source and the gate of a referenced transistor, and are commonly grounded (biased) through a current source for performing a nonsaturated, differential logic operation.

(1) Note. Current mode logic (CML) and differential current switch logic are other state-of-the-art expressions for a source-coupled logic arrangement providing complementary drain output and functioning as NOR/OR circuits.

116 Schottky-gate FET (i.e., MESFET):
This subclass is indented under subclass 112. Subject matter including a junction field-effect transistor which operates on the principle of the injection of very highly concentrated majority carriers across a potential difference barrier which is formed by the junction of a lightly doped semiconductor material and a metal layer deposited thereon.

(1) Note. A MESFET or metal-semiconductor field-effect transistor can be made of silicon or gallium arsenide; however, GaAs type MESFETs are most commonly used.

117 Depletion or enhancement:
This subclass is indented under subclass 116. Subject matter wherein the logic circuit includes either a depletion type which has channel conductivity on for zero or negative gate-source voltage or an enhancement type which is normally off with zero or negative gate-source voltage bias applied.

118 Diode transistor logic:
This subclass is indented under subclass 116. Subject matter wherein diodes are active switching elements responsive to respective input logic signals for providing logical function outputs which control output transistor elements.

119 MOSFET (i.e., metal-oxide semiconductor field-effect transistor):
This subclass is indented under subclass 112. Subject matter includes a field-effect transistor having a metallic gate insulated from the channel by an oxide layer (e.g., SiO_2, etc.).

120 Depletion or enhancement:
This subclass is indented under subclass 119. Subject matter wherein the logic circuit includes either a depletion type which has channel conductivity on for zero or negative gate-source voltage, or an enhancement type which is normally off with zero or negative gate-source voltage bias applied.

121 CMOS:
This subclass is indented under subclass 119. Subject matter wherein the logic function unit includes two enhancement mode metal-oxide semiconductor field-effect transistor elements connected in series with gates tied together, each having a channel of conductivity type opposite that of the other (i.e., P-MOS vs. N-MOS).

122 Complementary FET's:
This subclass is indented under subclass 112. Subject matter wherein the logic function unit includes at least two field-effect transistor elements, each having a channel of conductivity type opposite that of the other (e.g., p-channel vs. n-channel, etc.).

123 With semiconductor diode or negative resistance device:
This subclass is indented under subclass 112. Subject matter wherein the logic function unit includes (a) a semiconductor device having two electrodes (anode and cathode) and a single junction (pn) that allows current to flow in only one direction; or (b) a semiconductor device characterized by an operating current-voltage plot having a portion with a negative slope.

124 Bipolar transistor (e.g., RTL, DCTL, etc.):
This subclass is indented under subclass 104. Subject matter including a semiconductor device of the type having at least three electrodes (emitter, base, and collector), two potential barriers, and wherein a controlled current flow comprises both majority and minority carriers (i.e., holes and electrons).

(1) Note. Among the logic function configurations found in this subclass are (a) resistor-transistor logic (RTL) that has a resistor as an input component coupled to the base of a bipolar transistor; and (b) direct-coupled transistor logic (DCTL) which is a NOR gate type of bipolar logic in which the output of one gate is coupled directly to the input of the succeeding gate.

125 Wired logic or open collector logic (e.g., wired-OR, wired-AND, dotted logic, etc.):
This subclass is indented under subclass 124. Subject matter which includes a logic family having their output gates eliminated simply by wiring the outputs of some basic logic circuits together, the resultant circuit is called wired-OR or wired-AND depending on the type of

logic, and the joint output is in turn input to other logic gates for performing additional logic functions.

(1) Note. Wired logic is widely used in ECL having emitter outputs directly connected. There are also special TTL gates, known as open-collector gates, where collector outputs are directly connected.

126 Emitter-coupled or emitter-follower logic:
This subclass is indented under subclass 124. Subject matter wherein the logic function unit includes either: (a) an emitter-coupled arrangement which has the emitters of plural input transistors connected to the emitter and the base of a referenced transistor and commonly grounded (biased) through a current source for performing a nonsaturated, differential logic operation; or (b) an emitter-follower arrangement which has a plurality of transistors with the emitters commonly coupled as an output and which produces, as an output, a signal which is in phase with the input logic signals.

127 Current mode logic (CML):
This subclass is indented under subclass 126. Subject matter wherein the logic utilizes an emitter-coupled arrangement which provides complementary collector outputs and functions as a NOR/OR circuit.

128 Transistor-transistor logic (TTL):
This subclass is indented under subclass 124. Subject matter wherein the logic function unit includes a forward-biased input transistor which is responsive to an input logic signal at each of its one or more emitters and with its collector being directly coupled to the base of an output transistor.

(1) Note. In TTL, the base-collector junction of the input transistor (usually a multiemitter type) remains forward biased and in the saturation region when the circuit is in either the "on" or "off" condition.

129 Complementary transistor logic (CTL):
This subclass is indented under subclass 128. Subject matter wherein the logic function unit includes transistors of opposite conductivity type (e.g., npn and pnp type, etc.).

130 Diode-transistor logic (DTL):
This subclass is indented under subclass 124. Subject matter wherein diodes are active switching elements responsive to respective input logic signals for providing logical function outputs which control output transistor elements.

131 With metal semiconductor junction diode (e.g., Schottky barrier, etc.):
This subclass is indented under subclass 130. Subject matter wherein the diode transistor logic device includes diodes of the type which operate on the principle of the injection of very highly concentrated (i.e., "hot") majority carriers across a potential difference barrier which is formed by the junction of a lightly doped semiconductor crystal and a metal layer deposited thereon.

132 With negative resistance device (e.g., tunnel diode, etc.):
This subclass is indented under subclass 124. Subject matter wherein the bipolar transistor logic circuit includes a semiconductor device characterized by an operating current-voltage plot having a portion with a negative slope.

(1) Note. Devices such as tunnel diodes, back diodes, or four or more layer diodes, are proper for this subclass, as well as devices which switch on or avalanche as a result of negative resistance conduction induced by increasing an electrical field condition (e.g., IMPATT or GUNN effect elements, etc.).

SEE OR SEARCH THIS CLASS, SUBCLASS:
134, for negative resistance diode logic functions of AND, OR, NAND, NOR, or NOT.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 568+ for miscellaneous negative resistance circuits.

133 Diode:
This subclass is indented under subclass 104. Subject matter including a two electrode (anode and cathode), single junction (pn) semi-

conductor device used as an active switching element responsive to respective input logic signals to perform the logic function.

134 Negative resistance diode (e.g., tunnel, gunn, etc.):

This subclass is indented under subclass 133. Subject matter includes a diode characterized by an operating current-voltage plot having a portion with a negative slope.

(1) Note. Devices such as tunnel diodes, back diodes, or four or more layer diodes are proper for this subclass, as well as devices which switch on or avalanche as a result of negative resistance conduction induced by increasing an electrical field condition (e.g., IMPATT or GUNN effect elements).

SEE OR SEARCH THIS CLASS, SUBCLASS:

132, for a circuit having bipolar transistor and negative resistance diode logic functions of AND, OR, NAND, NOR, or NOT.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 568+ for miscellaneous negative resistance circuits.

135 Negative resistance device:

This subclass is indented under subclass 104. Subject matter which includes a semiconductor device characterized by an operating current-voltage plot having a portion with a negative slope.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 568+ for miscellaneous negative resistance circuits.

136 MISCELLANEOUS:

This subclass is indented under the class definition. Subject matter not provided for in any of the preceding subclasses.

END