Distributed Power for the DFEA2 System

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Table of Contents

Introduction 3
Bulk 48V Supplies 4
Location 5
AC Distribution 6
  Safety Interlocks 7
DC Distribution 8
  Shock Prevention 8
Remote Control and Monitoring 10
Current Density Calculations 11
  Backplane 11
  Bulk Supply to the Backplane 11
  Lug to Power Tap 11
  Power Tap Pin to Backplane 12
  Power Plane 12
  Hard Metric Connector Pin 13
  Voltage Drop and Power Dissipation on the Backplane 13
Local Power Regulation on the DFEA2 boards 15
Environmental Concerns 16
  Bulk 48VDC Power Supplies and Cables 16
  Backplanes and DFEA2 Boards 16
References 17
Revision History 17
Appendix A 18

Introduction

In run 2a two crates of electronics formed the heart of the Central Track Trigger electronics. These two crates contained Digital Front End boards (called DFEAs) and each crate required two low voltage high current power supplies. These power supplies proved to problematic for several reasons:

- The power supply location resulted in long, bulky cables and poor cooling.
- The remote sense feature on the supplies never worked correctly, resulting in poor voltage regulation, oscillation and noise.
- No redundancy, meaning that the loss of one supply would take down an entire crate until an access could be made.

Increasing Tevatron luminosity strained the track finding capability of the original DFEA hardware and it was decided to upgrade these crates for run 2b. The upgrade crates were completely redesigned: new power supplies, new crate controllers, and of course new DFEA boards, appropriately called DFEA2.

Rather than use another low voltage power supply scheme these new crates are powered by a 48VDC system and the low voltage regulation will be done at the board level. (Such systems have been in used in telecom industries for decades.) This "distributed power" architecture solves the problems we encountered with the original DFEA boards:

- The bulk supplies can be relocated to facilitate better airflow.
- The power supply cabling does not carry large currents.
- Remote sense is no longer needed.
- The bulk 48V supplies support N+1 redundancy.

Bulk 48V Supplies

There are several vendors which produce DPS/SSI compliant supplies. I have selected the Shindengen HS-1201 supply [2] for our application.

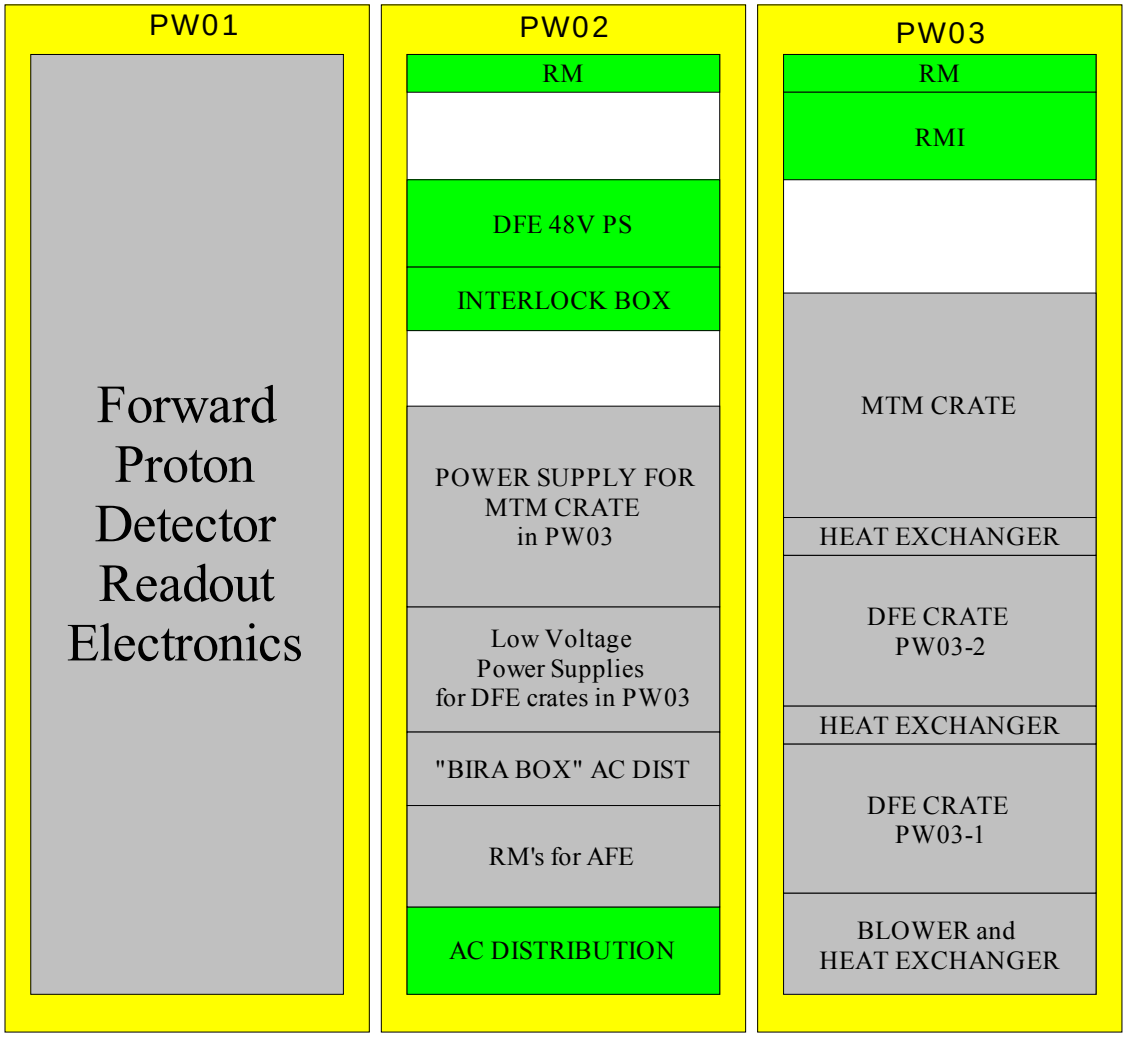
Each HS-1201 supply is rated for 48VDC output at up to 24A. Cooling is achieved through internal fans which vent out of the front of the crate. Over-Voltage, Over-Current, and Thermal protection features are standard in these power supply units.

Three power supply units will be installed in a 3U high rack-mountable chassis:

The power supplies have the AC input and DC output connectors in the back. Since the chassis has mating connectors installed in the back of each bay no tools are needed when swapping out the supplies – just pull the unit out with the ejector handle.

Location

The DFE power supply chassis and AC distribution box are located in PW02, while the rack monitor, rack monitor interface are located in PW03.



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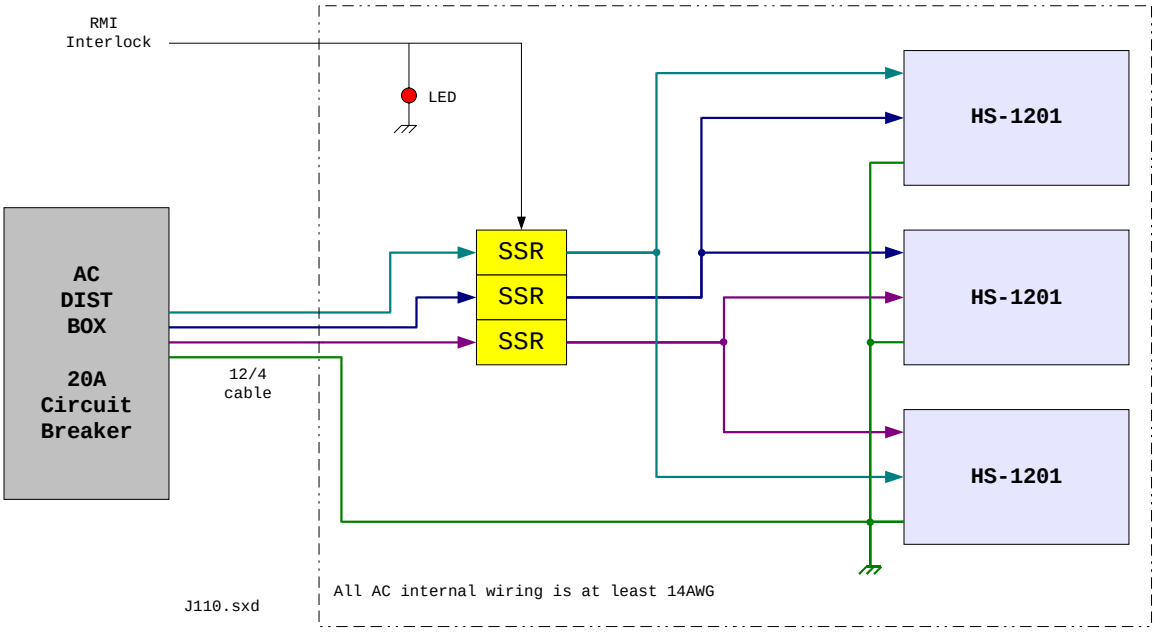
AC Distribution

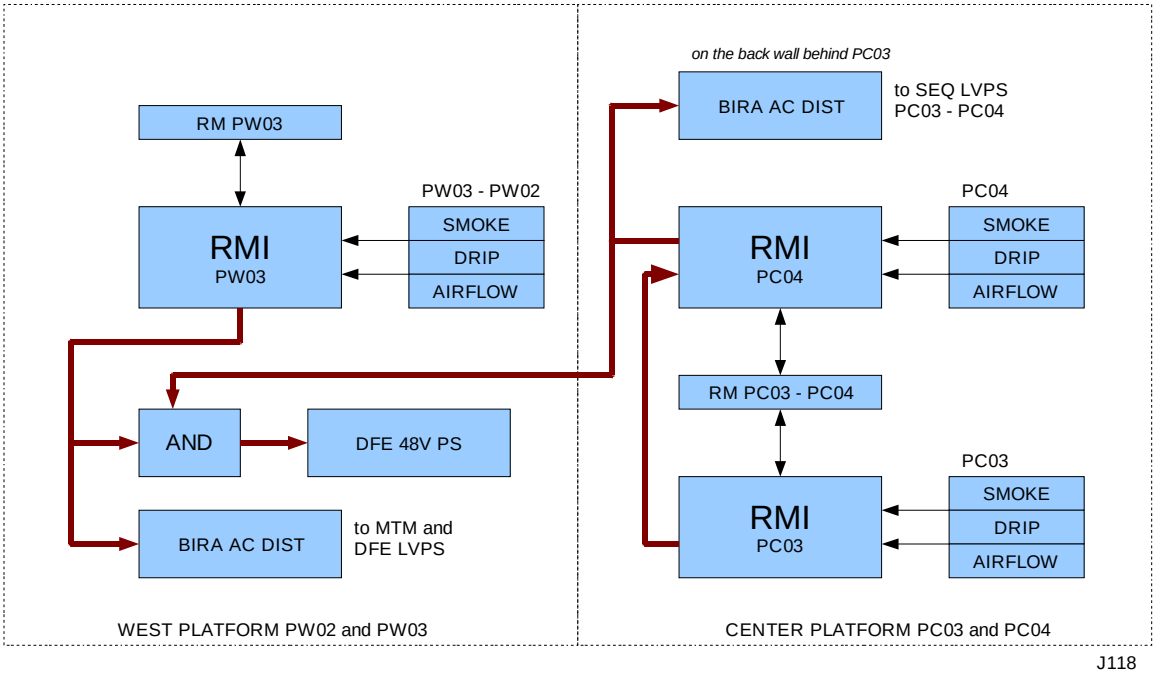
Three power supplies will be wired for 2 phase 208VAC operation, and these three supplies will be connected across three phases as shown below. A three pole 20A circuit breaker is connected in series with a set of solid-state relays (SSRs).



AC power is controlled by a 20A circuit breaker in the distribution box and the solid state relays in the chassis, which are driven by the Rack Monitor Interface.

Safety Interlocks

In this system the crates are in PC03 while the power supplies feeding these crates are located in PW02. Thus the AC power to the DFEA2 48VDC supplies in PW02 must be cut if a fault condition occurs in PC03, PC04, PW02, or PW03. We're set up to monitor airflow, water drips, and smoke detection in all racks. The Rack Monitor Interfaces are chained together as follows:



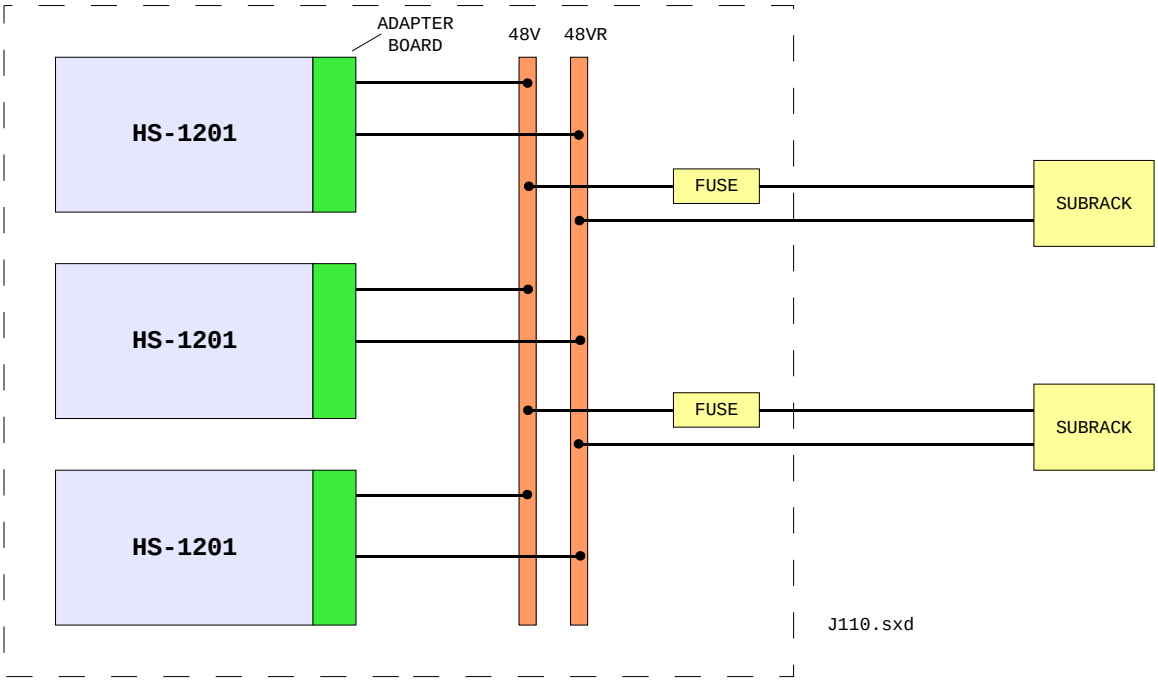
The TTL interlock signal going to the 48VDC supplies is this logical AND of the "Fault Out" TTL interlock signals from the RMI in PW03 and PC03/04. A simple circuit based on relays performs this AND function (see Appendix A for the schematic).

The VESDA system connects to all Rack Monitor Interfaces, but is not shown the diagram above.

DC Distribution

The power supply outputs are floating relative to chassis ground. However, resistors to chassis ground are used to prevent the common mode voltage from wandering.

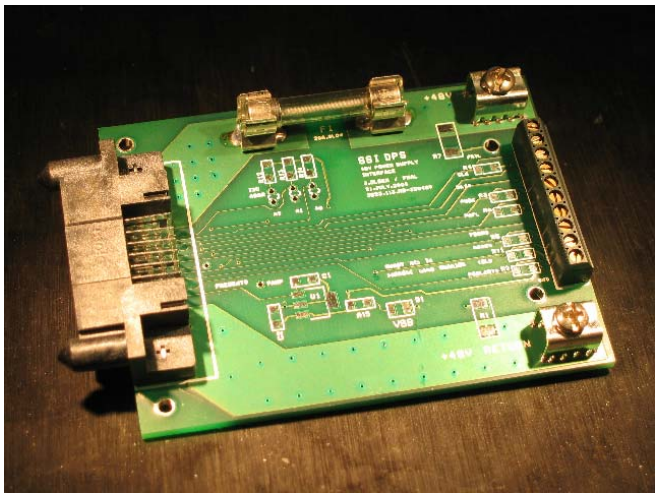
The three 48V terminals are tied together at a small copper busbar inside the chassis; likewise for the 48VR terminals. The bus bars are connected to the crates using 8AWG (90°C insulation or better) and are fused at 20A. The bus bars measure 3/16" x 1" yielding a cross sectional area of 0.187 square inches, or a maximum current rating of 187A. Three HS-1201 supplies running under full load can only deliver 72A maximum.

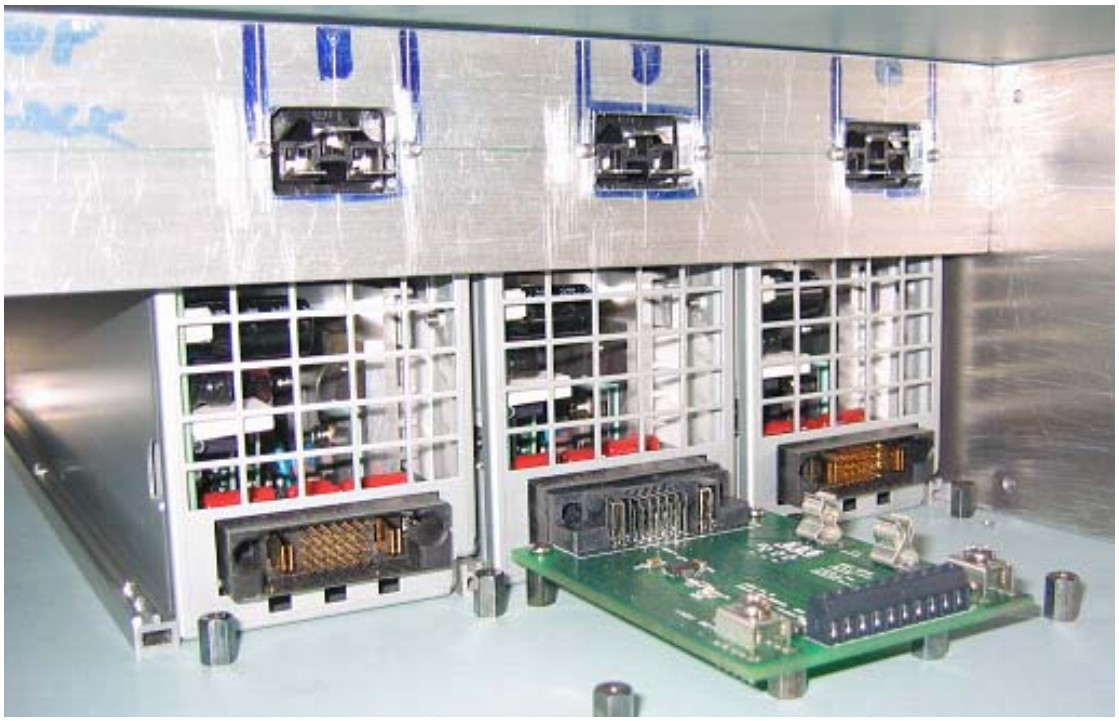


Shock Prevention

All AC and 48V conductors will be shielded with Plexiglas covers or heat shrink tubing. This includes the busbars in the rear of the chassis and the "powerbug" connectors on the backplane.

The output connector (Molex 87607) of the HS-1201 does not allow for direct cable connections, so a small adapter board has been fabricated to break these signals out to Power-Bug style terminals or a terminal block. The 48V and 48VR nets on this board are a minimum of 0.400" wide and 2oz copper was used – these traces are good for 20A with < 10°C temperature rise [3]. A standard 25A 3AG fuse is also used on the 48V connection.





The 48VLS (load-share) control signal is wired common to all supplies to allow for dynamic load sharing between supplies (N+1 redundant operation). Thus any one supply can be hot-swapped without affecting any of the powered crates.

Remote Control and Monitoring

This power supply chassis is connected to the RM with two ribbon cables: one for control and one for status. The bit definitions are:

*** STATUS ***	*** CONTROL ***
15: (not connected)	15: X
14: PSALERT# BAY3	14: X
13: PSALERT# BAY2	13: X
12: PSALERT# BAY1	12: X
11: ACOK# BAY3	11: X
10: ACOK# BAY2	10: X
09: ACOK# BAY1	09: X
08: PRFL BAY3	08: X
07: PRFL BAY2	07: X
06: PRFL BAY1	06: X
05: PWOK BAY3	05: X
04: PWOK BAY2	04: X
03: PWOK BAY1	03: X
02: FAIL BAY3	02: PSON# BAY3
01: FAIL BAY2	01: PSON# BAY2
00: FAIL BAY1	00: PSON# BAY1

When the chassis is viewed from the front BAY1 is on the right.

PSALERT#: Pulled LOW if any supply is approaching its over-temp, over-current, or under/over-voltage limit.

ACOK#: This signal is pulled LOW when the AC input voltage is within specification.

PRFL: Predictive Failure Signal. This signal goes HIGH when the supply has determined when the cooling fans have started to slow down and may soon fail.

PWOK: This signal is asserted HIGH when the outputs are within specification.

FAIL: This signal goes HIGH if the supply has shutdown due to an over-temp, over-current, or under/over-voltage condition.

PSON# the RM must pull this signal LOW to enable the 48V supply outputs.

Supply outputs may be enabled or disabled independently. If a supply trips off (FAIL=1) toggle the corresponding PSON# input 0-1-0 to clear the trip. If the supply trips off again just disable it – the other two supplies will safely handle the load until an access can be made to swap out the faulty supply.

In addition to these status bits, each power supply features a microprocessor interface bus (I2C) that allows an host to read the trip status; input voltage and current; output voltage and current; temperature; fan speeds; and hours of operation. Since this interface is too complex for the RM it's currently not used.

Current Density Calculations

Backplane

The DFE upgrade backplane is a custom 6U monolithic unit with no bus bars. The 48V and 48VR is distributed to the slots through power planes. The following sections calculate the current density from the cables through to the boards.

Bulk Supply to the Backplane

These leads will be fused at 20A at the bulk supply. The power supply leads are 8AWG with 600V insulation rated at 90 degrees C or better.

Lug to Power Tap

Three power taps (ERNI 114194 or equivalent) will be used for the +48V and another three will be used for the +48VRTN. Lugs will attach to the three taps using a small copper bus bar. This bus bar will be 0.125” thick copper and tin plated.

According to the ERNI literature [4], each power tap is rated for 40A @ 20C, and is de-rated to 24A @ 70C, per specification IEC60512 test 5b.

The lug to power tap surface area measures approximately 7x11mm, or $1.2x10^{-2}$ in^2 so assuming 20A is flowing through three power taps, the current density is 560 A/ in^2. A small copper bus bar will be installed between the two power taps to insure that *all three* taps are connected the bulk supply cabling.

Power Tap Pin to Backplane

Each power tap connector has ten press-fit pins. The power taps are pressed into plated through holes in the backplane; they will not be soldered in and thermal relief patterns will not be used. Assuming that the backplane uses 1oz copper (thickness 1.4 mil) for the internal plane layer, the contact area per pin is:

(6.28)(0.5mm)(1.4mil) = $1.7x10^{-4}$ in^2 per pin. If two power taps are used, the total surface area is $3.4x10^{-3}$ in^2. A total of 20A flowing through these three power taps yields a current density of 3921 A/in^2, which exceeds the design guideline.

However, it should be noted that these current densities are present only in a thin cross section and that the metal area available for heat dissipation is much larger than the cross sectional area in which the heat is generated.

If one "unrolls" the cylindrical cross section it becomes equivalent to an internal PCB trace 123 mils wide. A 1oz 125 mil wide internal trace can handle 3A at +10°C temperature rise [3]. In this application only 1A will flow through each pin, resulting in an estimated temperature rise of ~5°C.

Power Plane

The cross sectional area of the 1oz Cu backplane power plane is approximately 9" x 1.4mil = 0.126 in^2, which leads to a maximum current density of 1587 A/in^2, which exceeds the design guideline.

However, if one considers the backplane to be a 9" wide 1oz Cu internal trace, the IPC-D-275 and IPC-2221 specifications [5] can be extrapolated out as follows:

$$Area = [Max\_Current / (k*(temp\_rise^b))]^{1/c}$$
$$Trace\_Width = Area/(Thickness*1.378)$$

For IPC-D-275 internal layers: k = 0.0150, b = 0.5453, c = 0.7349. Setting Max_Current = 30A, temp_rise=1°C, thickness = 1.4mil, the minimum Trace_Width is calculated to be 9215 mils. In other words, under full load this backplane will experience a temperature rise of ~1°C.

Hard Metric Connector Pin

Each slot will be individually fused at 2A. The +48V and +48VRTN are supplied through two pins each. These are Hard Metric (IEC-61076-4-101) pins which have a maximum resistance of 20 mΩ. All pins are press fit into a 0.6mm plated through hole. Thermal reliefs will not be used.

Assuming the backplane is 1oz copper, the plane to through-hole surface area is:

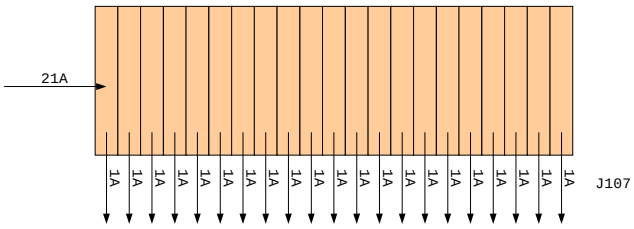
$(6.28)(0.3mm)(1.4mil) = 1.0x10^{-4}$ in^2 per pin.

Assuming that 2A is passing through two plated through holes the maximum current density is 9629 A/ in^2. Again, it should be noted that this is an extremely small cross sectional area, and any heat generated here will dissipate into the solid copper plane.

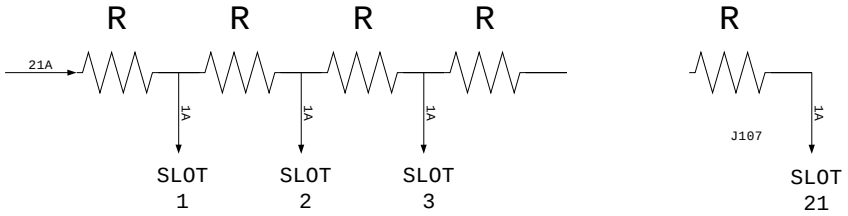
This cylindrical cross section is equivalent to an internal 1oz copper trace 75 mils wide. The IPC-D-275 specification states that such a trace can supply 1.5A with at 10°C temperature rise. In this application each pin can supply a maximum of 1A, so the estimated temperature rise is ~5°C.

Voltage Drop and Power Dissipation on the Backplane

The backplane can be thought of as being a PCB trace 9" wide. Which can be modeled like this:



or in schematic form,



The value of R is calculated as:

$R = \rho * l/a$

Where ρ is the resistivity of copper, 0.6788 μΩ*in; l is the segment length, 0.8", and a is the cross sectional area of the 9" x 0.0014 (1oz Cu) plane = 0.0126 in^2. The value for R is 43 μΩ.

Once the value for R is known, a straightforward spreadsheet calculation will determine the voltage drop and power dissipated in the copper plane:

slot	current (A)	voltage (V)	drop (V)	Power (W)
0	-21	48.000000	0.000000	
1	1	47.999095	0.000905	0.019006
2	1	47.998233	0.000862	0.017239
3	1	47.997414	0.000819	0.015559
4	1	47.996638	0.000776	0.013964
5	1	47.995906	0.000733	0.012455
6	1	47.995216	0.000690	0.011033
7	1	47.994570	0.000646	0.009697
8	1	47.993966	0.000603	0.008447
9	1	47.993406	0.000560	0.007284
10	1	47.992889	0.000517	0.006206
11	1	47.992415	0.000474	0.005215
12	1	47.991984	0.000431	0.004310
13	1	47.991596	0.000388	0.003491
14	1	47.991251	0.000345	0.002758
15	1	47.990949	0.000302	0.002112
16	1	47.990691	0.000259	0.001552
17	1	47.990475	0.000215	0.001077
18	1	47.990303	0.000172	0.000690
19	1	47.990174	0.000129	0.000388
20	1	47.990087	0.000086	0.000172
21	1	47.990044	0.000043	0.000043
		total power (W)		0.143

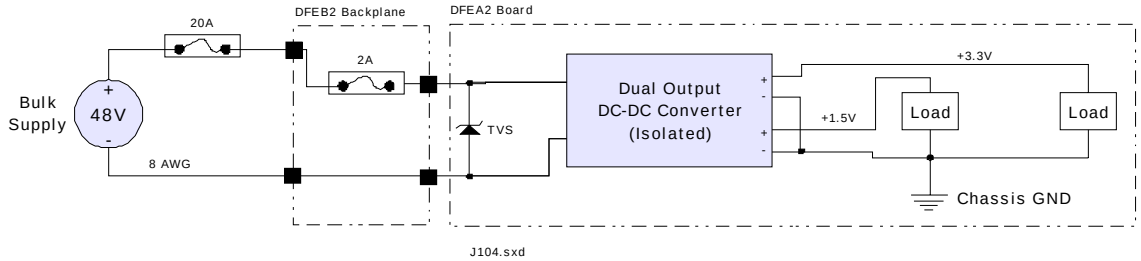
This is in fact the worst case condition: if any slot draws more current, the fuse on the bulk supply will blow; if any slot draws more than 2A, its local fuse will blow.

The total heat generated in the backplane is a function of: resistance in the power planes, resistance of the power taps, and hard metric connector vias. Heat dissipated in the power planes is calculated as ~286mW.

While the current density flowing through the plane/through-hole interface exceeds the 1000A/in^2 specification, it should be noted that this cross section is small and the copper power planes will act as a heat sink. Furthermore, when these cross sectional areas are modeled as traces, the IPC-D-275 specification shows only a small (~5°C) temperature increase in these areas.

Local Power Regulation on the DFEA2 boards

Local power regulation is achieved through the use of DC-DC converters. All boards will use an isolated DC-DC converter arrangement similar to the drawing below:



The 48V and 48VR inputs are floating with respect to GND, so no ground loops will be created. The converter common output pin will tie to the board ground plane and also to crate/chassis ground, which is tied to platform ground through a wide low-inductance woven copper cable.

The DC-DC converters will work properly as long as the input voltage is in the range of 36-72VDC, so voltage drops on the cables are not a major concern. A transient voltage suppressor rated for 72V protects the converter from over-voltage conditions. (The HS-1201 power supply will shutdown if the output voltage exceeds 55VDC.)

On all boards the DC-DC converters are located near the backplane connectors and care has been taken to route the 48V/48VR nets on interior layers to minimize the likelihood of an operator touching these signals.

DFEA boards (slots 2-21) will use the DIDT QD48T015033 converter. The DFEC2 crate controller (slot 1) uses the Datel UEP-3.3/6000-D48 converter. Both converters have an input to output isolation rated to 1500V or better.

The power estimates used for these boards are very conservative. Actual power consumption has been measured to be approximately 250W per crate when all boards are installed and programmed (quiescent state). When taking data it is unlikely that power consumption will rise above 500W per crate.

Environmental Concerns

Bulk 48VDC Power Supplies and Cables

The bulk 48VDC power supplies are "off the shelf" commercially available units manufactured by Shindengen (model HS-1201). These power supplies meet the following safety standards: UL60950, CSA C.22.2 No. 60950, VDE or TUV through CB Report, EN60950 [2].

These power supplies are not RoHS compliant and contain tin/lead solder as well as fiberglass (FR4) printed circuit boards, capacitors, plastics, adhesives and traces of solvents used in the normal manufacturing process. In the event of a catastrophic component failure a small amount of the material inside the supply could conceivably be vented into the D0 collision hall. It should be noted that these power supplies are externally fused to prevent overloading. Furthermore, the power supplies contain thermal sensors and fan speed sensors and will shutdown automatically if the internal temperature climbs significantly above ambient conditions.

All lead solder is contained inside the power supply and not accessible by anyone who would be installing or removing the supplies. The lead solder is therefore not subject to disruption that might make it hazardous per PPD-ESH-005 ("Safe Handling of Lead").

All power supply cabling (including lugs and bus-bars) are constructed of tin-plated copper.

Backplanes and DFEA2 Boards

The backplanes and DFEA2 boards are not built to RoHS specifications and contain lead solder joints as well as fiberglass (FR4) printed circuit boards, capacitors, plastics and traces of solvents (flux remover, etc.) used in the normal electronics fabrication process.

The backplane and DFEA2 boards are fused (in multiple places) to prevent uncontrolled energy from dissipating and potentially burning components and venting toxic substances into the D0 collision hall.

Lead solder joints in the backplane and on the boards are not disturbed when boards are inserted, removed, and handled normally. All board repairs should be done in an environment where exposure to lead is controlled per PPD-ESH-005.

References

1. Intel Server System Infrastructure (SSI) Distributed Power Supply (DPS) specification, available at:
http://www.ssiforum.org/Power%20Supplies%20%20Dated/DPS%20Dated%20_spec_1_0.pdf

2. Shindengen HS-1201 Power Supply information available at:
http://www.shindengen.com

3. IPC-D-275 Specification

4. ERNI Hard Metric Catalog, available online at
http://www.erni.com/DB/literature/ermet.ssi

5. Brooks, Douglas, "Temperature Rise in PCB Traces", available online at
http://www.ultracad.com

Revision History

5 October 2004: added RM control bit definitions.

27 October 2004: change cover page to include PORC information from R. Hance's guidelines. Added note about 10k resistors to ground on the 48V and 48VR lines. DC distribution uses 10AWG and 30A inline fuse. Add more detailed information about the RMI inputs. Add section explaining how AC and 48V conductors are covered and shielded. Added rack drawings of PW01-PW03.

22 March 2006: the shutdown finally occurs and this document is updated to reflect the actual hardware installation. Remove references to the test crate in PW02. Update power consumption estimates. Add section explaining the interlock system.

28 March 2006: added the circuit to perform the AND of the interlock signals.

4 April 2006: added "Environmental Concerns" section.

10 January 2008: add interlock box schematic to appendix A and drawing reference.

Appendix A: Interlock Box Schematic

This drawing is filed 0000-EA-173604.