DWG NO	SN	REV

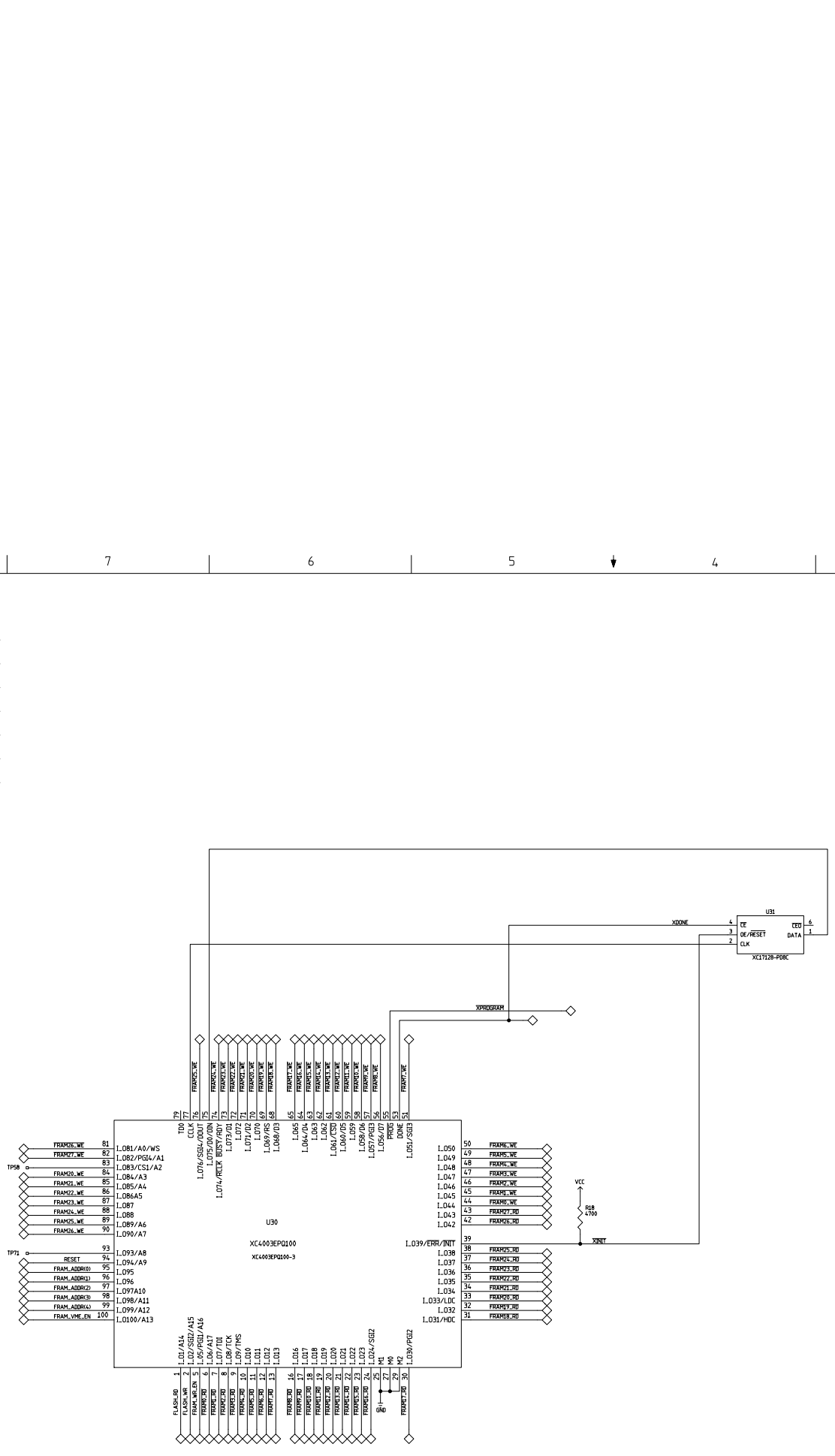
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

FRAM_ADDR(4:0)
FRAM_WR_EN
FRAM_VME_EN
FLASH_RD
FLASH_WR
XPROGRAM
RESET

FRAM0_RD
FRAM1_RD
FRAM2_RD
FRAM3_RD
FRAM4_RD
FRAM5_RD
FRAM6_RD
FRAM7_RD
FRAM8_RD
FRAM9_RD
FRAM10_RD
FRAM11_RD
FRAM12_RD
FRAM13_RD
FRAM14_RD
FRAM15_RD
FRAM16_RD
FRAM17_RD
FRAM18_RD
FRAM19_RD
FRAM20_RD
FRAM21_RD
XDONE
FRAM20_WE
FRAM21_WE
FRAM22_WE
FRAM23_WE
FRAM24_WE
FRAM25_WE
FRAM26_WE

FRAM22_RD
FRAM23_RD
FRAM24_RD
FRAM25_RD
FRAM26_RD
FRAM27_RD
FRAM0_WE
FRAM1_WE
FRAM2_WE
FRAM3_WE
FRAM4_WE
FRAM5_WE
FRAM6_WE
FRAM7_WE
FRAM8_WE
FRAM9_WE
FRAM10_WE
FRAM11_WE
FRAM12_WE
FRAM13_WE
FRAM14_WE
FRAM15_WE
FRAM16_WE
FRAM17_WE
FRAM18_WE
FRAM19_WE
FRAM20_WE
FRAM21_WE
FRAM22_WE
FRAM23_WE
FRAM24_WE
FRAM25_WE
FRAM26_WE
FRAM27_WE



CDF UPGRADE ELECTRONICS	Fermi National Accelerator Lab	
	ADMEM - PreProduction CDF Front-End Slave Interface FLASH RAM Control Xilinx FPGA	
Theresa M. Shaw	SIZE D / FSNC NO / DWG NO TMS-ADMEM-041597-P3B	REV A
RD/EED/EES	SCALE	SHEET 1 of 1

E:\JOBS_ADMEM\Analog_Admem\Analog_Admem\vbdc\admem_pre_prod.sbk!Flash_control1(40;19) Mon Jul 20 14:38:50 1998