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Detailed System Description of the HFT PIXEL RDO System

This document is an extension of the PIXEL RDO addendum to the HFT proposal. It is intended to give detailed parameters of the function of the PIXEL readout system that will allow for the understanding of the logic and memory and requirements and the functionality of the readout system. We will present the designs of the Phase-1 and Ultimate readout systems under periodic triggering conditions. The simulation of the system response to random triggering of the type expected to be seen at the STAR experiment is ongoing and will be available upon completion. The readout design is highly parallel and one of the ten parallel readout systems is analyzed for each system.

Phase-1 Readout Chain

The Phase-1 detector will consist of two carrier assemblies, each containing four ladders with ten sensors per ladder. The readout is via parallel identical chains of readout electronics. The relevant parameters from the RDO addendum are reproduced below.

Item	**Number**
Bits/address	20
Integration time	640 μs
Hits / frame on Inner sensors (r=2.5 cm)	59
Hits / frame on Outer sensors (r=8.0 cm)	6
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 1 Parameters for the Phase-1 based detector system used in the example calculations shown below.

The functional schematic of the system under discussion is presented below

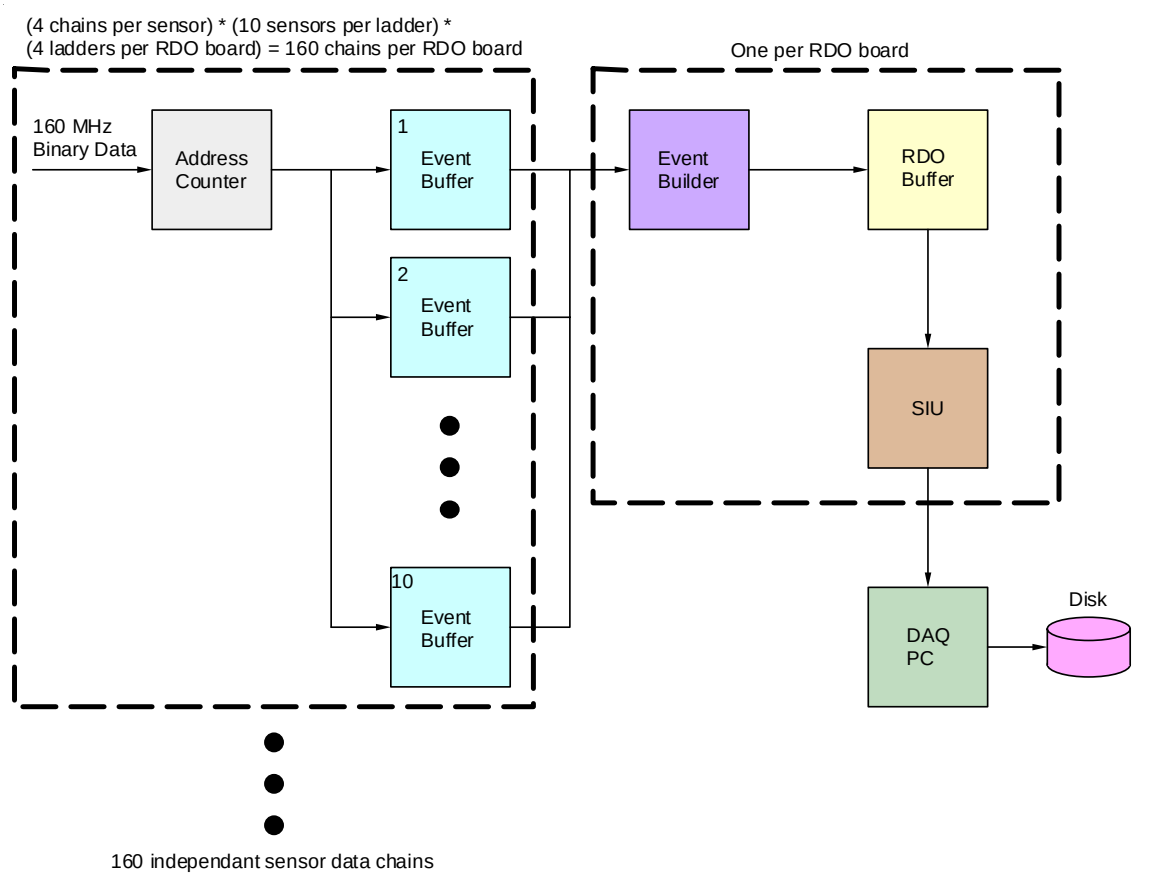

Figure 1 Functional schematic diagram for one Phase-1 sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for two cases. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic trigger rate of 2 kHz. These cases make the scaling clear. In both cases we will use the average (pile-up included) event size. We are currently simulating the dynamic response of the system to the triggering and event size fluctuations seen at STAR and will make this information available after the simulations are completed. It is important to note that the system is FPGA based and can be easily reconfigured to maximize the performance by the adjustment of buffer sizes, number of buffers, and most other parameters. The relevant parameters of the system pictured above are described below;

Data transfer into event buffers – The binary hit data is presented to the address counter at 160 MHz. The corresponding hit address data from the adders counter is read synchronously into the event buffers for one full frame of a 640 × 640 sensor at 160 MHz. This corresponds to an event buffer enable time of 640 μs.

Event Buffer – Each event buffer is 10 × the size required for the average inner sensor sized event data stream. The average inner sensor has 59 hits / event. There are 4 outputs per sensor so the average event address length is (0.25 sensor area) × (59 hits) × (20 bits) × (10 factor for event size fluctuations) = **2950 bits or 147 20-bit addresses**.

Data transfer into the RDO buffer via the event builder – The event buffers remain busy until all of the event buffers from that event are read out into the RDO buffer. This process is internal to the FPGA, does not require computational resources, and can run at high speed. In the interests of simplicity, we will assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then the address data from the event buffers is transferred into the RDO buffer in 20-bit words. The average carrier event size is [(6 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (59 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **1925 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **192.5 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **12 µs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. The data transfer rates for the SIU – RORC combination as a function of fragment size are shown below.

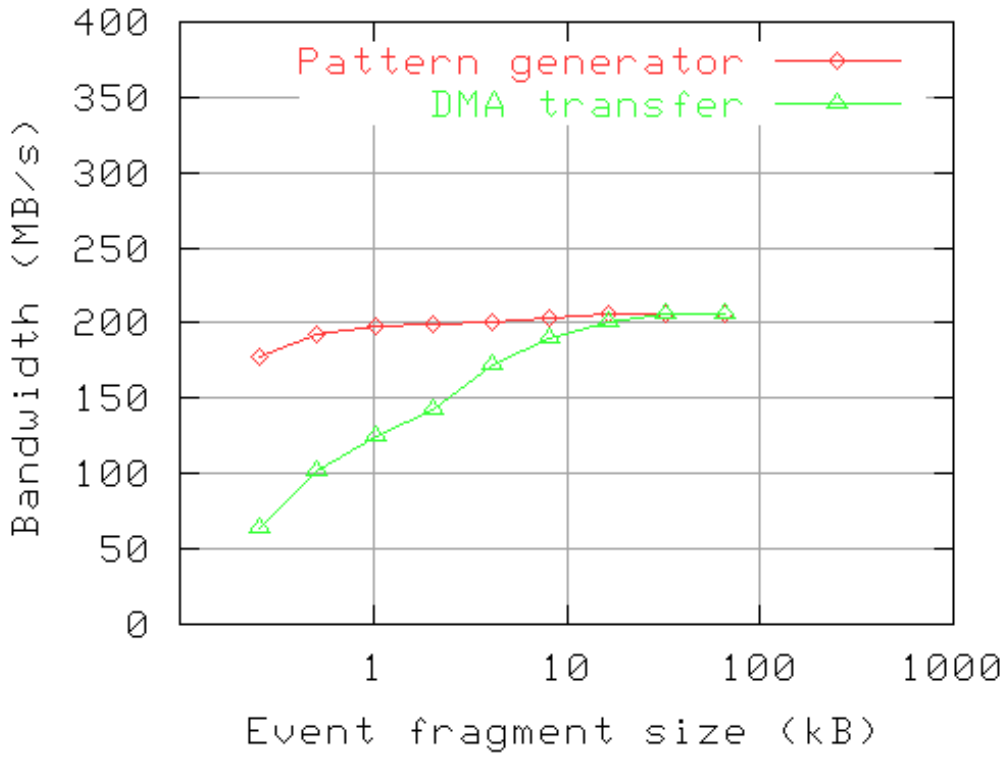

Figure 2 Bandwidth of the SIU - RORC fiber optic link as a function of event fragment size.

In this case, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) × (1925 address words) **= 61.6 kb or 7.7 kB.** In this example, our transfer rate is ~ 150 MB / s. This transfer then takes **51 µs.**

Data transfer to the DAQ PC Hard Disk drive – The event data is buffered in the DAQ PC RAM (>4GB) until only accepted events are written to disk and then transferred via Ethernet to an event building node of the DAQ system. Level 2 trigger accepts are delivered to the RDO system and transferred via the SIU – RORC to the DAQ receiver PCs. Only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the following chronograms.

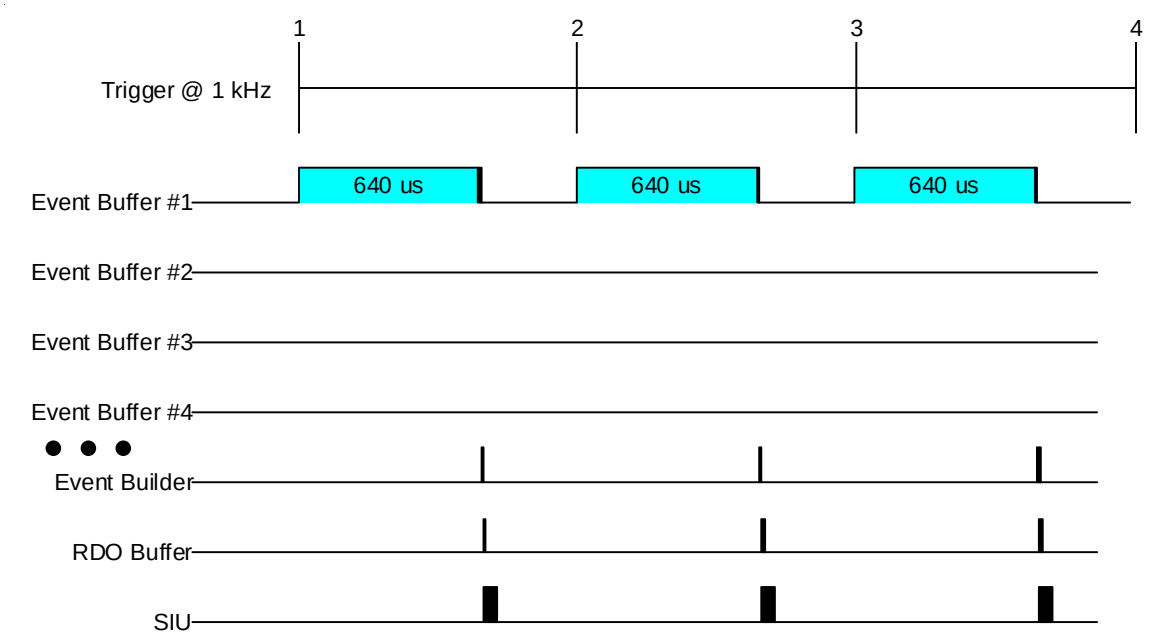

Figure 3 Chronogram of the Phase-1 based readout system functions for a 1 kHz periodic trigger.

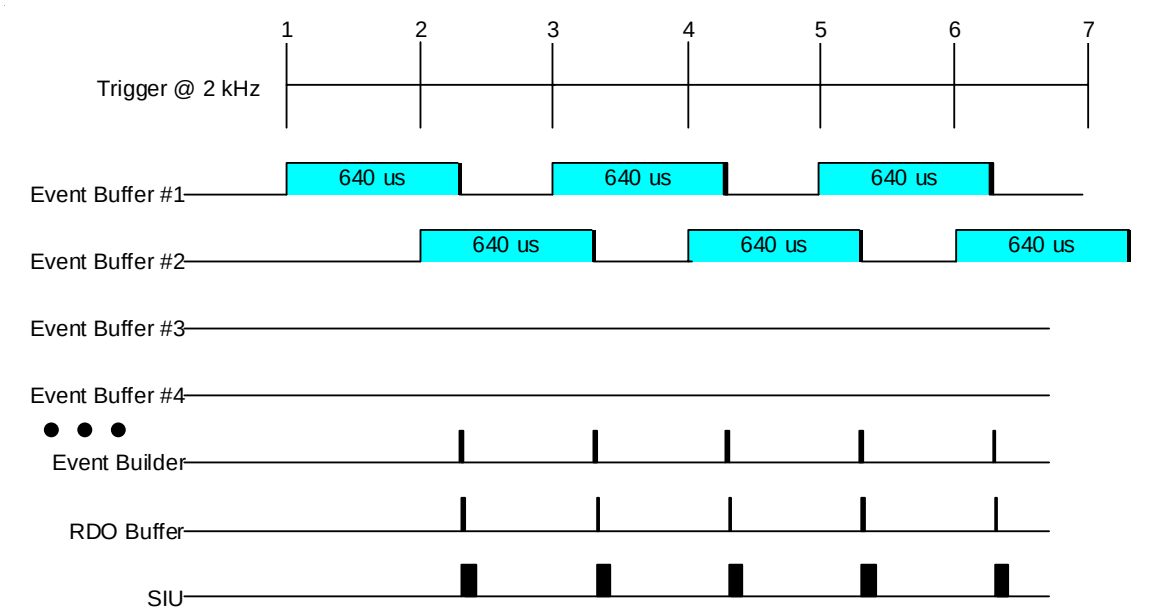

Figure 4 Chronogram of the Phase-1 based readout system functions for a 2 kHz periodic trigger.

The memory resources required in the FPGA / motherboard combination are (160 readout buffers) × (2.95 kb per event buffer) + (192.5 kb for the RDO buffer) = **664.5 kb**. The Xilinx Virtex-5 FPGA in our design contains 4.6 – 10.4 Mb of block RAM so the entire design fits easily into the FPGA.

Ultimate Sensor Detector Readout Chain

Again, the Ultimate sensor readout system consists of ten parallel readout chains. The main difference between the Phase-1 sensors and the Ultimate sensors is the inclusion of zero suppression circuitry in the Ultimate sensor, thus only addresses are read out into the RDO boards. In addition, the integration time of the Ultimate sensor is 200 μs and there is one data output per sensor. These differences lead to the functional schematic of the readout system shown below.

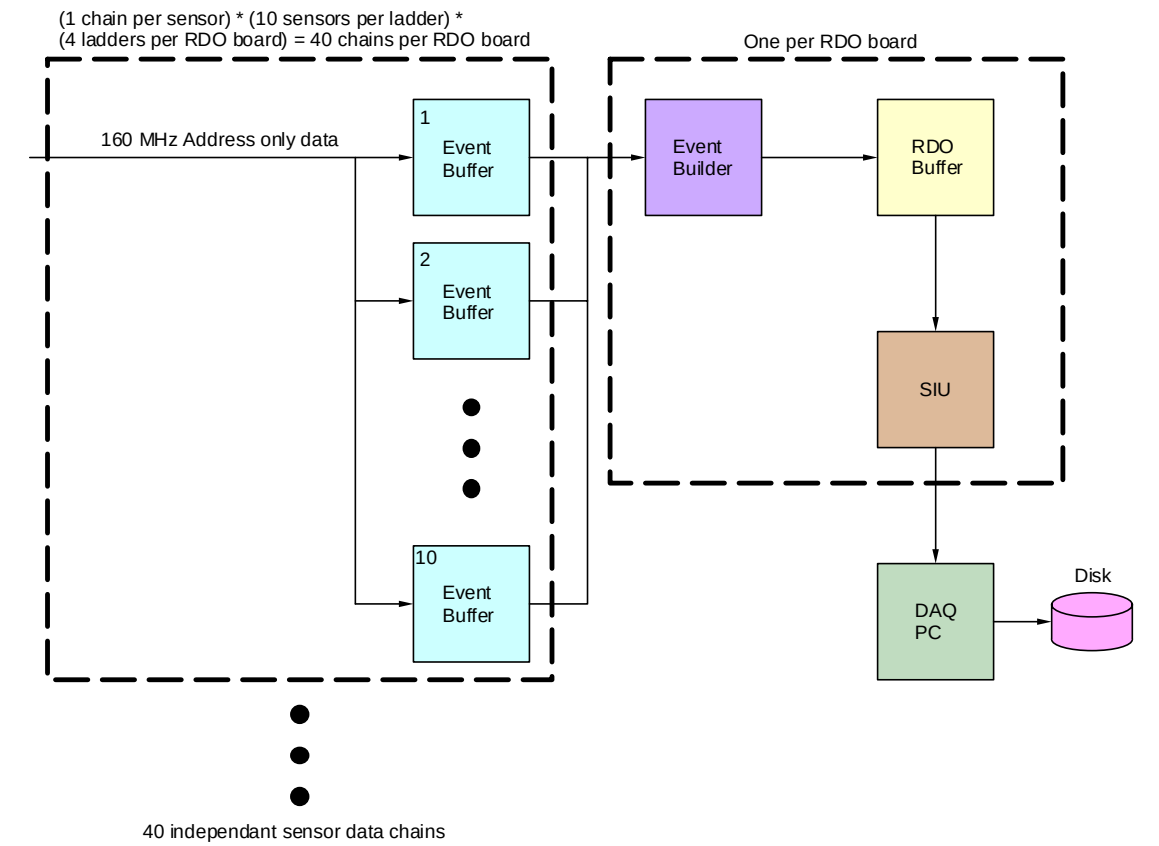

Figure 5 Functional schematic diagram for one Ultimate sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for the same two cases as shown for the Phase-1 readout system. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic data rate of 2 kHz. Again, in both cases we will use the average (pile-up included) event size. The relevant parameters of the Ultimate sensor based system pictured above are described below;

Item	Number
Bits/address	20
Integration time	200 μs
Hits / frame on Inner sensors (r=2.5 cm)	61.5
Hits / frame on Outer sensors (r=8.0 cm)	6
Ultimate sensors (Inner ladders)	100
Ultimate sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 2 Parameters for the Ultimate sensor based detector system used in the example calculations shown below.

Data transfer into event buffers – The 20-bitaddress data is presented to the event buffer 160 MHz. The integration time is now 200 μs giving an event buffer enable time of 200 μs.

Event Buffer – Each event buffer is 10 × the size required for the average inner sensor sized event data stream. The average inner sensor has 61.5 hits / event. There is one output per sensor so the average event address length is (1 sensor) × (61.5 hits) × (20 bits) × (10 factor for event size fluctuations) = **12,300 bits or 615 20-bit addresses**.

Data transfer into the RDO buffer via the event builder – As before, the event buffers remain busy until all of the event buffers from that event are read out into the RDO buffer. In the interests of simplicity, we will again assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(6 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (61.5 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **1988 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **198.8 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **12.4 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. Again, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) × (1988 address words) **= 63.6 kb or 7.9 kB.** In this example, our transfer rate is ~ 150 MB / s. This transfer then takes **53 μs.**

Data transfer to the DAQ PC Hard Disk drive – Again, only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the following chronograms.

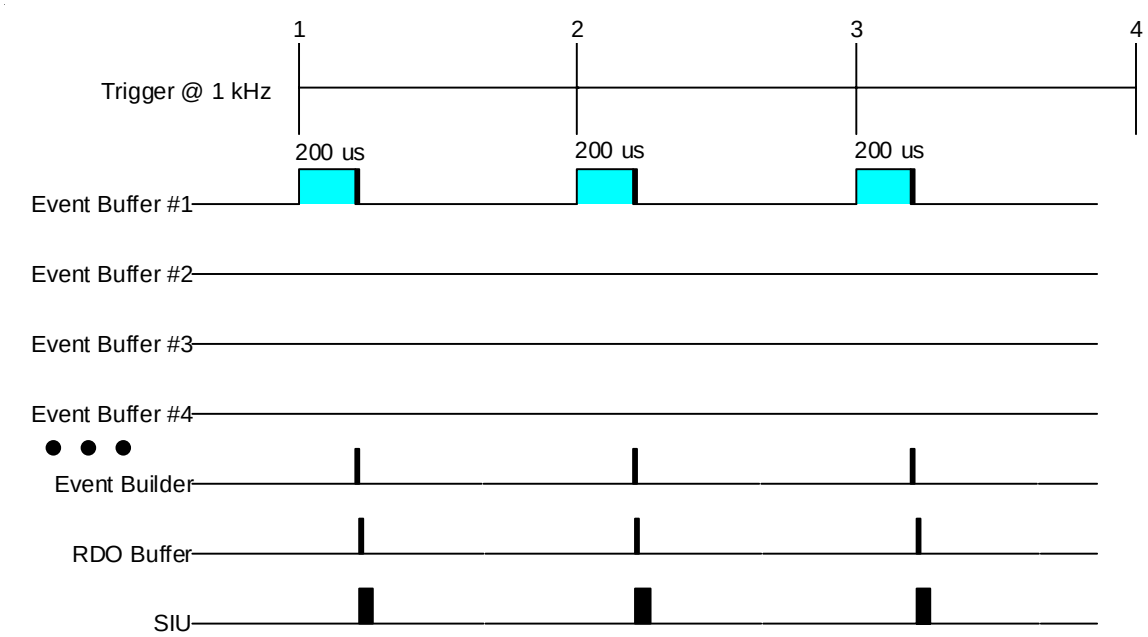

Figure 6 Chronogram of the Ultimate sensor based readout system functions for a 1 kHz periodic trigger.

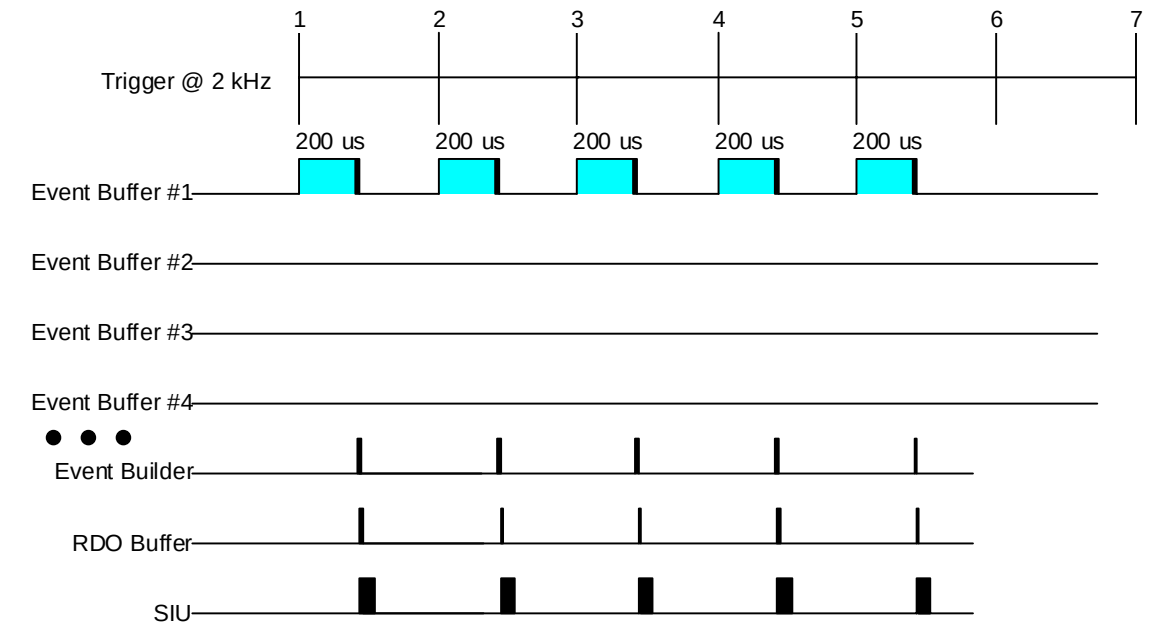

Figure 7 Chronogram of the Ultimate sensor based readout system functions for a 2 kHz periodic trigger.

The system memory resource requirements are effectively the same as those required for the Phase-1 RDO system. This fits easily into the memory resources of the Virtex-5 FPGA.