INTRODUCTION ***SCOTT HOLM***

<u>FINDER CHIP</u>

- ***FUNCTION***

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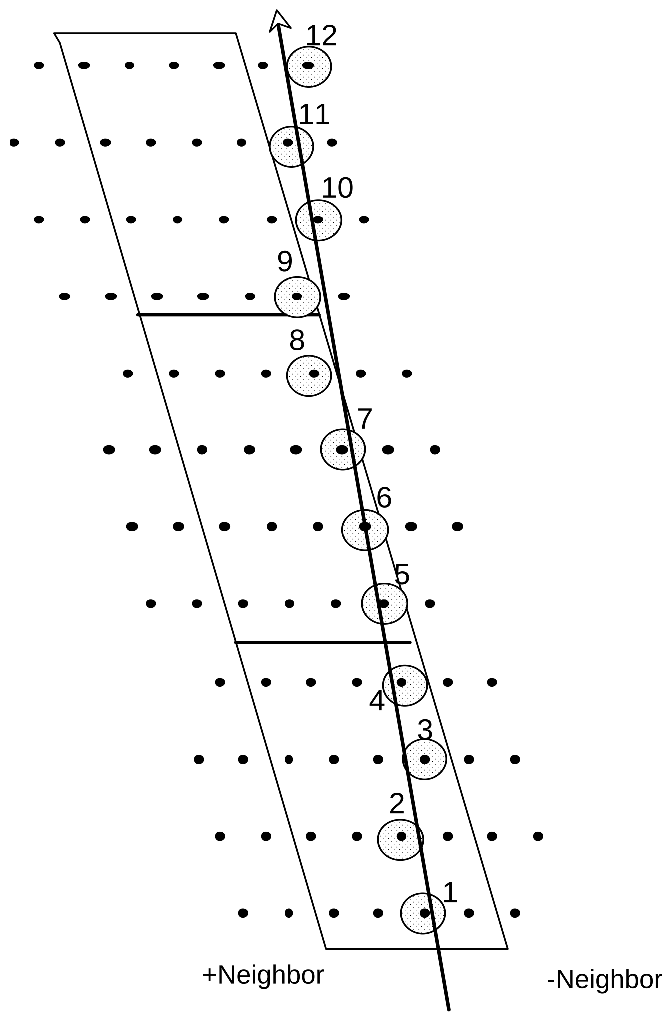
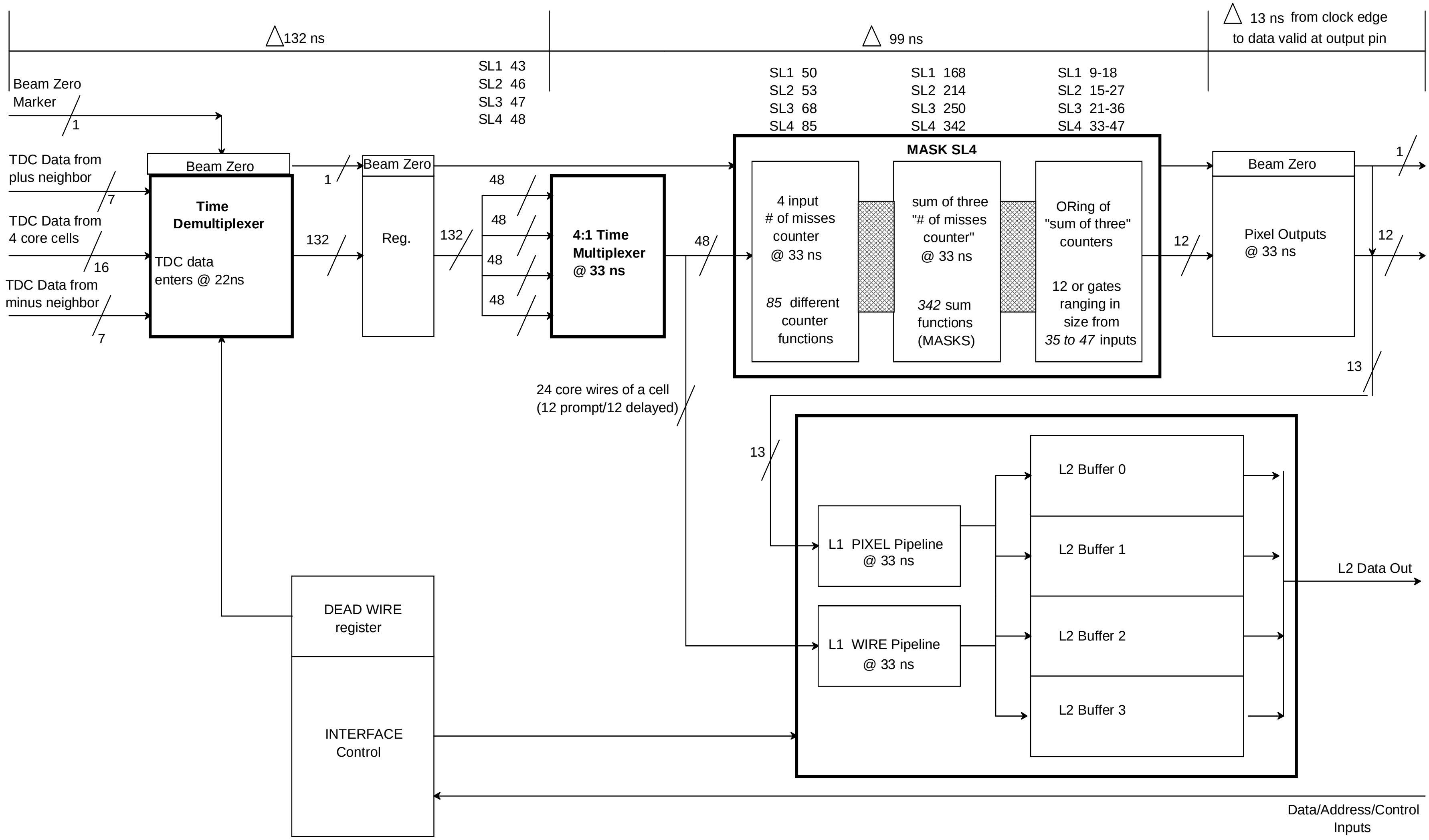
FINDER - FUNCTION

- **Identify track segments in a Super Layer.**
- **Send segment information to the LINKER.**

1. **Segment is present when 9 out of a set of 12 wires(MASK) related to a cell are on or “hit”.**
2. **Segment is represented by a pixel which tell the location and/or slope of the segment in the cell.**
3. **Twelve pixels for each cell.**



12 wires of a MASK
Line shows a segment



XFT FINDER Block Diagram

SH 12/17/96

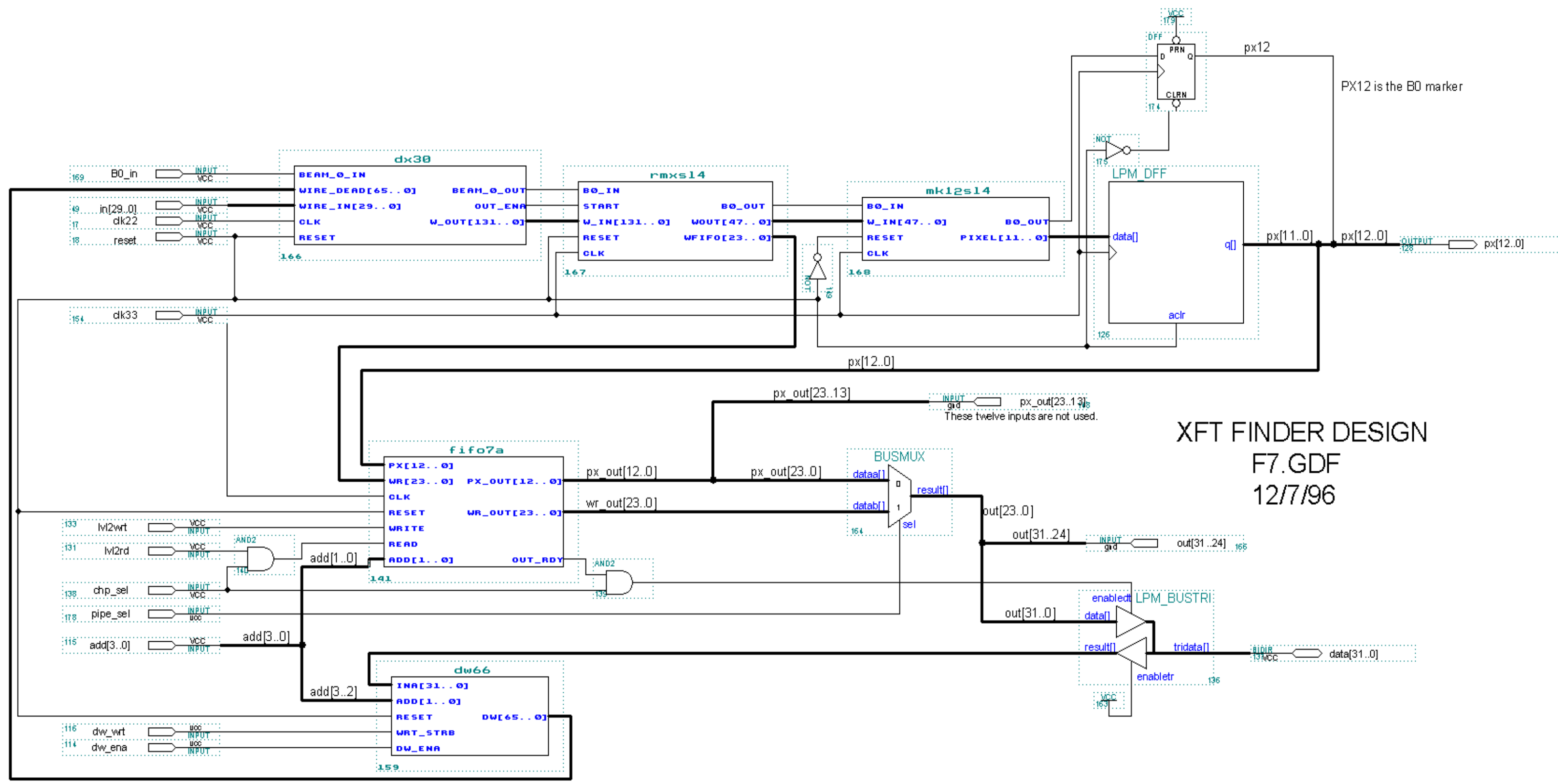
- **DEMULTIPLEXER**
  - 6 to 1 Time demultiplexer of wire information from the TDC operating at 22ns.
  - 6 time slices of wire information forms a 132 bit register that contains the prompt and delayed wire information of 4 cells and the pertinent neighboring cells wire information(9 wires each side).
  - 132 bit register is valid for the next 132ns.
- **MULTIPLEXER**
  - 1 to 4 multiplexer of wire information from the 132 bit register.
  - Multiplexes the 132 bits of wire information into 4 - 48 bits of wire information that relate to each of the 4 cells and feeds them to the MASK set.
  - The 48 wires change every 33ns so in 132ns four cells of wire information are pipelined into the MASK block.
  - Multiplexer also sends the prompt and delayed wire information of a cell to the level 1 pipeline every 33ns so in 132ns the level 1 pipeline receives the prompt and delayed information of all four cells.
- **MASK SET**
  - Looks for the number of misses within a group of 12 wires(MASK).
  - If the number of misses is 3 or less, a pixel that relates to a segment in the cell is turned on.
  - More than one Mask may turn on the same pixel.
  - The Mask set has 3 pipelined stages running at 33ns so the 12 bits of pixel data for a cell is output 99ns after the wire information for that cell is selected by the Multiplexer.
- **LEVEL 1 PIPELINE & LEVEL 2 BUFFERS**
  - The wire and pixel information of the four cells are stored in a level 1 pipeline that is programmable up to 64 time slices(132ns) deep.
  - On a level 2 write command the wire and pixel information of the 4 cells from one time slice(132ns) is stored in one of four level 2 buffers.
  - Level 2 buffers are readable through VME.

FINDER IMPLEMENTATION

- FINDER design implemented in a CPLD using ALTERA MAXPLUS2 software with the targeted device a **ALTERA EPF10K50RC240-3** "FLEX 10K50"

- FLEX 10K50:
  - Contains both embedded arrays and logic arrays.
  - 2,880 logic elements - 20,480 RAM bits - 3,184 registers - 189 I/0 elements
  - In circuit reconfigurable via external configuration EPROM, Intelligent controller or JTAG.

- Design is implemented with a top level schematic in a graphical design file.
  - The graphical design file include symbols which contain text design files written in the ALTERA hardware description language(AHDL) and other graphical design files.



XFT FINDER DESIGN
F7.GDF
12/7/96
PX12 is the B0 marker
px12
LPM_DFF
data[]
q[]
aclr
px[11..0]
px[12..0]
px[12..0]
dx30
BEAM_0_IN
WIRE_DEAD[65..0]
WIRE_IN[29..0]
CLK
RESET
BEAM_0_OUT
OUT_ENA
W_OUT[131..0]
rmxs14
B0_IN
START
W_IN[131..0]
RESET
CLK
B0_OUT
WOUT[47..0]
WFIFO[23..0]
mk12s14
B0_IN
W_IN[47..0]
RESET
CLK
B0_OUT
PIXEL[11..0]
B0_in
in[29..0]
clk22
reset
clk33
fifo7a
PX[12..0]
WR[23..0]
CLK
RESET
WRITE
READ
ADD[1..0]
PX_OUT[12..0]
WR_OUT[23..0]
OUT_RDY
px_out[12..0]
wr_out[23..0]
px_out[23..13]
px_out[23..0]
These twelve inputs are not used.
BUSMUX
dataa[]
datab[]
result[]
sel
out[23..0]
out[31..24]
out[31..0]
LPM_BUSTRI
enabledt
data[]
result[]
tridata[]
enabletr
data[31..0]
lvl2wrt
lvl2rd
chp_sel
pipe_sel
add[3..0]
add[1..0]
add[3..2]
dw66
INA[31..0]
ADD[1..0]
RESET
WRT_STRB
DW_ENA
DW[65..0]
dw_wrt
dw_ena

FINDER RESULTS

- **FITTING - Different FINDER design for each Super Layer.**

MAX+plus II Compiler Report File
Version 7.0 08/26/96
Compiled: 12/11/96 13:23:35

******* Project compilation was successful**

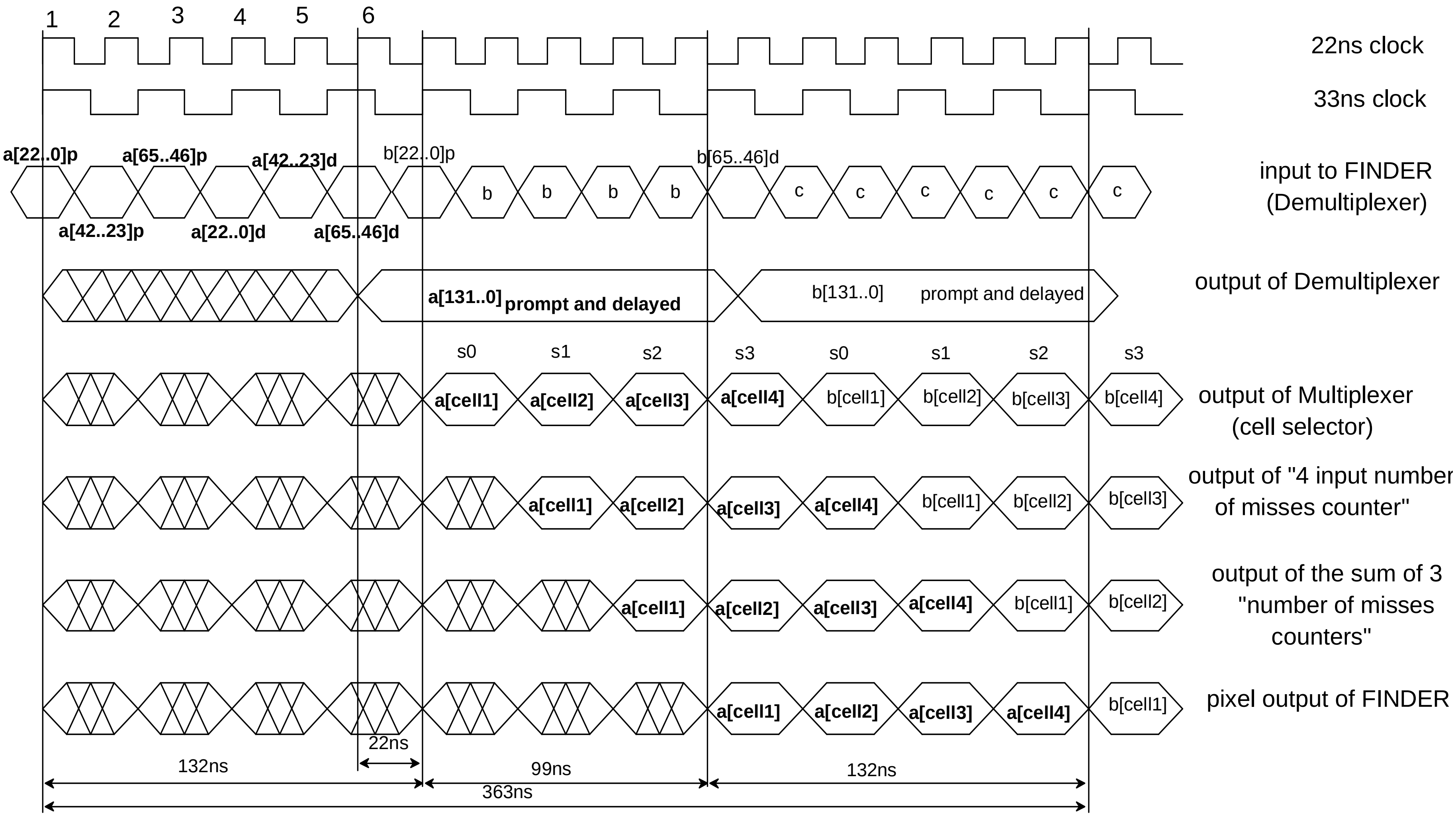
**** DEVICE SUMMARY ****

Chip/ POF	Device	In Pins	Out Pins	Bidir Pins	Memory Bits	Memory % Utilized	LCs	Lcs % Utilized	# Masks
fndsl1	**EPF10K50RC240-3**	**93**	**13**	**32**	**9908**	**48 %**	**1304**	**45 %**	**168**
fndsl2	**EPF10K50RC240-3**	**63**	**13**	**32**	**9908**	**48 %**	**1481**	**51 %**	**214**
fndsl3	**EPF10K50RC240-3**	**63**	**13**	**32**	**9908**	**48 %**	**1670**	**57 %**	**250**
fndsl4	**EPF10K50RC240-3**	**63**	**13**	**32**	**9908**	**48 %**	**2064**	**71 %**	**342**

All four designs similar with the exception of the number of masks and also SL1 has 30 extra input pins for the possibility of having the wires come out both sides of detector.

- **SIMULATION**

  - Timing Simulation was successful with 22ns input clock and 33ns output clock. Simulator checks of setup/hold time of registered data within the chip were OK.
  - DEMULTIPLEXING at 22ns requires that the input portion of the design be hand placed.
  - Requires 3 time slices(132ns) for the data to be extracted from the wire information and forwarded to the LINKER. 4 cells worth of information.



XFT FINDER - Timing Diagram

SH 12/17/96

FINDER COST

- Quantity = 336
- 24 SL1/3 boards each having 6 FINDERS = 144
- 24 SL2/4 boards each having 8 FINDERS = 192
- total = 336 + LINKERs
- >500 quantity $256.00 each.   Jan. 97 pricing
- 336 * $256 = $86,016
- price is expected to drop by time order is placed