IP-177 Eight Channel Delay Timer

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The IP-177 timer is an IndustryPack module containing eight delay timers. This design uses the General Purpose IP module, GPIP, a commercially available IP module that contains an Altera 10K40 FPGA, 256k bytes of static RAM, two receivers for incoming clock signals, and 40 bits of digital I/O connected to the user connector shown in Figure 1. Various designs can be effected by programming a small PROM that is socketed on the GPIP.

Characteristics of the IP-177

The IP-177 has eight 16-bit delay timers on board. Each channel has an associated delay register, an output pulse width register, and a control register. Once triggered, the timers will delay for a variable amount of time determined by the value stored in the delay register before outputting a pulse with a width determined by the value stored in the width register. Figure 2 shows the memory map for the IP-177 module where addresses listed are the offsets from the module base address. Diagrams of the control registers are shown in Figures 3-7. Parameters that affect all channels are stored in the Master Control Register. In these registers, a bit value of "1" causes the named function of the bit to be enabled.

Clock Input

The input to the IP-177 module is normally the Fermilab Tevatron Clock, TClk, signal. A self tracking input to an analog discriminator helps to eliminate the need for input threshold adjustment, and helps maintain the symmetry of the clock signal. Logic in the Altera Gate array uses the onboard delay line to decode the modified Manchester TClk signal to recover both the 10 MHz clock frequency and the 8-bit encoded events. For use in other modules, there is an option to repeat the incoming clock through two separate drivers. The 10 MHz timebase and a 1 MHz signal are also driven off the module for use by external devices.

Channel control registers

Operating characteristics of the individual timing channels are determined by settings in the 8-bit Channel Control registers shown in Figure 2. Individual bits are assigned as follows:

Bit 7-	*Enables the timer output*
Bits 6 & 5-	*Timebase Select. Values 00, 01, 10, 11 select timebase prescaled by 1, 10, 100, or 1000, respectively, to allow for longer delays*
Bit 4-	*Enable ExtTrig for Prescale sync.*
Bit 3-	*Booster Reset Enable. This is a logical "OR" of TClk events $11, $12, $13, $14, $15, $16, $17, $19, $1C*
Bit 2-	*External trigger select enable*
Bit 1-	*Should be set to "1".*
Bit 0-	*Daisychain Enable. Only for odd numbered channel Control Registers ($41, $45, $49, and $4D)*

Master Control Register

There is a single 8-bit Master Control register that controls functions for the module. The bit assignments are as follows:

Bit 7-	*Enables the TClk out signals to be driven offboard as TClkOut0 and TClkOut1.*
Bit 6-	*Enables the 10MHz signal to be driven offboard.*
Bit 5-	*Enables the 1 MHz signal to be driven offboard*
Bit 4-	*Enables prescaler synchronization.*
Bit 3-	*1-Select Booster Reset as the prescale synchronization event* *0- Select Sync Event Register (Addr $52) as the prescale synch event*
Bit 2-	*1- Use offboard 10MHz timebase* *0- Use onboard 10 MHz oscillator.*
Bit 1-	*1- Enable external 10MHz timebase* *0- Use 10MHz recovered from TClk*
Bit 0-	*Enables four gate signals to be driven offboard.*

Triggering from TClk events

TClk is received using an analog discriminator whose output is input to the 10K40 FPGA. Using a tapped delay line and logic in the FPGA, the TClk signal is decoded and all the clock events are decoded into 8-bit values. These values are used as an address to access 256 byte-wide words of a RAM array included in the FPGA. The RAM array is preloaded at reset time with data that determines which timer channels are to be triggered by each TClk event. A "1" stored in a given bit location will cause the corresponding timer channel to trigger when that location is accessed. For example, if the number $A1 is stored in the RAM array location $10, then when TClk event $10 is detected, timer channels 7, 5, and 1 will be triggered. This design has been used for many years in legacy timer modules implemented in CAMAC and VMEbus. Because any value may be stored in any word of the RAM array, triggers for a given channel may be the OR of the occurrence of several TClk events.

Many timers need to be triggered at Booster Reset time, 15 times per second. Triggering at Booster reset time requires the OR of nine different TClk events. Because this is a common requirement, the logic for this trigger is included in the gate array, and is enabled by storing a "1" in bit 3 of the individual timer control register.

Timing channels in the IP177 may be used in pairs in a mode where an even numbered channel's output pulse triggers the next higher odd numbered channel. This mode, called *daisychain* mode, couples the two timing channels so that they may be used in coarse/fine or start/width applications.

Timebase Considerations

Using the 10 MHz timebase recovered from TClk, a 16-bit delay timer can provide delays of only 6.5 ms. To allow for longer delays, three decade scalers are included in the logic of the gate array. Each timer channel can select one of the resulting four timebase frequencies; 10MHz, 1MHz, 100kHz, or 10kHz. The selection is made separately for each timer using bit 6 and bit 5 of the individual channel control register shown in Figure 4. The resolution of the timer is equal to the period of the selected timebase. To eliminate the time jitter caused by using different timebase frequencies, the scalers are synchronized by resetting them at a known time early in the cycle. The scalers may be reset by Booster Reset, by the occurrence of the TClk event stored in the Synchronize Event Register, or by an externally supplied pulse.

Software triggering of timer channels

For each timer channel, there is a register location that may be written to cause the channel to trigger. The value that is written is not used, only the fact that the location was accessed. The memory offsets for this software triggering feature are $60, $62, ...$6E for triggering channels 0, 1, ...7, respectively.

Interrupts

Each IP module has two interrupt lines to use for interrupting the host processor. The IP177 module uses delayed output pulses from timer channels 0 and 1 to trigger latches that assert IRQ0 and IRQ1. In response to the interrupt, the processor will acknowledge the interrupt and retrieve IRQ0 Vector or IRQ1 Vector. These vectors are stored in offset addresses $5A and $5C. IRQ0 and IRQ1 interrupts are separately enabled by bits 0 and 1, respectively, of the IRQ Enable register located at offset address $5E. Interrupt requests are cleared when the processor reads the interrupt vector during the interrupt cycle.

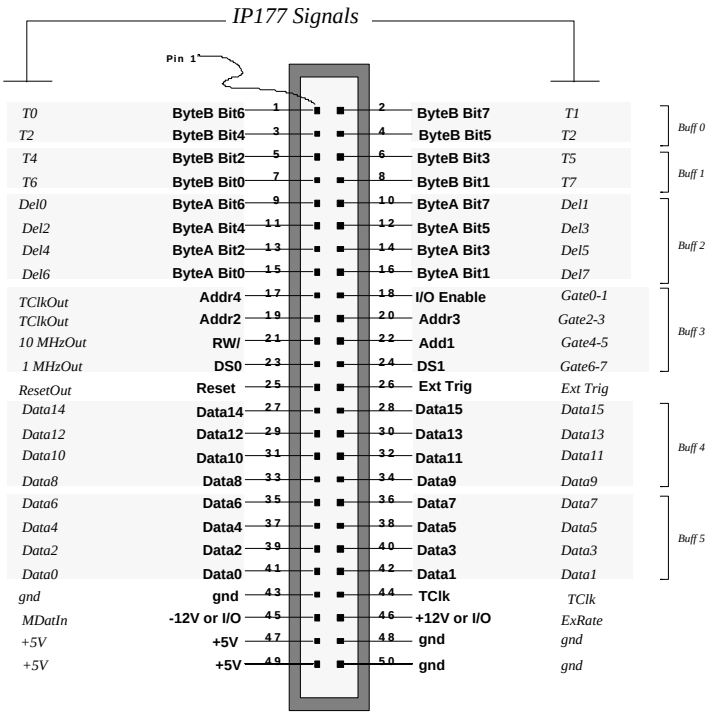


Figure 1. I/O Interface Connector Pinout for GP-IP Delay Timers

$00	Channel 0 Delay		Channel-0 Width	
$08	Channel-1 Delay		Channel-1 Width	
$10	Channel-2 Delay		Channel-2 Width	
$18	Channel-3 Delay		Channel-3 Width	
$20	Channel-4 Delay		Channel-4 Width	
$28	Channel-5 Delay		Channel-5 Width	
$30	Channel-6 Delay		Channel-6 Width	
$38	Channel-7 Delay		Channel-7 Width	
$40	ControlReg 0	ControlReg 1	ControlReg 2	ControlReg 3
$48	ControlReg 4	ControlReg 5	ControlReg 6	ControlReg 7
$50	Master Control Reg	Sync. Event Reg		
$58		IRQ0 Vector	IRQ1 Vector	IRQ Vector Enable
$60	SW Trig 0	SW Trig 1	SW Trig 2	SW Trig 3
$68	SW Trig 4	SW Trig 5	SW Trig 6	SW Trig 7

Figure 2. Register Map for IP177 Eight Channel Timer

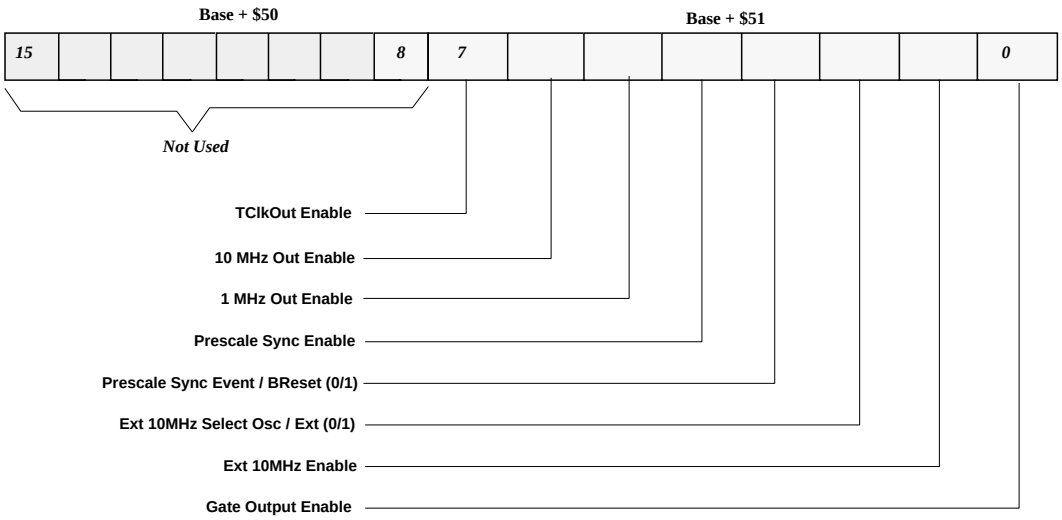
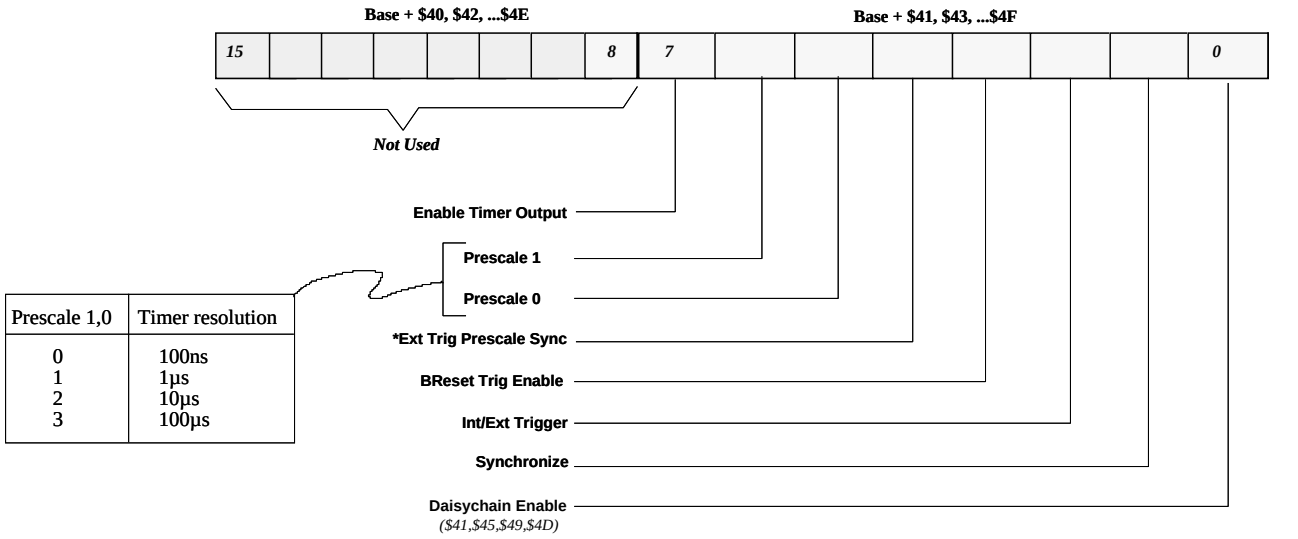


Figure 3. Master Control Register for IP177 Eight Channel Timer



* External trigger prescale sync control is Base + $41 only, but affects all 8 timers.

Figure 4. Control Registers for Individual IP177 Timer Channels

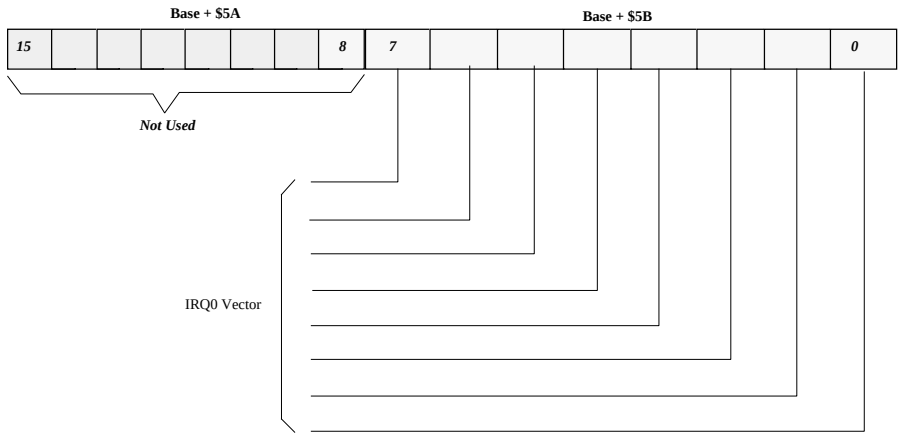


Figure 5. IRQ0 Vector Register for IP177 Eight Channel Timer

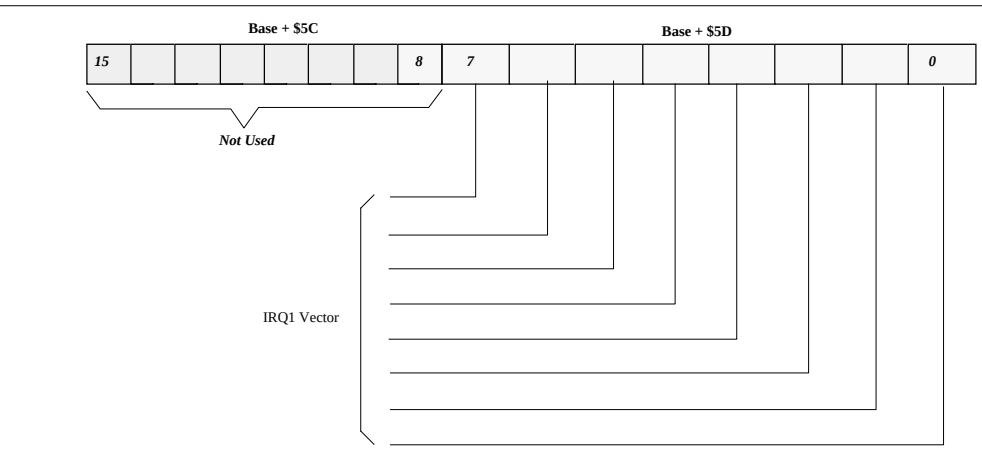


Figure 6. IRQ1 Vector Register for IP177 Eight Channel Timer

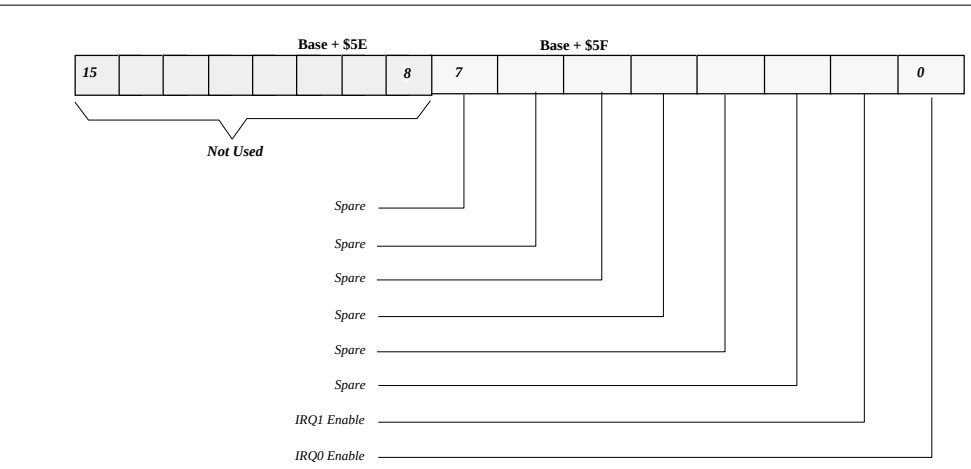


Figure 7. IRQ Vector Enable Register for IP177 Eight Channel Timer