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Bias voltages for VDDA = 2.5 V and 2.0 V

node	b1	b2	b3	b4	b5	p6	paset	R_{paset} [Ω]
voltage [mV]	612.1	656.0	768.3	1,574	1,492	1,893	57.95	1.8 K
voltage [mV]	606	700	754	1,594	1,534	1,922	60.3	1.8 K ± 10
voltage [mV]	620	689	770	1,568	1,503	1,894	62.4	1805 ± 5
voltage [mV]	610	676	755	1,571	1,524	1,908	62.7	1803 ± 5
voltage [mV]	611	676	759	1,579	1,517	1,905	-	1801 ± 5

Table 1: **Simulated** bias voltages at VDDA = 2.5 V (top) and **measured** for Chips I - IV.

node	b1	b2	b3	b4	b5	p6	paset	R_{paset} [Ω]
voltage [mV]	616.8	169.1	776.7	1,084	980.8	1,396	57.82	1.8 K
voltage [mV]	606	219	752	1,101	1,034	1,423	59.1	1.8 K
voltage [mV]	618	206	769	1,076	1,004	1,396	60.9	1805 ± 5
voltage [mV]	609	195	754	1,079	1,022	1,411	61.7	1803 ± 5
voltage [mV]	611	197	761	1,083	1,014	1,406	-	1801 ± 5

Table 2: **Simulated** bias voltages at VDDA = 2.0 V (top) and **measured** for Chips I - IV.

Gain for Chips III and IV

#	C_{in} [pF]	ΔV_{out} [mV]	gain (at buffer): 2 V [mV/fC]	gain (at buffer): 2.5 V [mV/fC]
0	5	15.8	9.5	8.4
1	172.3	334	5.8	6.4
3	29.0	70	7.2	7.4
7	52.0	115	6.6	6.7
10	172.3	234	6.2	6.9
11	114.1	161	6.3	6.5

Table 3: Chip III: **measured** gain at VDDA = 2.0 V (left) and 2.5 V (right), $R_{paset} = 1.8K$,V_{in} = 100 mV, BW0=1,BW1=0.

Comment: less 'leakage' and more precise measurements at 2.0 V

#	C_{in} [pF]	gain (at buffer) [mV/fC]
0	50.4	7.5
2	51.6	7.5
4	51.8	7.4
6	52.0	7.4
10	52.0	7.4
11	52.4	7.1

Table 4: Chip IV: **measured** gain at VDDA = 2.5 V and $R_{paset} = 1.8K$, V_{in} = 94.8 mV, BW0=0, BW1=1.

Rise time and band width switch for Chips III and IV

BW 0/ BW 1	C_{in} [pF]	rise time (at buffer): chip III [ns]	rise time (at buffer): chip IV [ns]
0/0	52	17.0	17.6
1/0	52	75.5	80.5
0/1	52	111.0	115
1/1	52	158	174
0/0	172	24	-
1/0	172	123	-
0/1	172	171	-
1/1	172	242	-

Table 5: Chip III and IV: **measured** rise times, (VDDA= 2.5 V, $R_{paset} = 1.8K$,V_{in} = 100 mV i.e. 52/3 or 172/3 fC).