EU Specific Targeted Research Project

MICROTRAP

"Development of a pan-European Microtrap Technology capability for Trapped Ion Quantum Information Science"

EU Framework 6 IST Programme

Future & Emerging Technologies Initiative

NPL

universität innsbruck

INSTITUT FOR FYSIK OG ASTRONOMI
IFA

Oxford Physics

CUANDO · UNIVERSITAT ULM · SCIENDO DOCENDO

Microtrap consortium

National Physical Laboratory, UK (Co-ordinator)

- *Patrick Gill, Alastair Sinclair & Guido Wilpers, Michael Brownnutt*

Universitaet Innsbruck, Austria

- *Rainer Blatt, Wolfgang Haensel, Hartmut Haeffner, Christian Roos, Piet Schmidt , Jan Benhelm ++*

University of Aarhus, Denmark

- *Michael Drewsen, Jens Sorensen, Solvejg Jorgensen ++*

University of Oxford, UK

- *David Lucas, Andy Steane, Matthew McDonnell, Nick Thomas ++*

Universitaet Siegen, Germany

- *Christof Wunderlich, Vladimir Elman, Michael Johanning ++*

Universitaet Ulm, Germany

- *Ferdinand Schmidt-Kaler, Kilian Singer, Robert Tammer, Stefan Schultz ++*

Microtrap

- Discussion at Michigan workshop, May 2004
- Pre-proposal to EU, September 2004
- Positive evaluation, Dec 2004
- Full proposal, May 2005
- Strongly positive evaluation, July 2005
- Contract negotiation, November/December 2005
- Scheduled start date, April 1st 2006

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Microtrap Programme

Phase 1: 0-18 months

Phase 1 Build

- Trap design and fabrication concept evaluation
- Comparison and selection of Supplier technology capabilities
- Purchase orders to preferred suppliers (by month 3)
- Supplier fabrication and sample chip supply to partners (by month 9)
- Evaluation of chip trap operation, cooling efficiency and heating /decoherence rates with various ions (by month 18)

In parallel:

- Efficient trap drive development and loading techniques
- Trap chip carrier mounting and fast vacuum interconnects
- Shuttling algorithms for remote loading and entanglement
- Spatially resolved ion addressing and detection

Microtrap Programme

Phase 2: 19–36 months

Phase 2 Build

- Critical review of phase 1 fab & microtrap design and outcomes (by month 20)
- Refined design to preferred suppliers
- Supplier fabrication and supply to partners (by month 27)
- Incorporation of vacuum interface advances, drive and shuttling technology and addressing/detection advances in partner labs
- Entanglement and gate operation demonstrations with various ions
- Consideration of functionality for expanded segment operation and integration into arrays

Input Data for Microtrap design

- Partner existing fabrication activities
- Wider awareness of trapology ideas and techniques through eg trapped ion QC workshops at Michigan, NIST etc
- Emerging QIP techniques

Outputs

- New & focused trap technology
- Publication of results in peer-reviewed journals
- Contribution to global knowledge and fab capability in this area
- Added value to complement international effort in TIQC

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Existing Partner links to fabricators

IOF

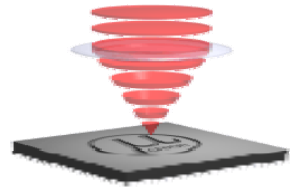
Institut Angewandte Optik und Feinmechanik

Innsbruck

Institut für Festkörper elektronik TU WIEN

Ulm

Micreon GmbH
Ultrafast Laser Processing
...The Next Dimension



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CIP Centre for Integrated Photonics

Oxford

CCLRC

Central Microstructure Facility

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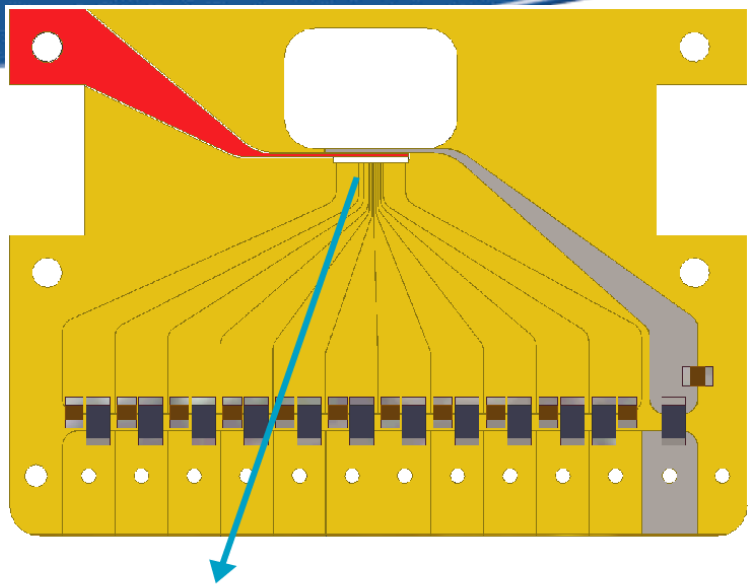
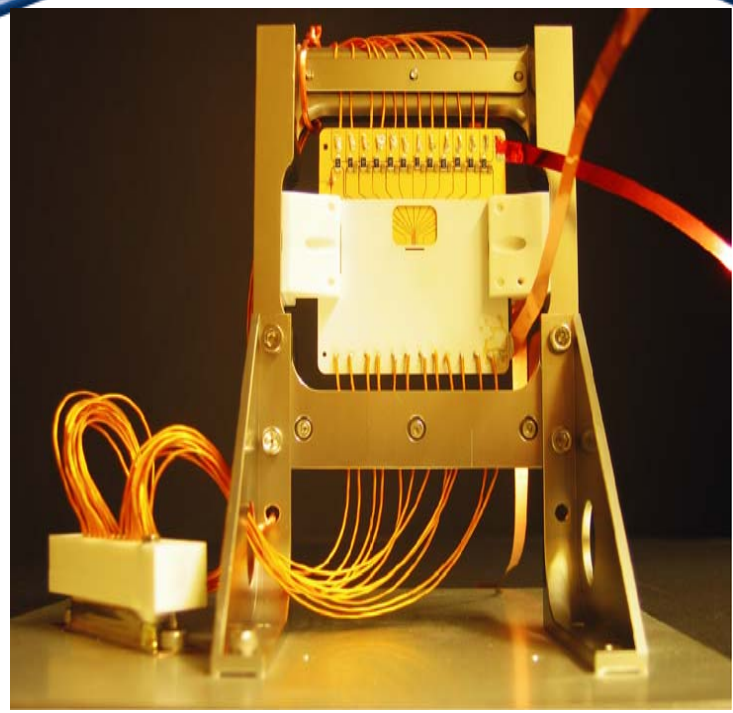
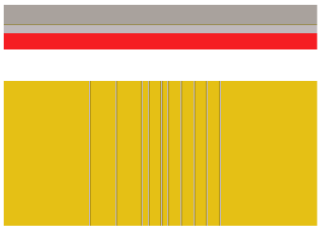
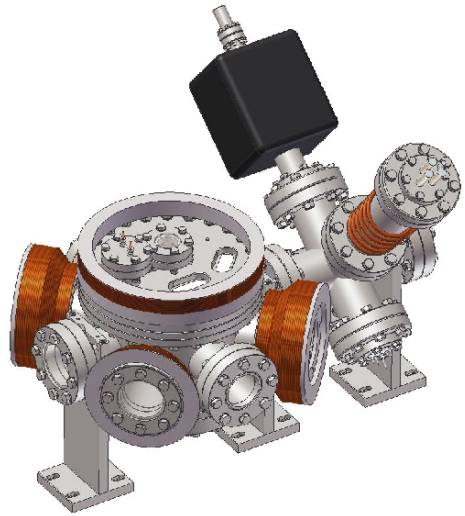
Present chip mounting - Ulm







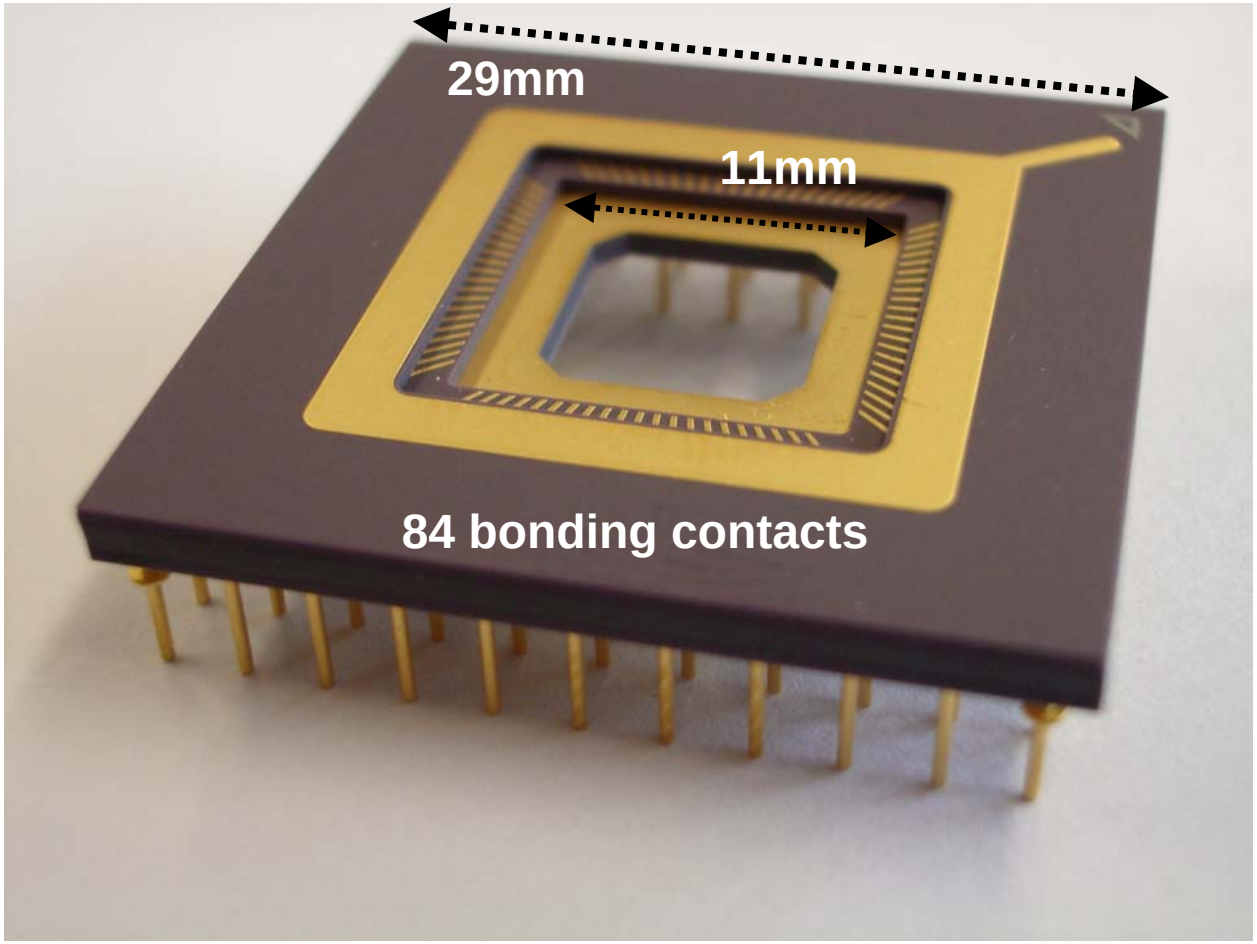
- 11 DC-electrodes
- 1 compensation (grey)
- 1 RF-electrode (red)



Dimensions:

Chip:	35mm x 50mm
Central slit:	5mm x 400µm
Segment widths:	80µm…360µm

chip mounting issues



Chips for segmented two layer traps
- Ulm / Micreon GmbH

Various fabrication methods and materials:

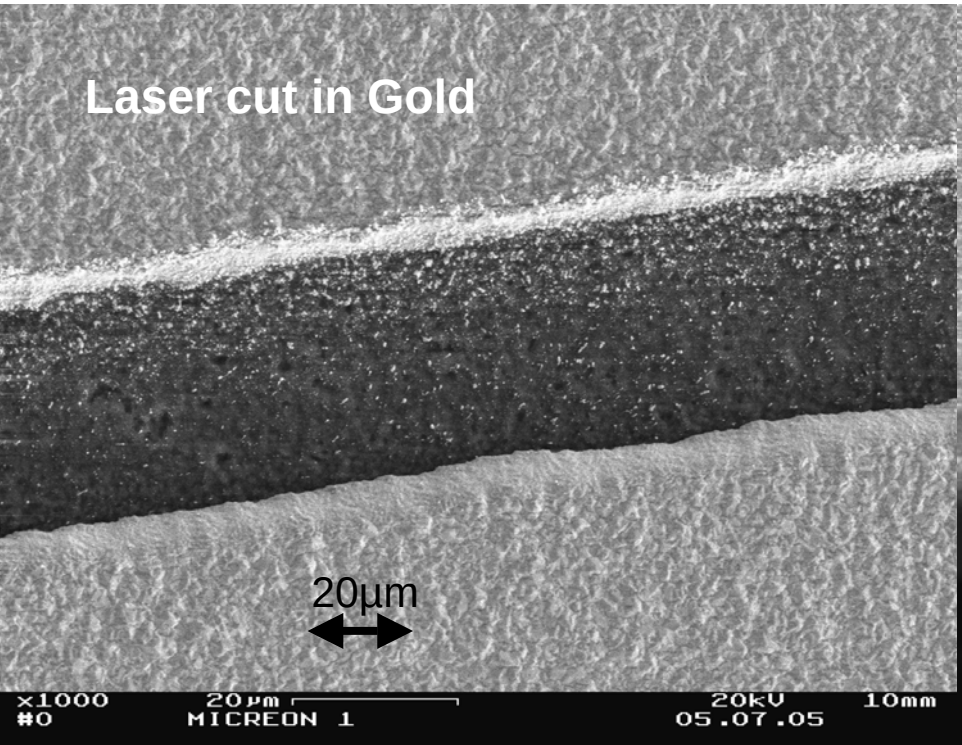
ceramic-gold

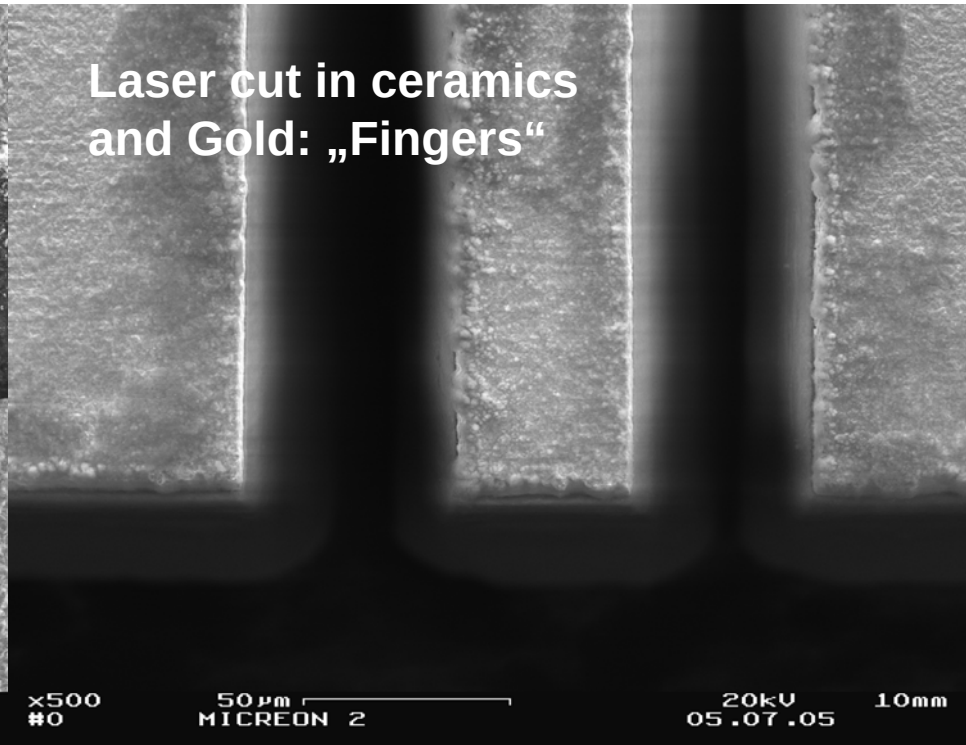
ns-laser cut / ceramic-gold **gaps > 12 µm (old trap)**

fs-laser cut / ceramic-gold **> 5 µm (future trap)**

gold on glass

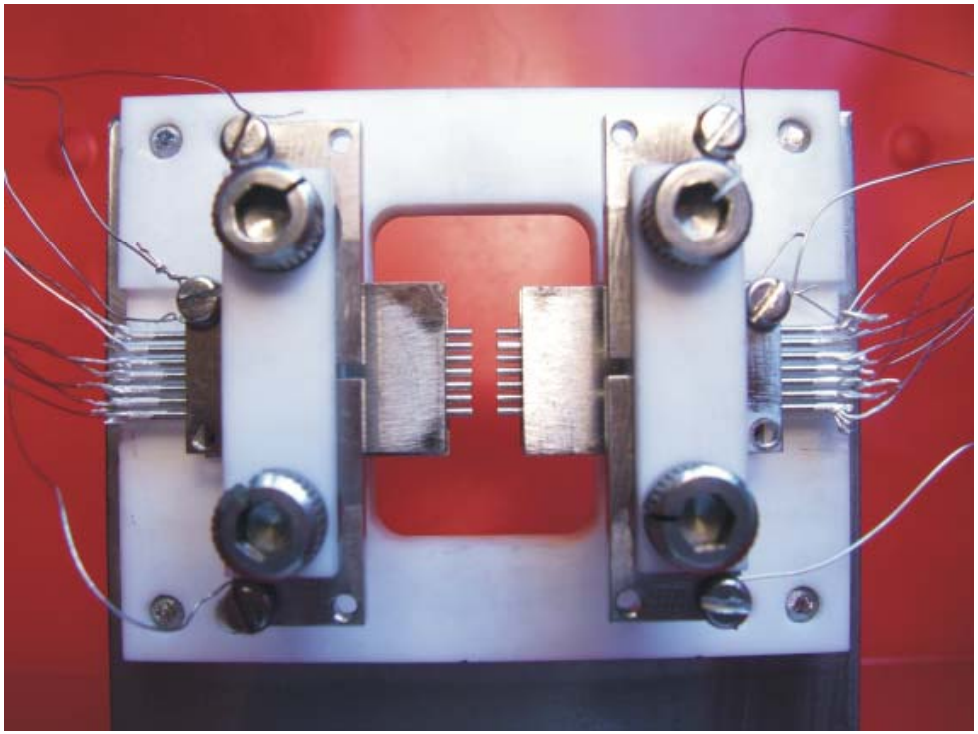
semiconductor carrier material….

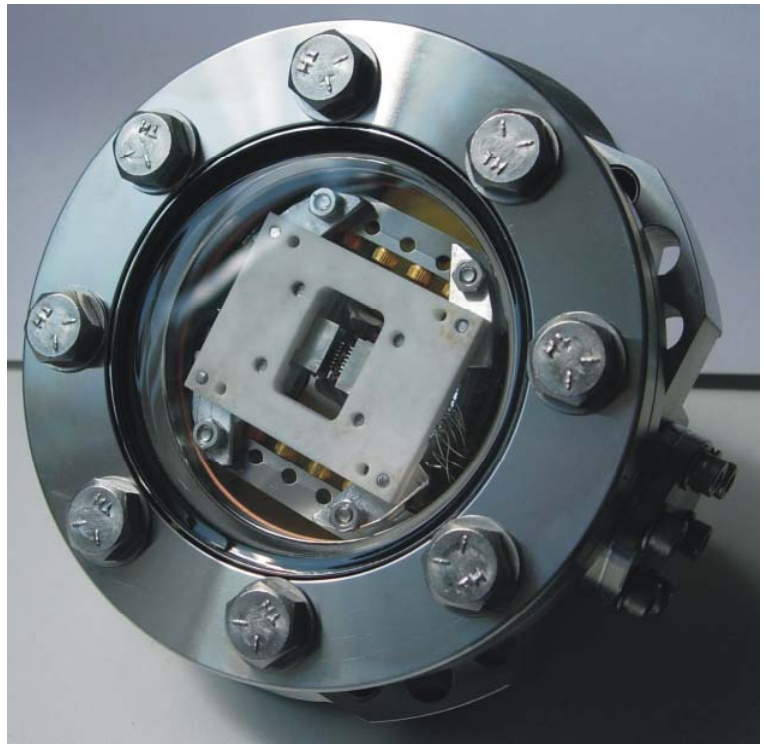




Oxford intermediate design

ion-electrode distance = 0.7 mm
trap-trap separation = 0.8 mm
test open design concept
Built by University of Liverpool (S.Taylor)



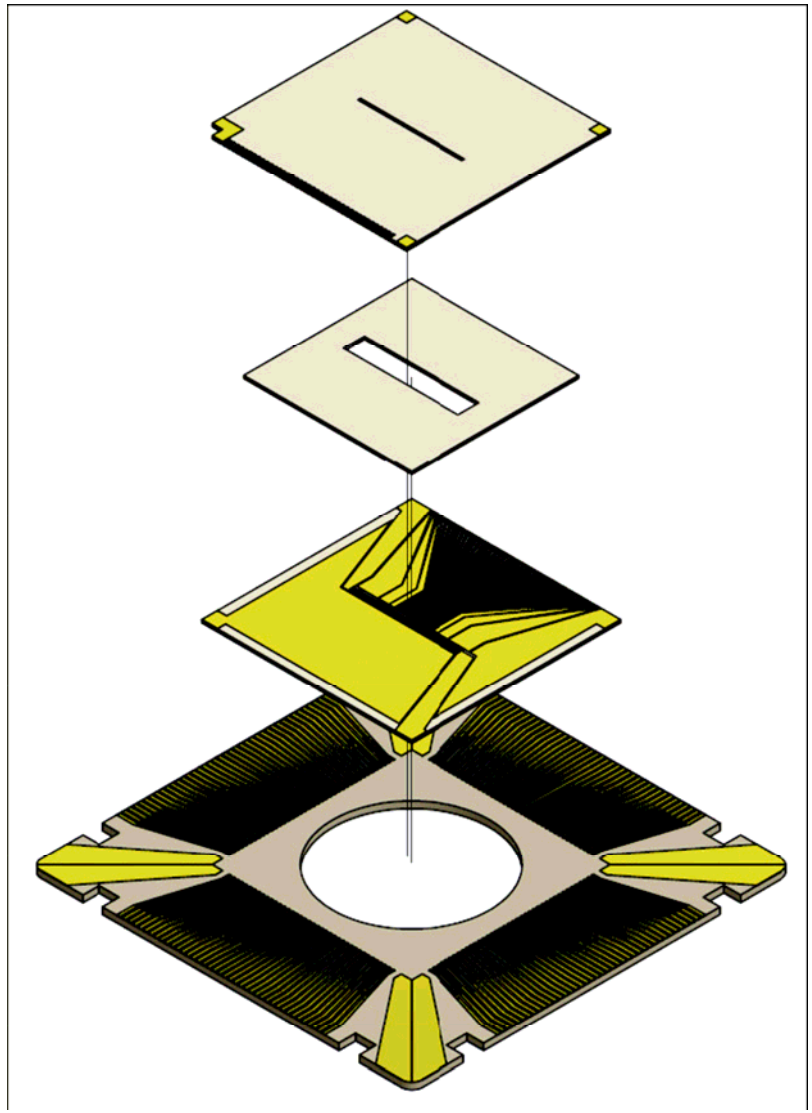


Oxford Physics

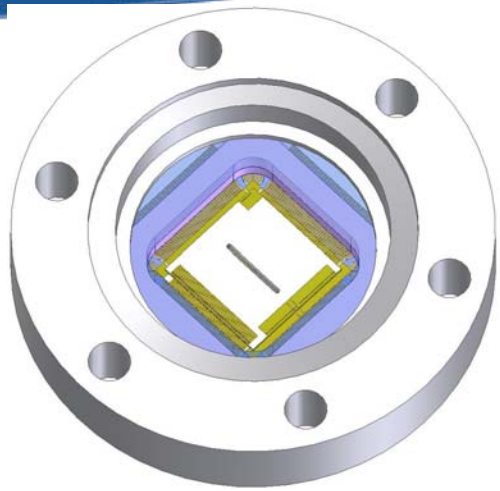
Innsbruck: IOF Fraunhofer Institute, Jena

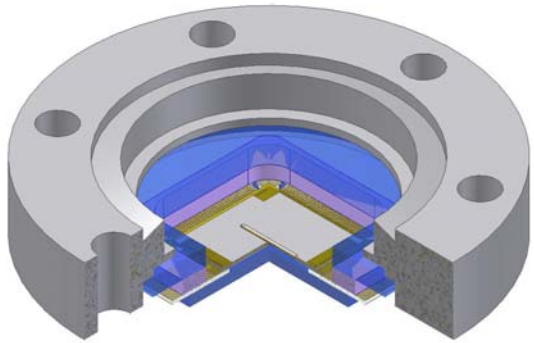
Au on aluminium nitride

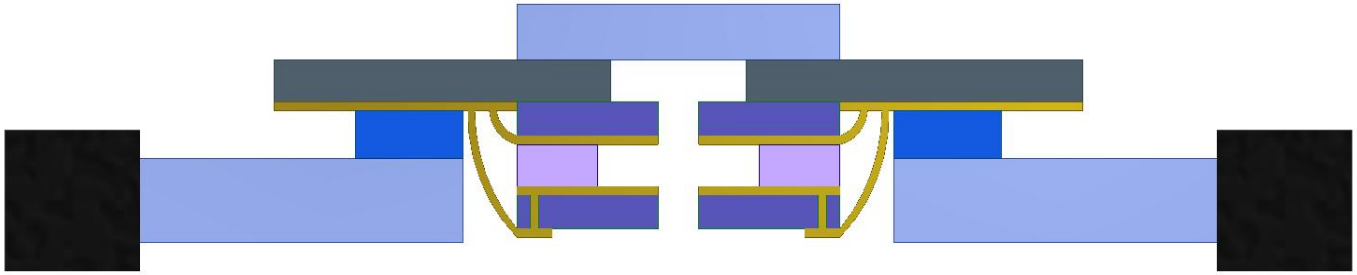
- Top and bottom Ti-Ni-Au coated Aluminium nitride layers
- intermediate Al nitride insulating layer
- alignment with microscopic positioning
- bonded with UHV glue
- similarly bonded to Al-N chip carrier

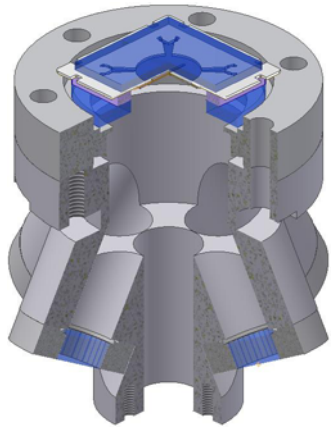


Innsbruck IOF chip-mounting and feedthrough concept



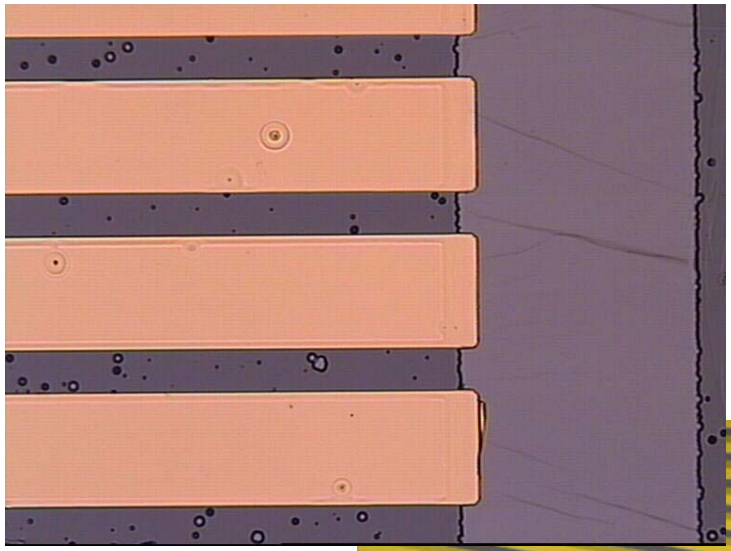


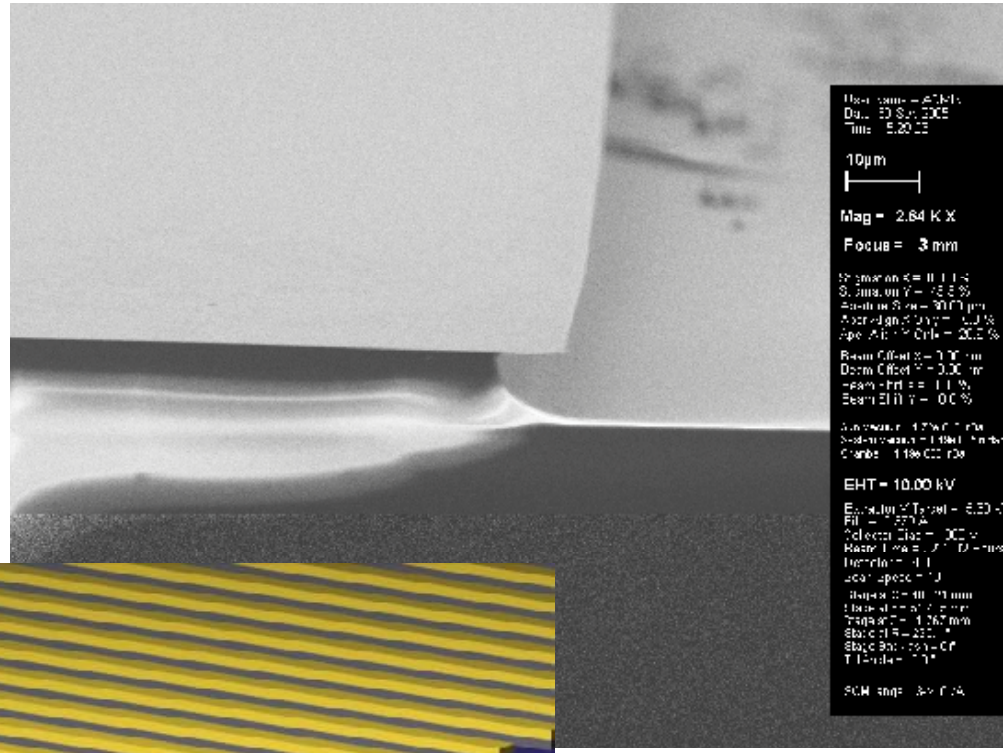


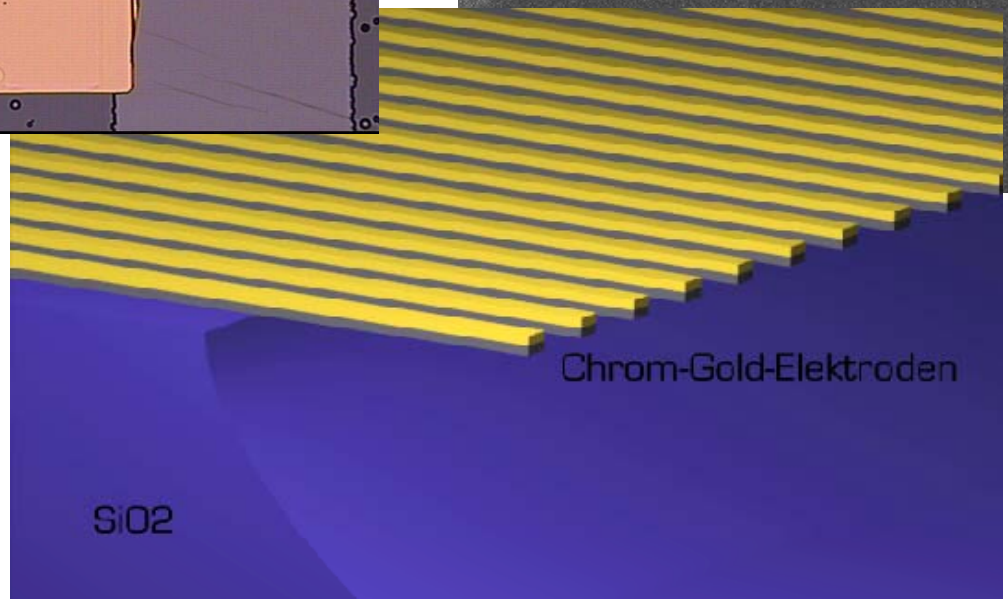


Innsbruck: FKE Vienna

Cr / Au on silica







NPL - CIP Fabrication process
Au-coated silica on silicon

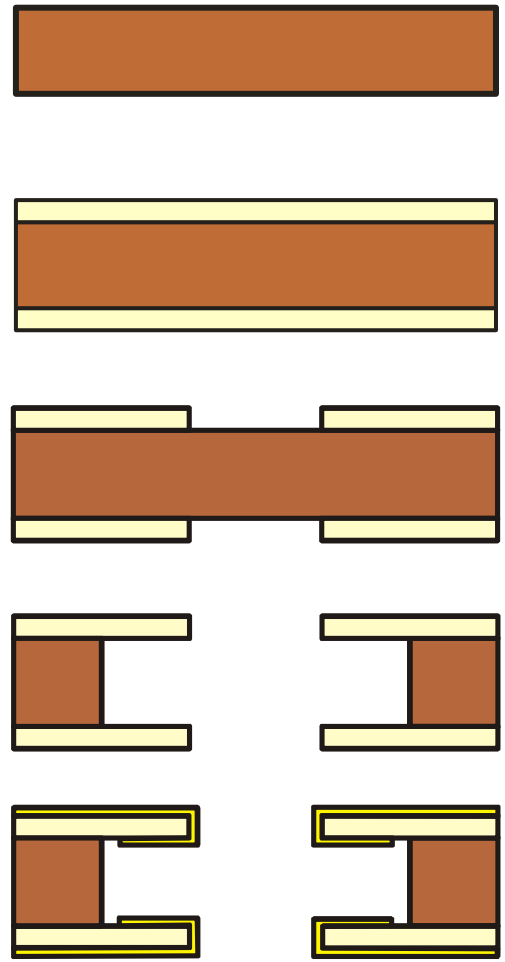
silicon wafer, 500 → 100 μm thick

thermal oxidisation up to 20 μm thick

etch to remove SiO_2:create “fingers”

plasma and wet etches to remove Si

pattern gold electrodes



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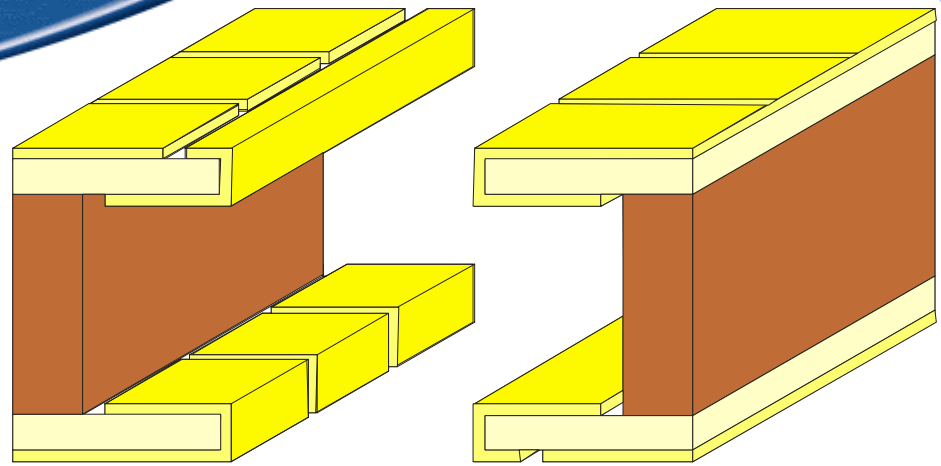
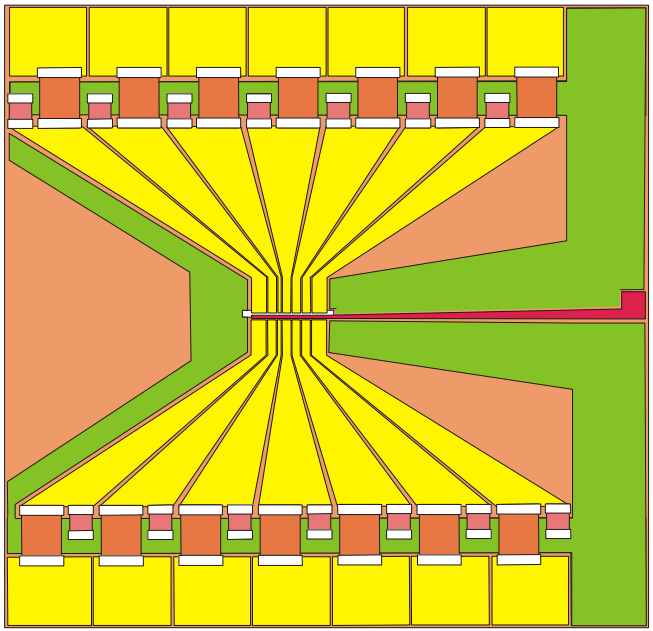
NPL - CIP example trap layout



15 mm x 15 mm chip size,
same pattern on both sides



- DC and compensation electrodes
- RF electrode
- ground
- exposed silica
- resistors
- capacitors

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Aiming to form an effective European partnership

capable of collectively pushing forward trap fabrication processes in a number of ways

capable of contributing to the wider international effort in trapped ion QC.

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