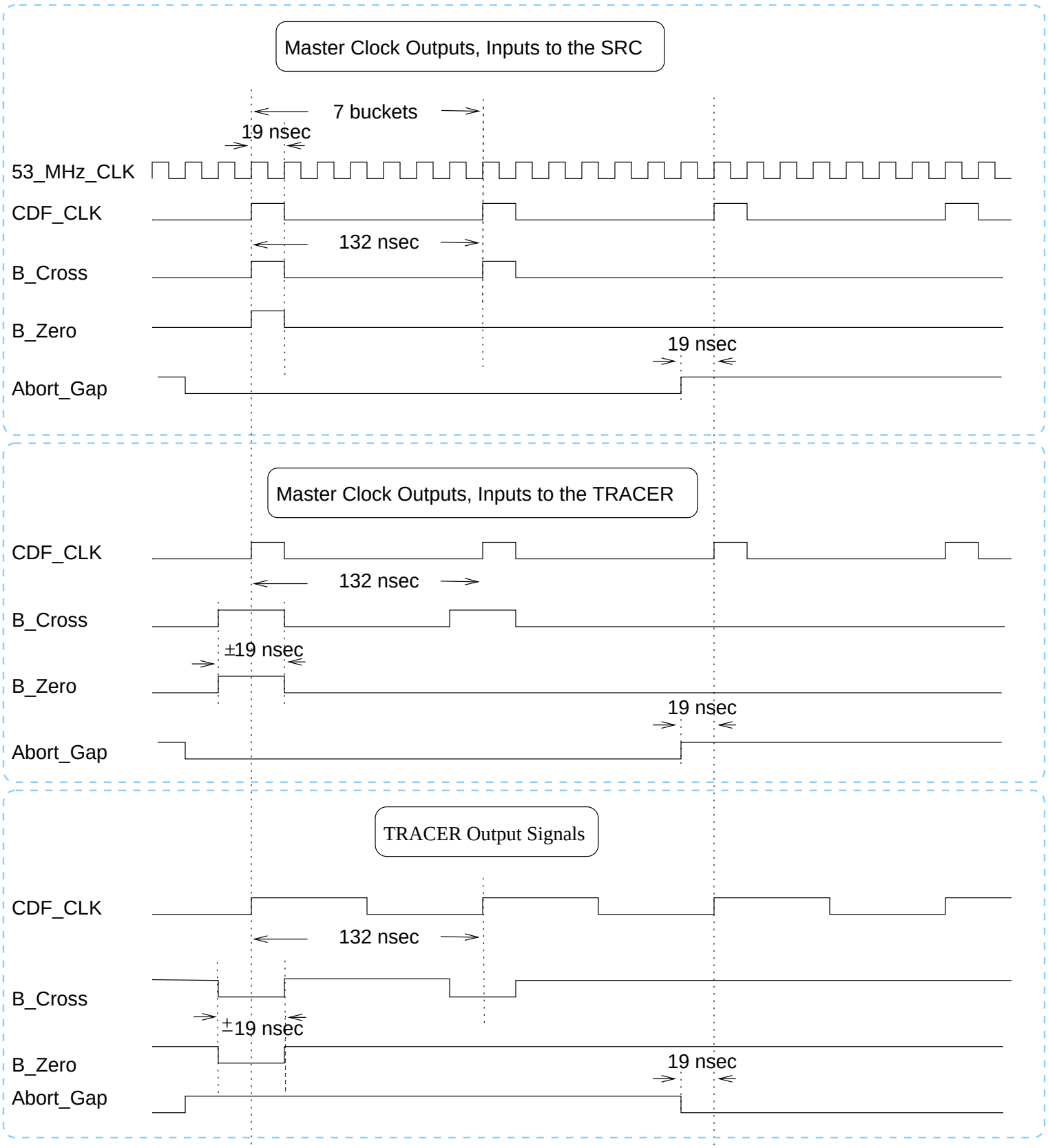
Master Clock Outputs, Inputs to the SRC
7 buckets
19 nsec
53_MHz_CLK
CDF_CLK
132 nsec
B_Cross
B_Zero
19 nsec
Abort_Gap
Master Clock Outputs, Inputs to the TRACER
CDF_CLK
132 nsec
B_Cross
±19 nsec
B_Zero
19 nsec
Abort_Gap
TRACER Output Signals
CDF_CLK
132 nsec
B_Cross
±19 nsec
B_Zero
19 nsec
Abort_Gap