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Linker Chip/Board Design

XFT Mini-Review
December 18, 1996

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Introduction

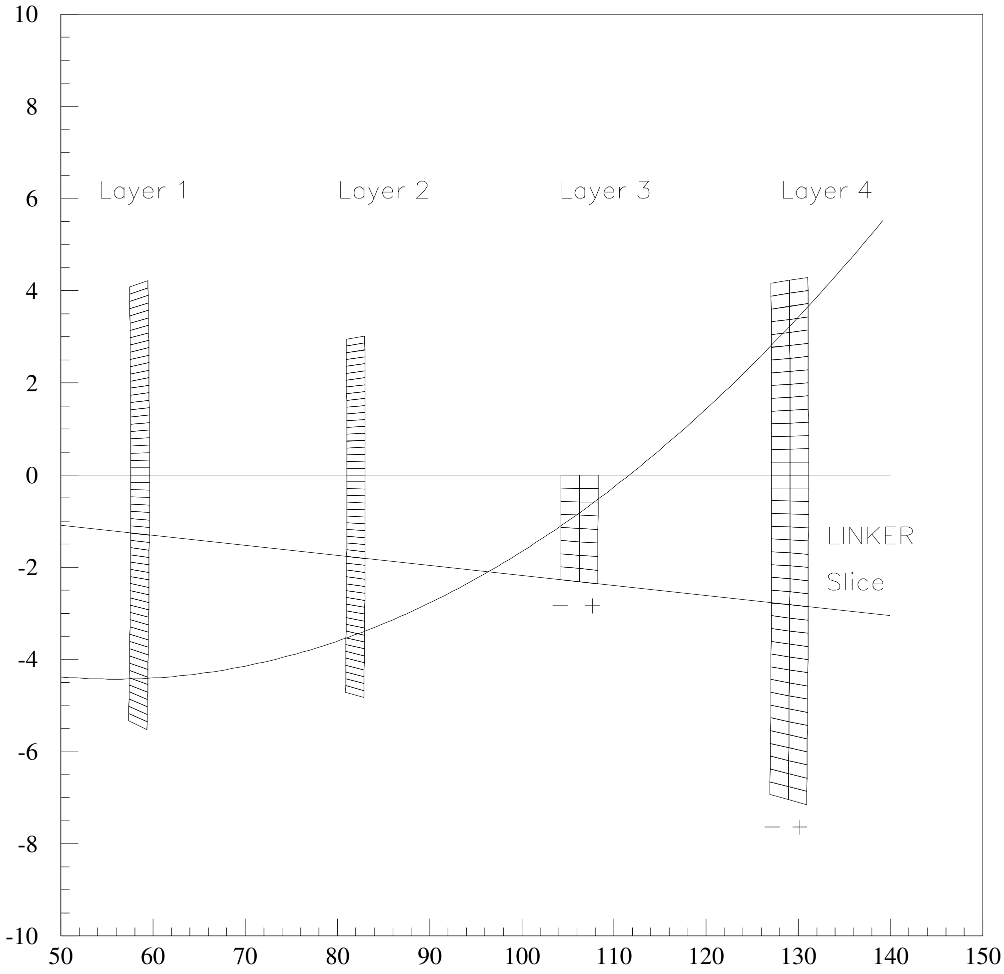
- Task of the Linker:

  The task of the linker is to connect lit pixels between the axial superlayers to find valid tracks. From all valid tracks, the Linker reports the "best track". In addition, in the absence of a four layer track, the Linker will report the "best track" passing through the inner three axial superlayers, if a such a track is found. (See Diagram).

- ϕ Coverage of Linker Chip:
  - Each Linker chip will examine 1.25 degrees of phi.
  - There will be 288 Linker chips in the system.

- ϕ Coverage of Linker Board:
  - Each Linker Board will contain 12 Linker Chips.
  - Covers 15 degrees in phi.
  - There will be 24 Linker boards in the system.

Road Finding in Linker



Inputs to the Linker Chip/Board:

- Each COT cell is providing 12 bits of information. Twelve phi pixels for the inner two axial layers. For the outer two axial layers there are two sets of 6 phi pixels, one set for tracks with positive slope and one set for negative slope.
- Because of track curvature, each chip needs many more pixels than those contained within 1.25 deg (see picture). A total of 212 pixels must be input to each chip. Many pixels get used by several Linker chips.
- A Linker board gets all the pixel information from 21 Finder chips. (A total of 1008 bits of information).

Output of Linker Chip/Board:

- Each Linker reports the best track which passes through its 1.25 deg slice, as measured at third axial layer.
- Often a track near the edge of a linker chip will be found by the neighbor linker chip as well. *Within* a Linker *board* we plan to remove these duplicate tracks. *Between* Linker boards the XTRP is expected to remove these tracks.
- The format of the information sent to the XTRP in 7.5 degree slices (2 cables per Linker Board) in 4 words, each sent in 33 ns.

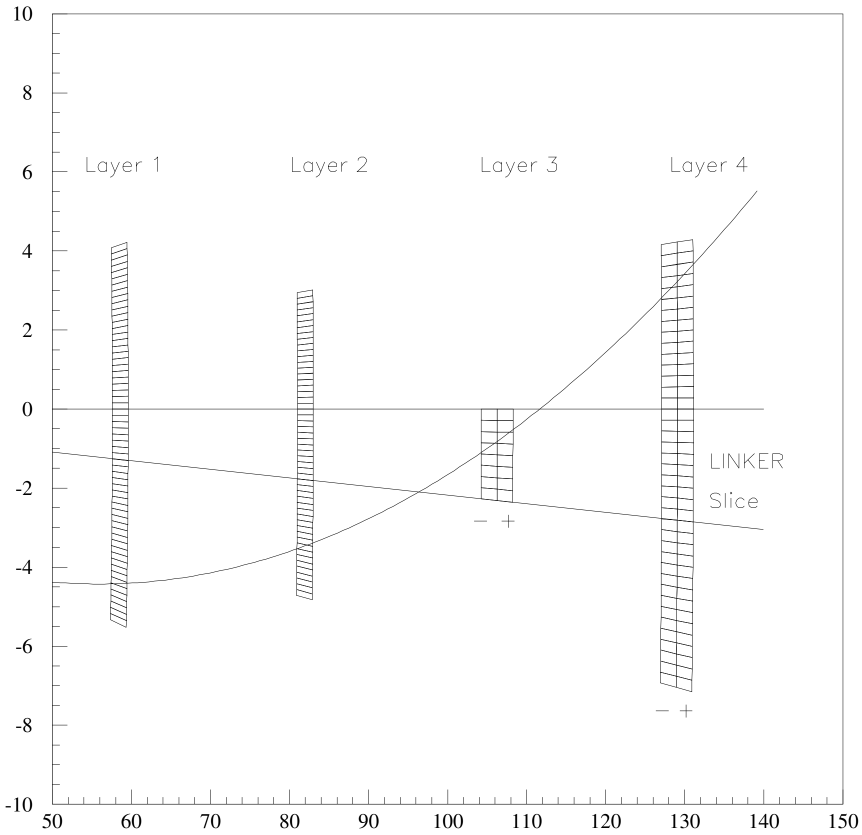
w1: Mk(2), B0(1), Ph1/S/I/X/SP (7), Ph2/S/I/X/SP (7), Ph3/S/I/X/SP (7), SP(1)
w2: Mk(2), B0(1), Pt1 (7), Pt2 (7), Pt3 (7),SP(1)
w3: Mk(2), B0(1), Ph4/S/I/X/SP (7), Ph5/S/I/X/SP (7), Ph6/S/I/X/SP (7), SP(1)
w4: Mk(2), B0(1), Pt4 (7), Pt5 (7), Pt6 (7),SP(1)

Progress in Chip Design Since last Mini-Review

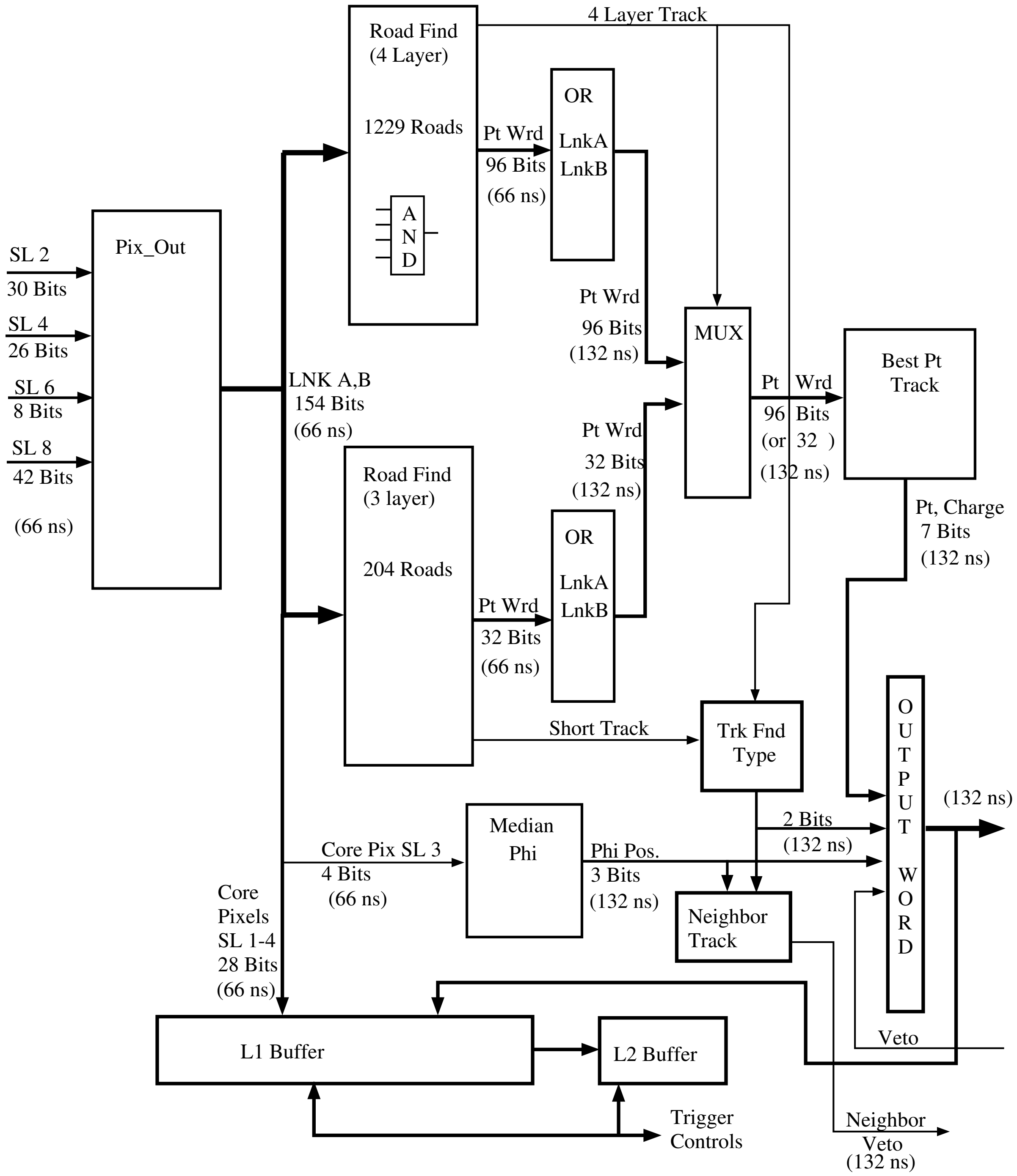
- Design has stabilized.
- Implemented 12 pixel input.
- Implemented a short track (3 inner layers) into the design.
- Design implemented in ALTERA 10K50. Currently running test vectors.
- Tested portions of logic in ALTERA 10K20.
- Preparing to test full design in ALTERA 10K50 (more below).

Linker Chip Design

- Design has been implemented in a PLD (ALTERA 10K50) using ALTERA software design tools.
- The Linker requires 2458 4-layer roads and 408 3-layer roads.
- We have taken advantage of a two fold symmetry to reduce the number of roads which must be implemented in the chip. (1229 4-layer roads and 204 3-layer roads).
- The 4-layer tracks are sorted into 96 bins of Pt (48 for each charge) while the 3-layer tracks are sorted into 32 bins (16 for each charge).
- With 12 bits/cell from the Finder, the Linker has 212 inputs (106 every 66 ns).



Linker Chip Block Diagram



Results of Fits and Simulations

- The Linker fits into a 10K50 and uses 2550 logic elements (88 % of available LE). It uses 8448 bits of memory (41% of available).
- It uses 163 of the 189 available I/O pins.
- From the beginning of the data entry to the output requires four 132 ns clock ticks. (An additional tick is required to send the data to XTRP).
- We have run (and continue to run) test vectors through the simulation.
- We have written a FORTRAN (sorry it's not C++) Hardware simulation for the Linker chip. We are using this to check the results of complex test vectors.

Test Boards

Test Board 1:(Oct-Sept 1996)

- Small board with a single 10K20 (1,152 LE).
- Provided important initial experience with ALTERA FLEX 10K series. (Learned how to download and run).
- Implemented portions of the Linker design in the 10K20. (e.g. Road finding for roads with just the "core" pixels.)

Test Board 2:

- Much more complex board (See Block Diagram).
- Uses a 10K50 for full FINDER and LINKER Chip testing.
- Has a VME interface.
- Uses 10K20 as input and output buffers to test large numbers (256) of test vectors at (or near) speed.
- Layout of board near completion. We hope to go out for board fabrication before the holiday break.
- Two boards will be fabricated (one stationed at FNAL and the other at OSU).
- Testing with this board will begin in January.

BLOCK Diagram of Test Board 2:

Summary and Future Direction

- The design of the Linker has stabilized.
- It has been implemented in an ALTERA 10K50.
- We are testing and refining the linker design using ALTERA software.
- Plan testing of the FINDER and LINKER design with Test Board 2 (January-March).
- Design and Construction of Prototype Linker Board by early June for an XFT system test with the goal of having the XFT in the vertical slice test by August 1997.