Test set-up

- TESTCLK provides 132 ns clock
- TRACER provides calibration pulses
  - after each 100 pulses fine delay incremented
  - after each 1000 pulses coarse delay incremented
  - total of 10000 pulses at 100 points in time

For each channel of TDC, check:

- output width
- output start time
- linearity of response

Checks done with 1 TDC in crate and with up to 11 TDC's in crate

For now, reference everything to first channel

Remaining Issues

- Channels with no output
- “Out of phase” output

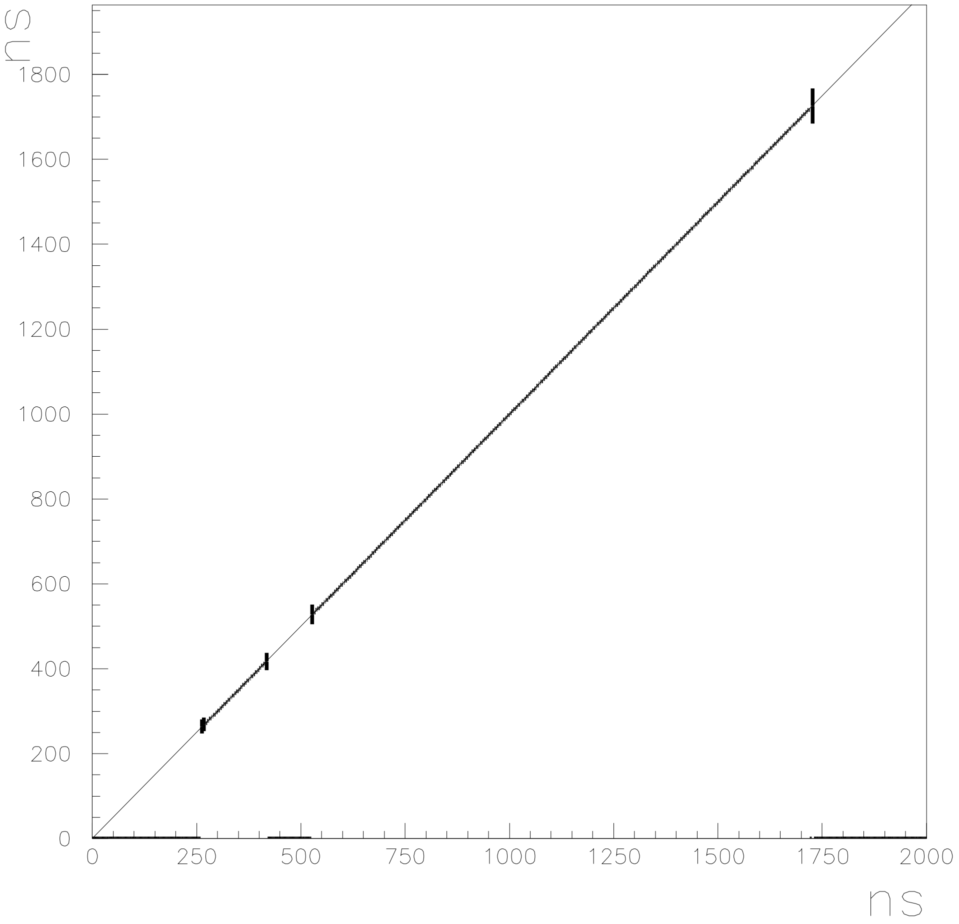
Channels with no output

- Some channels gave no output for all 10000 events.
  - Problem independent of # of TDC's in crate - these channels are most likely "dead".
- Occasionally ch. 6 and 7 would give no output.
  - Problem traced to lack of termination of Level 1 accept. Problem went away after resistors added to board.

- **Occasionally most of the channels for a given cycle would have no output.**
  - **Effect went away when TRACER was moved. Problem most likely due to known clock problems.**

- **Ch. 72 gives no output when TDC is in slot 15 or 16.**
  - **Is this a TDC problem or crate problem?**

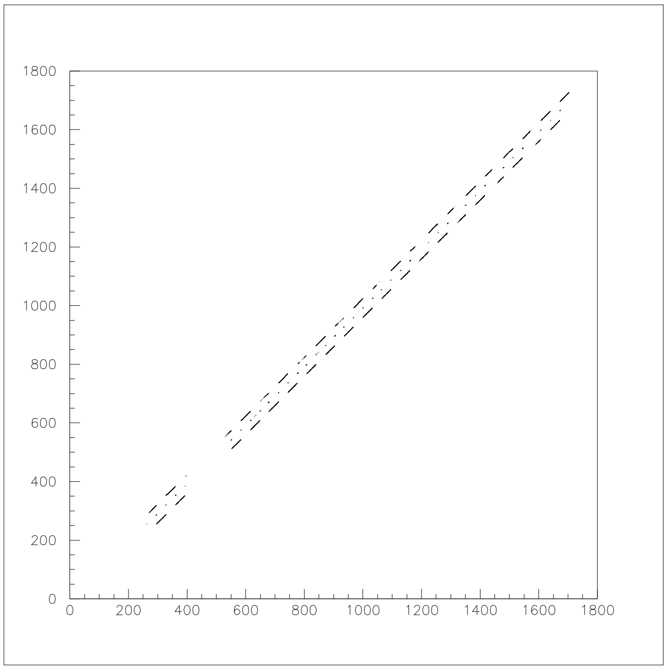
Now, study the "Out of phase output" problem



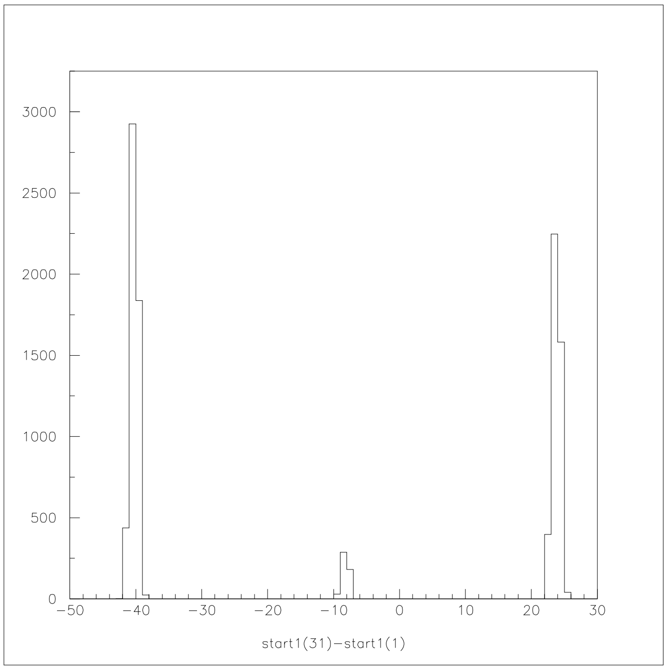
1 TDC case, channel 11

$T_{\mathrm{start}_{11}}$ vs. T_{start_1}

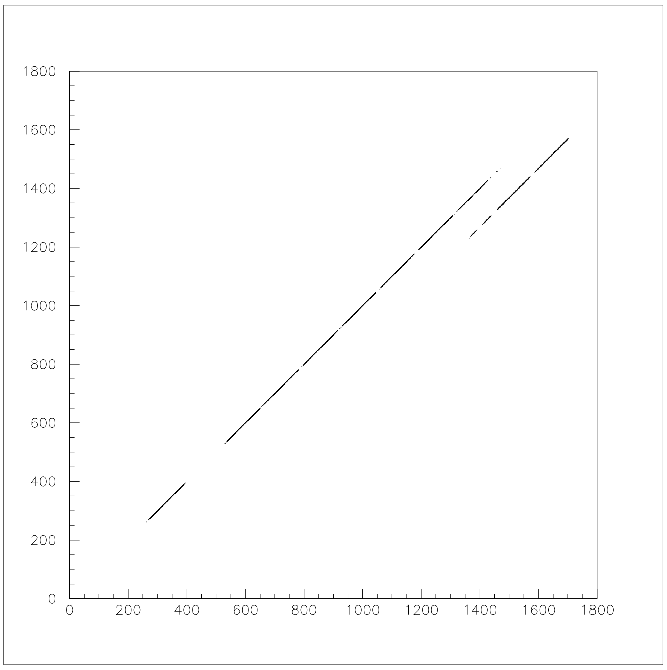
This is what we want



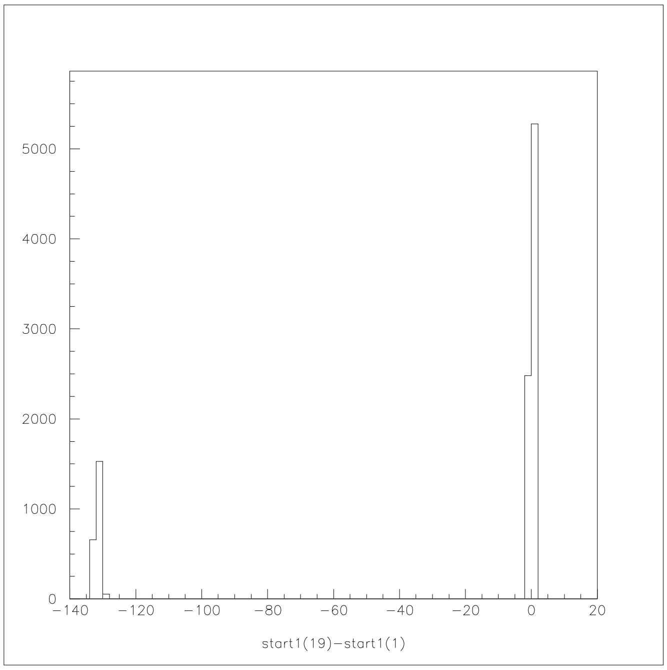
Slot 11, TDC 0030



Output seperated by 66 ns i.e. 1/2 clock cycle



Slot 14, TDC 0026



Output seperated by 132 ns i.e. 1 clock cycle

The "132 ns" problem

- May be due to a bad L2 buffer address, arising from lack of termination.
- If a bit is lost, data intended for L2B1 may be written to L2B0. The data would be 132 ns out of phase.
- Will study by modifying readout code to give data in all 4 buffers.