Characteristic Impedance Measurement of Planar Transmission Lines*

Uwe Arz(1) , Dylan F. Williams(2), and Hartmut Grabinski(3)

(1) Physikalisch-Technische Bundesanstalt, Section 2.22, POB 3345, 38023 Braunschweig, Germany
E-mail: uwe@ieee.org

(2) National Institute of Standards and Technology, Mailstop 813.01, 325 Broadway, Boulder, CO 80305, USA
E-mail: dylan@boulder.nist.gov

(3) Laboratorium für Informationstechnologie, Universität Hannover, Schneiderberg 32, 30167 Hannover, Germany
E-mail: hgra@lfi.uni-hannover.de

ABSTRACT

In this paper we investigate a simple, robust and general method to determine the characteristic impedance of planar transmission lines based on calibration comparison. We apply the method to different types of planar transmission lines such as CPW and microstrip on lossless substrates, and to lines on lossy silicon typical of high-speed interconnects including VLSI interconnects.

INTRODUCTION

We investigate the performance of the calibration comparison method for characteristic impedance determination, which is based on the calibration comparison method of [1] and was introduced in [2] and [3]. We demonstrate the method for different types of planar transmission lines, including VLSI interconnects built in CMOS technology.

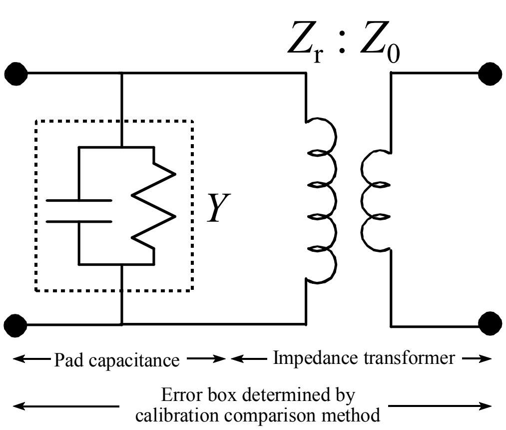

Fig. 1. Equivalent circuit model of error boxes determined by the calibration comparison method of [1].

The method begins with a first-tier multiline TRL calibration [4] in a set of easily characterized reference lines. The reference impedance Z_r of this calibration is set to 50 Ω using the method of [5], plus a transmission-line capacitance measurement of a resistor [6]. The reference plane is moved back to a position close to the probe tips. Then, a second-tier multiline TRL calibration in the transmission lines of interest is performed, yielding error boxes that relate the second-tier to the first-tier probe-tip calibration. References [2] and [3] suggest modeling these error boxes with the equivalent circuit shown in Fig. 1, from which a simple and robust estimate of characteristic impedance can be derived that is insensitive to contact-pad parasitics.

The model of Fig. 1 consists of a lossy shunt contact-pad with admittance Y followed by an impedance transformer mapping the reference impedance Z_r of the probe-tip calibration into the reference impedance Z_0 of the second-tier TRL calibration.

When transition parasitics are dominated by contact-pad capacitance and conductance, the error box X' measured by the calibration comparison method will be approximately equal to X. The transmission matrix X of the circuit in Fig. 1 is

---

$$X = \frac{1}{\sqrt{1-\Gamma^2}}\begin{bmatrix}1 & \Gamma\\ \Gamma & 1\end{bmatrix} + \frac{YZ_r}{2}\begin{bmatrix}-1 & -1\\ 1 & 1\end{bmatrix}, \text{ where } \Gamma \equiv \frac{Z_0 - Z_r}{Z_0 + Z_r}.$$ The estimate $\Gamma_1 \equiv \sqrt{\dfrac{(X_{12}' + X_{21}')^2}{4 + (X_{12}' + X_{21}')^2}}$, derived from this model, can be shown to be insensitive to the contact-pad admittance Y and is used to determine Z_0.

PLANAR TRANSMISSION LINES ON LOSSLESS SUBSTRATES

First, we apply this characteristic impedance measurement method to transmission lines built on lossless substrates. In this case, the reference method of [5] can be applied to determine the characteristic impedance directly from the propagation constant measurement, which can be measured very accurately using the multiline TRL method [4].

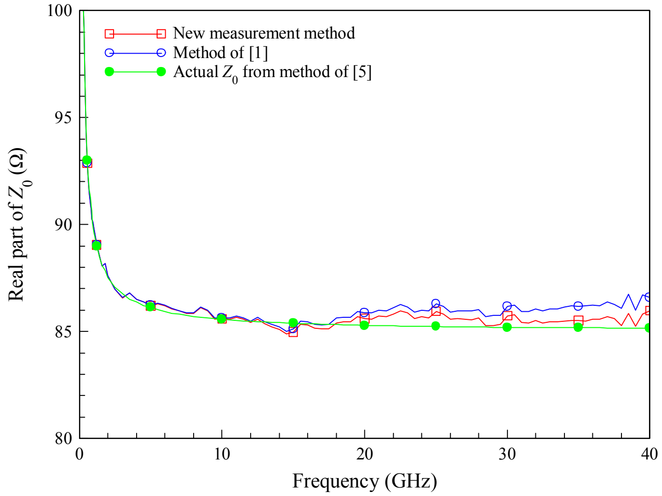

Fig. 2. Real part of the characteristic impedance Z_0 of a CPW built on a fused silica substrate. The plotted data is from [3].

Fig. 2 shows the real part of the characteristic impedance Z_0 of a coplanar waveguide built on a fused silica substrate, measured with different methods, and compared to the accurate method of [5]. The results of Fig. 2 show that the calibration comparison method for characteristic impedance determination agrees well with the reference method of [5] and performs slightly better at higher frequencies than the characteristic-impedance estimate proposed in [1].

Next, we investigated the performance for microstrip lines built in a semi-conductor technology with a feature size of 2 µm. The 6 µm wide signal conductor was built in the second metal level, while the ground metallization plane was built in the first level of metal and connected to the silicon substrate with ohmic contacts.

Because the silicon oxide between the two metal layers had very low loss, the capacitance C per unit length was constant with frequency and the conductance G per unit length negligible. We used a value of $C \approx 3.29$ pF/cm to determine the characteristic impedance Z_0 with the very accurate method of [5] from the propagation constant γ and C.

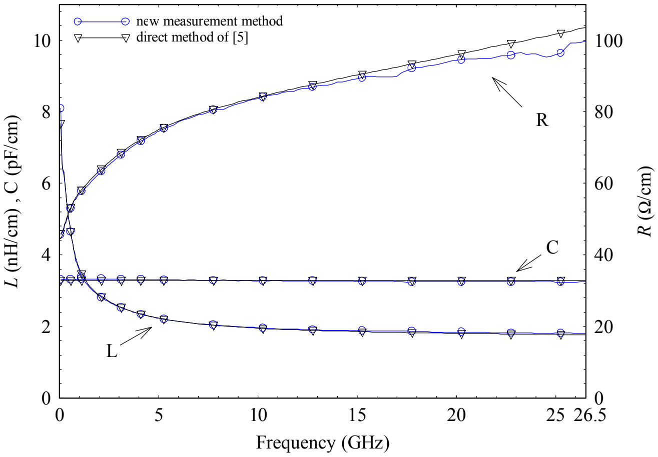

Fig. 3. Resistance, capacitance and inductance per unit length of the 6 µm wide microstrip lines. The plotted data is from [7].

Fig. 3 shows that the three relevant line parameters per unit length R, L, and C derived from γ and the two different Z_0 measurements agree well in the frequency range from 0.05 to 26.5 GHz.

Both the results obtained from measurements of a coplanar waveguide and a microstrip line demonstrate that the calibration comparison method for characteristic impedance determination is in good agreement with the reference method of [5].

HIGH-SPEED DIGITAL INTERCONNECTS ON LOSSY SILICON

Next, we investigated transmission lines built on lossy silicon substrates. Several substrate conductivities and line geometries were available for experiments. Figures 4 and 5 show the inductance and capacitance per unit length calculated from γ measured by the multiline TRL method [4] and Z_0 measured by the method of [2,3]. The results were compared against the quasi-analytic calculations of frequency-dependent transmission line parameters of [8] and agree closely over a broadband frequency range. Besides reproducing the prediction of the calculations of [8], the measurements also demonstrate the strong influence of the substrate on the transmission line properties.

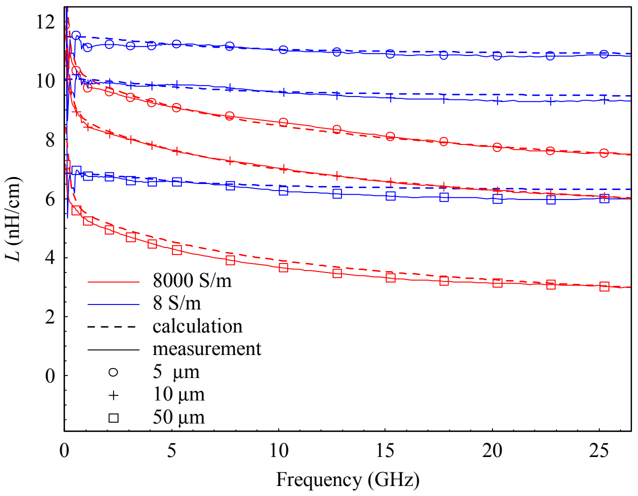

Fig. 4. Inductance per unit length of interconnects built on lossy silicon substrates.

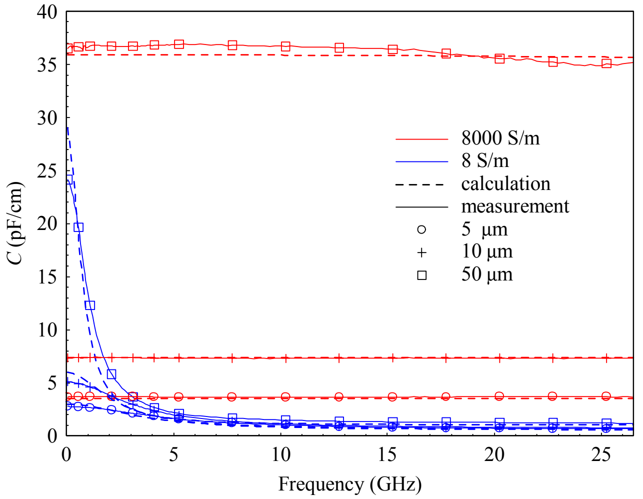

Fig. 5. Capacitance per unit length of interconnects built on lossy silicon substrates.

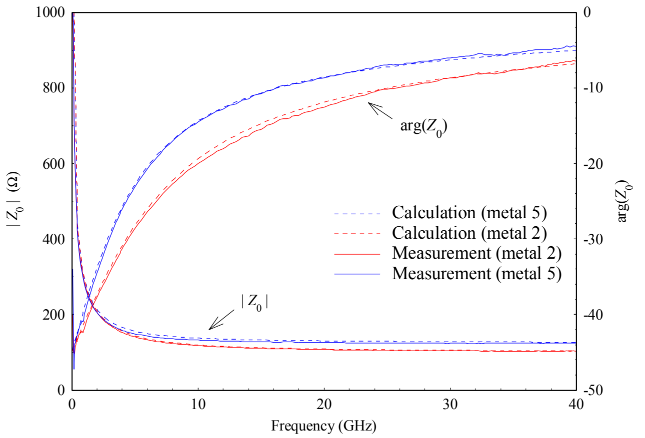

Fig. 6. Characteristic impedance of 1 µm wide lines built in different metal levels of a 0.25 µm CMOS technology.

Finally, we applied the method to measure the characteristic impedance of 1 µm wide interconnects built in the second and fifth metal level of a six-metal-level 0.25 µm CMOS technology (Fig. 6). Again, the quasi-analytic calculations of [8] were used for comparison and show a very good agreement over a frequency range of 40 GHz. The influence of the substrate skin effect on the transmission line parameters also becomes evident for these VLSI interconnects and is significantly more pronounced for the lines built in the second metallization layer, which is closer to the substrate surface.

REFERENCES

[1] D.F. Williams, R.B. Marks, and A. Davidson, "Comparison of On-Wafer Calibrations," *38th ARFTG Conf. Dig.*, pp. 68-81, Dec. 1991.

[2] U. Arz, D.F. Williams, and H. Grabinski, "Accurate Characteristic Impedance Measurement on Silicon," *2nd IEEE Workshop on Signal Propagation on Interconnects*, Digest of Abstracts, May 1998.

[3] D.F. Williams, U. Arz, and H. Grabinski, "Accurate Characteristic Impedance Measurement on Silicon," *IEEE MTT-S Symp. Dig.*, pp. 1917-1920, June 9-11, 1998.

[4] R.B. Marks, "A Multiline Method of Network Analyzer Calibration," *IEEE Trans. Microwave Theory and Tech.*, 39(7): pp. 1205-1215, Jul. 1991.

[5] R.B. Marks, D.F. Williams, "Characteristic Impedance Determination using Propagation Constant Measurement", *IEEE Microwave Guided Wave Lett.*, vol. 1, no. 6, pp. 141-143, June 1991.

[6] D.F. Williams and R.B. Marks, "Transmission Line Capacitance Measurement," *IEEE Microwave Guided Wave Lett.*, vol. 1, no. 9, pp. 243-245, Sept. 1991.

[7] U. Arz, D.F. Williams, and H. Grabinski, "Experimental Study of the Ground Plane in Asymmetric Coupled Silicon Lines," *EPEP 2001 Conf. Proc.* , pp. 317-320, Oct. 2001.

[8] E. Grotelüschen, L.S. Dutta, S. Zaage, "Quasi-analytical Analysis of the Broadband Properties of Multiconductor Transmission Lines on Semiconducting Substrates," *IEEE Trans. Comp., Packag., and Manufact. Tech.-Part B*, 17: pp. 376-382, Aug. 1994.