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Engineering Note

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Subject: Installing and Configuring VeriBest & Microstation CAD software on Windows 95 & NT

You will first install the VeriBest software from a remote computer. Once you install the software, you will need a "seed job" to get started with schematic entry and PCB layout. The "seed job" contains file pointers, templates, initial settings, and parts libraries. You will copy a "seed job", including a complete set of libraries, into a job directory for each new job. If you need to make new parts, you will put them in your own special local library within your job directory. You may carry this special library forward to each new project. You may also submit new parts to the Division VeriBest guru to be included in the seed libraries. Tom Wesson (X2948) is the guru and he graciously answers all VeriBest questions. Dave Huffman (X2273) can also answer VeriBest questions. This note covers getting started with schematic entry and printed circuit board design. Simulation, PLDs and FPGA design can be implemented after a working knowledge of these tools is acquired. VeriBest is difficult to get started with; but it is our only option if we are to do complex hierarchical group projects.

VeriBest Installation:

1. You will need the following platform capability to install and run the VeriBest software:
   - Windows 95 – Schematic entry only
   - Windows NT – Schematic entry and printed circuit board design
   - 200-400 megabytes of free disk space.
2. Run the VeriBest installation program setup.exe located at:
   - Domain Rd_floral \\ACME\VeriBest\Vb98A
   - Use the suggested default directory if possible to minimize later reconfiguring.
   - Select "VeriBest Design Capture" and, if you have Windows NT, "VeriBest PCB". Ignore all other components.
3. Place a shortcut on your desktop to the VeriBest user's manuals located at:
   - Domain Rd_floral\\Acme\Veribest\VB98a_docs\start.htm.
4. If you have Windows NT, and have installed VeriBest PCB, then run the Microstation installation program located at:
   - Domain Rd_floral \\Acme\Veribest\U_Station\ENGLISH\Intelnt\Ms95\Disk01\Setup32.exe.
   - Leave the default path designation, or set to another location as desired.
   - Select "minimum" installation.
5. For Windows 95 add the following to the autoexec.bat file:
   - set LM_LICENSE_FILE=7329@acme
6. For NT add the following to the System Properties/Environment Variables:
   - Variable LM_LICENSE_FILE
   - Value =7329@acme
7. Reboot your computer to activate these autoexec/environment changes.
8. From the Start menu, run "MicroStation 95" and supply the following initialization information when requested:
   - Your Name: Fermi National
   - Organization: Fermi National
   - Serial Number: 20006378700669
   - License Number: 2772648208

Installing a Seed Job:

Veribest uses "seed jobs" to start a project. A seed job contains an empty schematic and PCB; file pointers and libraries; and has some of the initial schematic and PCB settings already made. I have placed three VME seed jobs on my computer (DMACS domain, D0-rickh\\Shared\). These seed jobs originated with PPD/EET/EES. I have restructured the files and file pointers within these seeds to comply with VeriBest recommended practice. Otherwise these seeds are as used by Tom Wesson to produce many PCBs. One of the seeds is for a Standard 6U VME card, another is for a 9U VME-P card, and the third is for a 9U VME-P transition card. They are usefull especially for VME design because the connectors are placed and the board details are predrawn to specifications. The 9U seed has a VME slave interface based on a Xylnix FPGA. These are flat, multisheet designs and should be made hierarchical if they are used in DZERO projects. You may delete or convert any uneeded circuitry before entering your own schematics. The libraries in these seeds were developed by Wesson et. al. I also include a fourth seed (D0Seed). D0Seed job contains ALL of the part libraries, symbol libraries, cells, pads and pins as delivered by VeriBest. The unneeded libraries may be deleted from your job to reduce disk space and increase performance. As you become more skilled with the tools, you will be able to use parts, symbols, cells, pads etc. from any of the jobs or from other sources. The following information assumes that D0Seed from my directory is used:

9. Create a new directory on your computer for the job. For example D:\Testjob

10. Copy the contents of the seed job into your new directory. For example:
    - From > d0-RickH\\Shared\D0seed\Seed.prj To > D:\Testjob\Seed.prj
    - From > d0-RickH\\Shared\D0seed\library To > D:\Testjob\library
    - From > d0-RickH\\Shared\D0seed\vbdc To > D:\Testjob\vbdc
    - From > d0-RickH\\Shared\D0seed\vbpcb To > D:\Testjob\vbpcb

Configuring the Design Capture Program:

The seed job is now in place and ready to be configured so that schematic entry can begin. Configuration is very important, so follow the directions carefully.

11. Using Windows Explorer, rename the seedjob's .prj file to whatever you wish for your new project. The prj file is located in your new directory. For example:
    - From > D:\Testjob \seed.prj To > D:\Testjob \testjob.prj

12. Using Windows Explorer, rename the seedjob's .sbk file (schematic) to whatever you wish for your new project. The sbk file is located in your new \vbdc sub-directory. For example:
    - From > D:\Testjob \vbdc\Seed.sbk To > D:\Testjob \vbdc\testjob.sbk

13. Using Windows Explorer, rename the seedjob's .cdb directory to whatever you wish for your new project. The cdb directory is located in your new \vbdc sub-directory. For example:
    - From > D:\Testjob \vbdc\Seed.cdb To > D:\Testjob \vbdc\Seed.cdb

14. Start the VeriBest "Design Capture" program on your computer.

15. Open the new project as follows:
    - From the menu, Select "Project" > "Open"; then browse to the new directory for example: D:\Testjob.
    - Select the newly named project file for example: testjob.prj and then select "OK".

16. Verify that the project **files** pointer is correct as follows:
    - From the menu, Select "Project" > "Files" and verify that the file paths in the dialog window correctly point into your new project directory. For example: D:\Testjob\vbdc\testjob.sbk

17. Verify that the project **settings designs** pointers are correct as follows:
    - From the menu, Select "Project" > "Settings" > "Designs" and verify that the file paths in the dialog window correctly point into your new project directory. For example: D:\Testjob\vbdc\testjob.sbk etc.

18. Verify that all the project settings library directory pointers are correct as follows:
    - From the menu, Select "Project" > "Settings" > "Libraries"
    - Select each library type in turn and verify that the file paths in the dialog window correctly point into your new project directory. For example: the "Symbols" libraries should be D:\Testjob\library\symlib; and the "PDBs" should be D:\Testjob\library\pdblib.
    - Note that the 2dcell library should be changed to point into the pcb directory of your new job. "Remove" the pointer to the seed local2d.ccl library and "add Dir…" the pointer to your directory containing local2d.ccl. For example: D:\Testjob\vbpcb\.

19. Verify that all the project settings file locations pointers are correct as follows:

- From the menu, Select “Project” > “Settings” > “File Locations”
- Select each “Configuration File Type” in turn and verify that the file paths in the dialog window correctly point into your new project directory except as noted below. For example: the “BOM Format” file should be D:\Testjob\vbdc\Dzero_bom.fmt
- These files are not job specific and need not be specifically in your project directory: EDIF Configuration, FONTS, all HPGL Plot files, PDP Editor Properties may be blank, VerilogConfig may be blank, VHDL may be blank.

20. Verify that the PCB integration parameters are correct as follows:
    - From the menu, select “Project” > “Settings” > “VBPCB Integration”.
    - In the “Veribest PCB Netclass File” window, browse to the netclass.ncf file located in your vbpcb directory. For example D:\Testjob\vbpcb\netclass.ncf. Select the netclass.ncf file; then select “OK” to leave the Browse window.
    - Select “OK” to leave the “VeriBest PCB Integration” dialog window.

21. Open page 01 of the schematic as follows:
    - From the menu, select “File” > “Open” > “testjob.sbk” > “01” > “OK”

22. The default sheet size in these seeds is “D”. This can be changed; but you should consider leaving it as is. “D” size will contain a very large hierarchical schematic; and can be printed to “B” size. The printed “B” size is easily readable and can be zig-zag folded to fit in a standard looseleaf notebook with the title block displayed. This will allow you to document your whole project, including schematics, in a single notebook.

Enter the Schematic

Save your work often. Some hints are as follows:

- Always use “ Symbol” > “**Device Place**” command to place parts. Anything placed with the “Symbol” > “**Place**” command instead of “Device Place”, does not become a PCB part. The “Symbol” > “Place” command is for graphics, power & ground symbols, inter-sheet connections etc.

- If you need a “part” that is not in one of the supplied *.pdb libraries, then you will have to make it. But first, you will have to make a “symbol” for it and possibly a “cell” (PC board footprint).

- Use the Symbol Editor to make the symbol. Put the new symbol in your “new_parts.slb” library. The Symbol Editor is accessed from within VeriBest Design Capture for example “Symbol” > “Open”.

- If you need to make a “cell”, then use the “Cell Library Manager”. Put the new cell in your local 2dcell library. Your local 2dcell library is located at for example: D:\Testjob\vbpcb\local2d.ccl. The Cell Library Manager is accessed via your NT “Start” dialog. For example: Start > Programs > VeriBest VB98.0 > VeribBest PCB > VeriBest Cell Library Manager

- Now you can use the Parts Data Base (PDB) Editor to make the new “part”. You must make all new parts in your “new_parts.pdb” library. The PDB Editor can be accessed from within VeriBest Design Capture. Select from the menu “Tools” > “PDB Editor”. Once in the editor, select “File” > “open”. Then browse to your library, for example D:\Testjob\vbdc\lib\new_parts.pdb. This is your own library of new parts. When you’re done with this job, copy this file into your next job.

- Use the VeriBest Manuals! (Remember the the shortcut you placed on your desktop).

Compile, Package and Back Annotate the schematic

23. Save the file first or compile and package will not work right. Do this as follows:
    - From the menu select “File” > “Save”

24. From within the “Design Capture” program (continued from above), “compile” the schematic as follows:
    - From the menu, select “Tools” > “Other Utilities” > “Create CDB” > “OK”
    - In the “CDB Compiler Options” dialog box, verify that the project filename is correct; for example: D:\Testjob \Testjob.prj
    - Verify that “Incremental Compile” is **de-selected**.
    - Verify that “Flatten Design” is **selected**.
    - Select “OK”.
    - Wait for the compiler to finish and examine the “Command Output” for errors. Look for “Compiler finished, no errors found.
    - Select “OK”, “Cancel” etc as necessary to return to the schematic window.
    - If there were any errors in the compile, find and fix them and repeat the compile until no errors occur.

25. From within the "Design Capture" program (continued from above), "Package" the schematic as follows:
    - From the menu, select "Tools" > "Other Utilities" > "Packager" > "OK"
    - In the "Packager" dialog box, verify that the project filename is correct; for example: D:\Testjob\Testjob.prj
    - Verify that the "Actions" is "Package Symbols".
    - Verify that "Update CDB" is **checked**.
    - Verify that "Overwrite PDB" is **checked**.
    - Verify that "Log CDB Data" is **checked**.
    - Select "OK".
    - Wait for the Packager to finish and examine the "Command Output" for errors. Look for !THE CDB IS UP-TO-DATE!
    - If "Design hs NOT been packaged" appears, examine the "partpkg" file for information. For example: D:\Testjob\vbdc\partpkg.
    - Select "OK", "Cancel" etc as necessary to return to the schematic window.
    - If there were any errors in the packaging, find and fix them and repeat the packaging until no errors occur.
26. From within the "Design Capture" program (continued from above), "Back Annotate" the schematic as follows:
    - First, **close** the schematic – otherwise it won't back annotate without errors. Then:
    - From the menu, select "Tools" > "Other Utilities" > "Back Annotation" > "OK"
    - In the "Back Annotation" dialog box, verify that the project filename is correct; for example: D:\Testjob\Testjob.prj
    - Browse to locate the "Back Annotation File"; for example: D:\Testjob\vbdc\bamwasis.bam
    - Select "OK"
    - Wait for the "Back Annotator" to finish and examine the "Command Output" for errors. Look for "Back-annotation process completed successfully".
    - Select "OK", "Cancel" etc as necessary to return to the schematic window.
    - If there were any errors in the packaging, find and fix them and repeat the packaging until no errors occur.
27. Re-open the schematic. If you do not see the reference designators on the schematic, you must update the display as follows:
    - From the menu, select "View" > "Display; **uncheck** "Display Instance Text" , and select "OK"
    - Then, again from the menu, select "View" > "Display; **check** "Display Instance Text" , and select "OK"
28. Save your work!

Configure the PCB Editor (If you have it)

29. You can leave "Design Capture" running, or you can exit.
30. Start the "VeriBest PCB" program using the program manager.
    - In the "VeriBest PCB Open Design File" dialog box, browse to the "Design.vbd" file in your vbpcb directory. For example: D:\Testjob\vbdc\Design.vbd
31. Setup the project file pointers as follows:
    - From the menu, select "Integration" > "Project Integration
    - Browse to the correct "Project File". For example: D:\Testjob\Testjob.prj
    - From within the "Project Integration" dialog box, select "Edit".
    - In the "Multiple Paths" window, check for correct paths. For example, the "2D Cell Library Path" should indicate D:\Testjob\vbpcb\local2d.ccl. The "3D Cell Library Path" should indicate D:\Testjob\vbpcb\local3d.ccl; etc.
    - In the "Single Paths" window, all selections should be blank.
    - Select "OK" to leave the "Edit" menu.
32. Forward annotate to the PCB as follows:
    - From within the "Project Integration" dialog box, select "Forward Annotate".
    - Check the "Database Load" and "Netload" boxes.
    - In the "Unused Components" option window, you can select "Delete Including Spares" to clean unused seed components from the board. However, if a VME seeds was used, you should leave these components alone (Change to Spares) and use them as locators, for example, the VME connectors.
    - Select "OK".
    - Wait for the process to complete, note the message, then select "Close".
33. View the annotation file as follows:
    - From the menu, select "File" > "File Viewer"

- Ignore warnings related to 3D Cell Libraries
- Carefully examine “net XXX has 1 pin warnings” to be sure they don’t indicate open connections in the schematic.
- Look for “Netload completed successfully” message.

34. Verify “Layers Info” as follows:
    - From the menu, select “View” > “Level Display”
    - In the lower right quadrant of the “Level Display” dialog box, verify that “Class Display” Top & Bottom are checked and that “View 1” is listed in the window, then select “OK”

35. Delete unwanted drafting elements as follows:
    - From the Micro-station “Palettes” menu, choose “Fence”.
    - From the pop-up fence menus that appear, setup and delete elements inside fence.
    - You will not be able to delete the board outline with a fence. To delete a board outline, merely place a new one and the old one will disappear (“From the menu, select “Board” > “Board Outline” > “Place”).

36. Back up your project. It is ready to place and route.

PCB Notes

These are some abstract notes to remember. They will make more sense as you proceed with your work.

- Cells, Pads & Pins: Every part on your schematic has an entry in one of the parts libraries (*.pdb) that designates what footprint (cell) will be used on the PCB. When you get ready to place the cells on the PCB, The PCB editor gets the cell from the local2d.ccl library inside your vbpcb directory. The cells are made up of “pads” and the pads have “pins”. The pad table (xxxx.pad) and pin table (xxxx.pin) where this information is found are pointed to by settings in the “Setup > Job Parameters > Attached Files “ dialog. Be sure that the pads and pins you get when you make a PCB are what you want them to be. See below for info. Veribest was delivered with one set of pads and pins, the VBLIB product contains two more sets, and the seed jobs extracted from the EES group contain a third set. Our seed job contains the EES group set.

- Checking Cells: From within VeriBest PCB, select “Output > Reports > Cell Listing” to create a listing of the cells in your design (localjob.pdb). Then use the file viewer to view & print dgncells.txt. Note, to generate the list, you will have to respond to the action keys.

- Checking Pads & Pins: Use VeriBest Report Writer to generate and print listings of your project’s pad and pin tables. (Output > Reports > VeriBest Reports). Then use “Attributes” to check each component as you place it to make sure that the pads/pins are what you think they are. This is done as follows: Edit > Review > Object Attributes, then “left click” to select the component, then read the cell name in the lower right screen box, then “right click” to read the pin code, then “right click” again to read the pad code. Awkward ain’t it!

- More about Pins: pins represent the center of a pad within a cell. For through hole pads, pin numbers are actually drill sizes, however, pin 200-400 in the pin table are surface mount devices. Actual pin size is 5 mil and is used to locate the center.

- Importing Cells: The cell you need may be in on of the other xxx.ccl libraries (VeriBest\vbcore\library\cell\vbcore2d.ccl) etc. Use “Setup > Library Services > Cell Extraction” from within the PCB editor to look for the cells.

- Making Cells: You will use the “Cell Manager” to make new cells when the one you need is not in the library. All cells must be created by editing the local2d.ccl library. You edit the cell library as follows: from the menu, select “File” > “Open Cell Library”. Then browse to your library, for example D:\Testjob\vbpcb\local2d.ccl. More tips on cells are as follows:
    - When **editing** cells, do **not** change the pad. Use a pin with a proper **default** pad or make a new pin with the pad you need. The PCB editor will use the default pad, even if you specify a different one.
    - Put cells on layers 1 & 12 (top and bottom)
    - Leave solder mask top and bottom alone.
    - When adding cosmetic graphics (ie using Microstation), use level 72.

- PCB Editor: Use the advanced editor to do all adjustment of placing and routing. It is closer in format to the schematic editor. Eventually the basic editor will be discontinued.

- Use the VeriBest Manuals! (Remember the the shortcut you placed on your desktop).