Table 10: VME Commands and address of the TF board -1. The data bits not defined here should be masked by the software.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x0000000 (tf_register)	r/w	any time	bit0: run_mode bit1: generate FREEZE under run_mode
0x0000004 (tf_register)	r/w	r: any time(Tmode) w: Tmode	bit1-0: test mode type, bit5-2: TF ID, bit15-6: #events tried in test_mode, bit16: run test mode, bit17 : select VME clock, bit18: select 1/2 on-board clock, bit19: on-board clock disable, bit20: generate FREEZE, bit21 : generate INIT.
0x0000008 (fep_register)	r/w	r: any time(Tmode) w: Tmode	bit4-0: Max. trials for permutation, bit7-5: Min. hits requirement. bit8: INPUT_FIFO read disable.
0x000000C (opp_register)	r/w	r: any time(Tmode) w: Tmode	bit4-0: χ_1 cut value ($\times 2$), bit 5: do χ_1 cut, bit10-6: χ_2 cut value ($\times 2$), bit 11: do χ_2 cut, bit16-12: χ_3 cut value ($\times 2$), bit 17: do χ_3 cut, bit18: BP_FIFO write is debug mode (all SVT words are written), bit19: HOLD from the OPP processor
0x0000010 (fitc_register)	r/w	r: any time(Tmode) w: Tmode	bit4-0: Clock counts to the FIT_DONE. bit5: TF_FIFO read disable. bit6: BP_FIFO write disable. bit7: Select the 2nd set for the Intercept Memories. bit8: Ignore HOLD in the FIT and OPP processors under run_mode.
0x0000014 (FII0_register)	r/w	r: any time(Tmode) w: Tmode	bit4-0: bit shift distance for the ϕ (FIT0), bit9-5: bit shift distance to add the XFT ϕ product, bit14-10: bit shift distance to add the XFT c product note: each MSB is the shift direction bit15: Write-enable for the FIT0 intercept memory bit16: Status of the FIT0 intercept memory (1:ready,0:busy).
0x0000018	r/w	same as the FIT0	same definition as 0x0000014 for the d (FIT1).
0x000001C	r/w	same as the FIT0	same definition as 0x0000014 for the c (FIT2).
0x0000020	r/w	same as the FIT0	same definition as 0x0000014 for the χ_1 (FIT3).
0x0000024	r/w	same as the FIT0	same definition as 0x0000014 for the χ_2 (FIT4).
0x0000028	r/w	same as the FIT0	same definition as 0x0000014 for the χ_3 (FIT5).
0x000002C	r/w	any time (Tmode or freeze)	ISPY counter (write: reset) bit16-0: pointer, bit17: overflow, bit18: SPY status (Freeze=0)
0x0000030	r/w	any time (Tmode or freeze)	OSPY counter (write: reset) bit16-0: pointer, bit17: overflow, bit18: SPY status (Freeze=0)
0x0000034	r	any time(Tmode)	bit4-0: FEP program version number
0x0000038	r	any time(Tmode)	bit4-0: OPP program version number
0x000003C	r	any time(Tmode)	bit4-0: FITTER/CONTROL program version number
0x0000040	r	any time(Tmode)	bit4-0: FITTER/FIT0 program version number
0x0000044	r	any time(Tmode)	bit4-0: FITTER/FIT1 program version number
0x0000048	r	any time(Tmode)	bit4-0: FITTER/FIT2 program version number
0x000004C	r	any time(Tmode)	bit4-0: FITTER/FIT3 program version number
0x0000050	r	any time(Tmode)	bit4-0: FITTER/FIT4 program version number
0x0000054	r	any time(Tmode)	bit4-0: FITTER/FIT5 program version number

Table 11: VME Commands and addresses on the TF board -2.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x0000058	r	Tmode	INPUT FIFO read bit22-0 : SVT input data, bit23 : input HOLD.
0x000005C	r	Tmode	TF FIFO (bits 90-59) at FITTER/CONTROL
0x0000060	r	Tmode	TF FIFO (bits 99-91) at FITTER/CONTROL
0x0000064	r	any time(Tmode)	bit2-0: FITTER/FIT0 ID (must be 0)
0x0000068	r	any time(Tmode)	bit2-0: FITTER/FIT1 ID (must be 1)
0x000006C	r	any time(Tmode)	bit2-0: FITTER/FIT2 ID (must be 2)
0x0000070	r	any time(Tmode)	bit2-0: FITTER/FIT3 ID (must be 3)
0x0000074	r	any time(Tmode)	bit2-0: FITTER/FIT4 ID (must be 4)
0x0000078	r	any time(Tmode)	bit2-0: FITTER/FIT5 ID (must be 5)
0x000007C	r	Tmode	TF_FIFO (bits 31-1) read by FIT0
0x0000080	r	Tmode	TF_FIFO (bits 31-1) read by FIT1
0x0000084	r	Tmode	TF_FIFO (bits 31-1) read by FIT2
0x0000088	r	Tmode	TF_FIFO (bits 31-1) read by FIT3
0x000008C	r	Tmode	TF_FIFO (bits 31-1) read by FIT4
0x0000090	r	Tmode	TF_FIFO (bits 31-1) read by FIT5
0x0000094	r	Tmode	TF_FIFO (bits 58-32) read by FIT0
0x0000098	r	Tmode	TF_FIFO (bits 58-32) read by FIT1
0x000009C	r	Tmode	TF_FIFO (bits 58-32) read by FIT2
0x00000A0	r	Tmode	TF_FIFO (bits 58-32) read by FIT3
0x00000A4	r	Tmode	TF_FIFO (bits 58-32) read by FIT4
0x00000A8	r	Tmode	TF_FIFO (bits 58-32) read by FIT5
0x00000AC	r	any time(Tmode)	FIFO status bit1-0 : NOT EMPTY of INPUT FIFO, bit7-2 : NOT EMPTY of TF_FIFO, bit9-8 : NOT Half FULL of INPUT FIFO, bit15-10 : NOT Half FULL of TF_FIFO, bit17-16 : NOT FULL of INPUT FIFO, bit23-18 : NOT FULL of TF_FIFO,

Table 12: VME Commands and addresses on the TF board -3. The fitting result read by the OPP consists of 14 bits of data plus 3 bits of overflow error information.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x00000B0	r/w	any time (Tmode or freeze)	Error Status Register-1 (reset by the SVT INIT) read bit10-0 : error status write bit0 : clear the register write bit1 : clear the SVT ERROR write bit2 : clear the CDF ERROR
0x00000B4	r/w	any time (Tmode or freeze)	Error Status Register-2 (NOT reset by the SVT INIT) read bit10-0 : error status read bit31 : CDF_ERR presents, bit30 : SVT_ERR presents write bit0 : clear the register write bit1 : clear the SVT ERROR write bit2 : clear the CDF ERROR
0x00000B8	r/w	any time(Tmode)	bit10-0: TF Error MASK
0x00000BC	r/w	any time(Tmode)	bit10-0: SVT Error MASK
0x00000C0	r/w	any time(Tmode)	bit10-0: CDF Error MASK
0x00000C4	r/w	any time(Tmode)	bit9-0: EOE word Error MASK
0x00000C8	r	Tmode	bit16-0: ϕ result at OPP
0x00000CC	r	Tmode	bit16-0: d result at OPP
0x00000D0	r	Tmode	bit16-0: c result at OPP
0x00000D4	r	Tmode	bit16-0: χ_1 result at OPP
0x00000D8	r	Tmode	bit16-0: χ_2 result at OPP
0x00000DC	r	Tmode	bit16-0: χ_3 result at OPP
0x00000E0	r/w	Tmode	generate a single clock based on the VME data strobe.

Table 13: VME Addresses to the memories.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x0001xxx	r/w	Tmode	FIT0 Coefficient memory (bit 31-0)
0x0002xxx	r/w	Tmode	FIT1 Coefficient memory (bit 31-0)
0x0003xxx	r/w	Tmode	FIT2 Coefficient memory (bit 31-0)
0x0004xxx	r/w	Tmode	FIT3 Coefficient memory (bit 31-0)
0x0005xxx	r/w	Tmode	FIT4 Coefficient memory (bit 31-0)
0x0006xxx	r/w	Tmode	FIT5 Coefficient memory (bit 31-0)
0x0007xxx	r/w	Tmode	FIT0 Coefficient memory (bit 63-32)
0x0008xxx	r/w	Tmode	FIT1 Coefficient memory (bit 63-32)
0x0009xxx	r/w	Tmode	FIT2 Coefficient memory (bit 63-32)
0x000Axxx	r/w	Tmode	FIT3 Coefficient memory (bit 63-32)
0x000Bxxx	r/w	Tmode	FIT4 Coefficient memory (bit 63-32)
0x000Cxxx	r/w	Tmode	FIT5 Coefficient memory (bit 63-32)
0x000Dxxx	r/w	Tmode	FIT0 Coefficient memory (bit 67-64)
0x000Exxx	r/w	Tmode	FIT1 Coefficient memory (bit 67-64)
0x000Fxxx	r/w	Tmode	FIT2 Coefficient memory (bit 67-64)
0x0010xxx	r/w	Tmode	FIT3 Coefficient memory (bit 67-64)
0x0011xxx	r/w	Tmode	FIT4 Coefficient memory (bit 67-64)
0x0012xxx	r/w	Tmode	FIT5 Coefficient memory (bit 67-64)
0x0013xxx	r/w	Tmode	χ^2 Memory bit 9-0: Square of (address i/2).
0x01xxxxx	r	any time(Tmode)	ID PROM (see CDF note xxxx).
0x04xxxxx	r/w	r:freeze or Tmode w:Tmode(Tmode or freeze)	ISPY memory bit 22-0: SVT data, bit 23: HOLD
0x05xxxxx	r/w	r:freeze or Tmode w:Tmode(Tmode or freeze)	OSPY memory bit 22-0: SVT data, bit 23: HOLD
0x060xxxx	r/w	Tmode	SS_MAP memory bit 3-0: 4 LSB of SS position at layer 0. bit 7-4: 4 LSB of SS position at layer 1, and so on
0x068xxxx	r/w	Tmode	MAKE_ADDR memory bit 4-0: Sub-address to the Intercept memory. bit 12-5: Address to the Coefficient memory.
0x0700000	r/w	any time	read BP_FIFO, or write: Reset the FIFO bit 22-0: SVT data. bit 24-23: spare bit 30-25: FIFO flags. (FF1, FF2, AF1, AF2, EF1, EF2) EF1 is the empty flag of FIFO-1, and AF and FF is the almost Full and Full flags. Flags are active low.
0x40xxxxx	r/w	Tmode	Intercept Memory for FIT0 bit 12-0: Intercept, bit 13: sign
0x48xxxxx	r/w	Tmode	Intercept Memory for FIT1
0x50xxxxx	r/w	Tmode	Intercept Memory for FIT2
0x58xxxxx	r/w	Tmode	Intercept Memory for FIT3
0x60xxxxx	r/w	Tmode	Intercept Memory for FIT4
0x68xxxxx	r/w	Tmode	Intercept Memory for FIT5