The DØ Muon System Upgrade
DØ Note #2780

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1 Introduction

The upgrade of the DØ muon system for Run II was last reviewed at the April 1995 PAC meeting [1]. At that time, the muon upgrade consisted of the existing WAMUS PDTs with new electronics and a new forward trigger system made up of scintillator pixels and pad chambers. Since that review, the design of the upgraded muon system has undergone a major evolution. The primary reason for the change is aging of the WAMUS PDTs.

Studies of the aging of the forward WAMUS chambers (the "EF" PDTs) reveal that these chambers will not survive Run II [2]. This conclusion results from consideration of Fig. 1 where the luminosity which reduces the wire gain by a factor of $1/e$ is plotted for various groupings of chambers [3]. We can define PDT "lifetime" as this luminosity and stipulate that the chamber must be zap-cleaned [4] after one lifetime. For example, Fig. 1 implies that the EF B-layer PDTs (EFB) must be zapped $\sim 10-20$ times during a Run II of a few fb^{-1}. Past experience with the time-consuming and difficult zapping operation has shown that a long shutdown is necessary to clean the forward chambers. Given that these shutdowns occur only several times during the course of the run, we conclude that PDTs which require zap-cleaning more than ~ 3 times during Run II will not survive. The EFA, EFB, and EFC chambers are in this category. Indeed, the most forward central PDTs, the so-called "ring" chambers (numbered 10x,20x,14x,24x), are in trouble and will require a shielding factor of $\gtrsim 3$ just to survive. The bottom line from the aging studies is that the forward WAMUS PDTs will have to be replaced in order to retain coverage beyond $|\eta| \approx 1$ (pure CF).

In light of this, a new baseline design for the upgraded muon system has been developed. The new design was driven by the DØ Run II physics goals. The physics motivations for going to the highest luminosities are to study low-cross-section, high-p_T processes, such as top and W/Z, and to search for new phenomena. In order to maximize the acceptance for muons from these processes, we need sufficient detector coverage and an efficient, unprescaled trigger.

The range in $|\eta|$ for muons from top and WW events are shown in Fig. 2 [5]. Increasing the $|\eta|$ coverage from 1.0 to 1.7 increases the geometric detection efficiency from 50% to 85% for muons from W decay in top events. The $|\eta|$ distribution of muons from b-tagged jets is essentially the same as those from W's so the same efficiency gains are there for μ-tagging. Similarly, the acceptance rises from 35% to 75% for WW events. Another physics topic of interest for Run II is the measurement of the W asymmetry. Figure 3 plots the experimentally measured quantity, the decay lepton charge asymmetry, as a function of $|\eta^{lepton}|$ for two popular parton distribution functions [6]. Also shown in Fig. 3 is the significance of the difference between the predictions for the two pdf's as a function of $|\eta|$ coverage. It is evident that the significance rises rapidly with $|\eta^{max}|$ up to $|\eta| \sim 2$ after which the gains are small. It is clear from these representative processes that $|\eta|$ coverage out to ~ 2 is sufficient for high p_T physics. The new baseline features full muon coverage for $|\eta| \lesssim 2$.

The muon trigger in Run II will combine track candidates from the fiber tracker trigger (CFT) with information in the muon system. The effective η range of this trigger is thus defined by where the CFT trigger ends, *i.e.* at $|\eta| \sim 1.7$. Studies of Run II trigger rates [7, 8] show that the combined muon/CFT trigger will be unprescaled for high-p_T single muons ($p_T > 6$ GeV) and low-p_T dimuons ($p_T > 3$ GeV). With the proposed shielding, the combinatoric trigger rate is dramatically reduced to the point where the trigger rate is dominated by real muons.

The individual components of the new design will be discussed in detail in subsequent sections, a brief overview is given here. In general, we have attempted to minimize the number of regional boundaries, chamber technologies, and distinct electronics boards. We have also built in hooks to allow a natural path to surviving $\mathcal{L} = 10^{33}$ cm^{-2} s^{-1}.

For $|\eta| \lesssim 1$, the WAMUS PDTs are retained but the electronics, from the front-ends to the Movable Counting House (MCH), are completely replaced. There will be two layers of scintillator: the current "Cosmic Cap" that sits just outside the C-layer and a new set of "A-ϕ" counters located between the calorimeter and the A-layer. We will use standard DØ definitions for A, B and C layers (A is closest to the interaction region). There will be a CFT*A-ϕ trigger with good geometric acceptance that will enable us to trigger on low-p_T muons ($\gtrsim 1.5$ GeV/c) in the central region. There will also be a trigger based on the hits in the PDTs as in Run I.

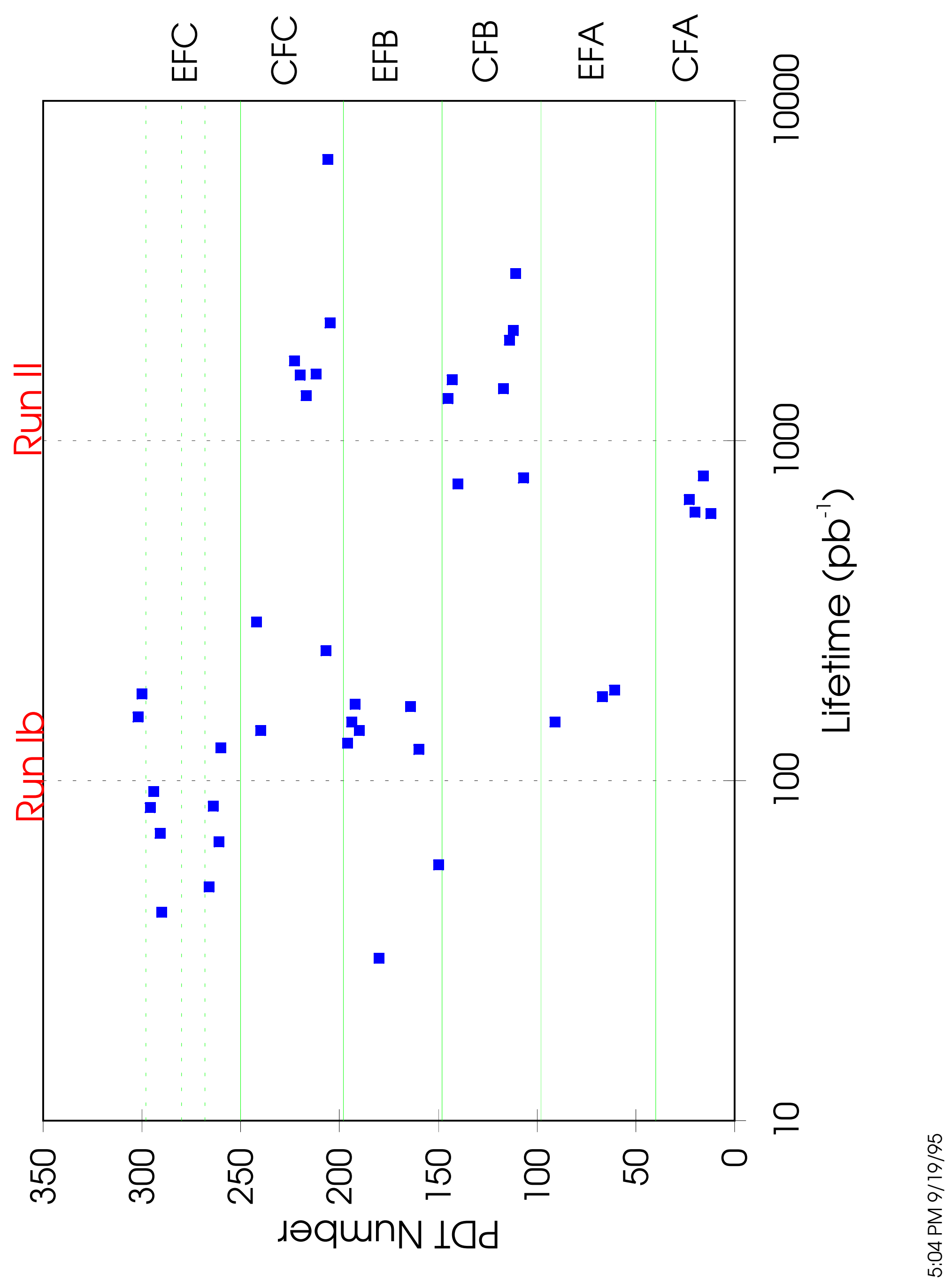


Figure 1: “Lifetime” of WAMUS PDTs versus chamber number. The approximate corresponding region is shown on the right hand axis.

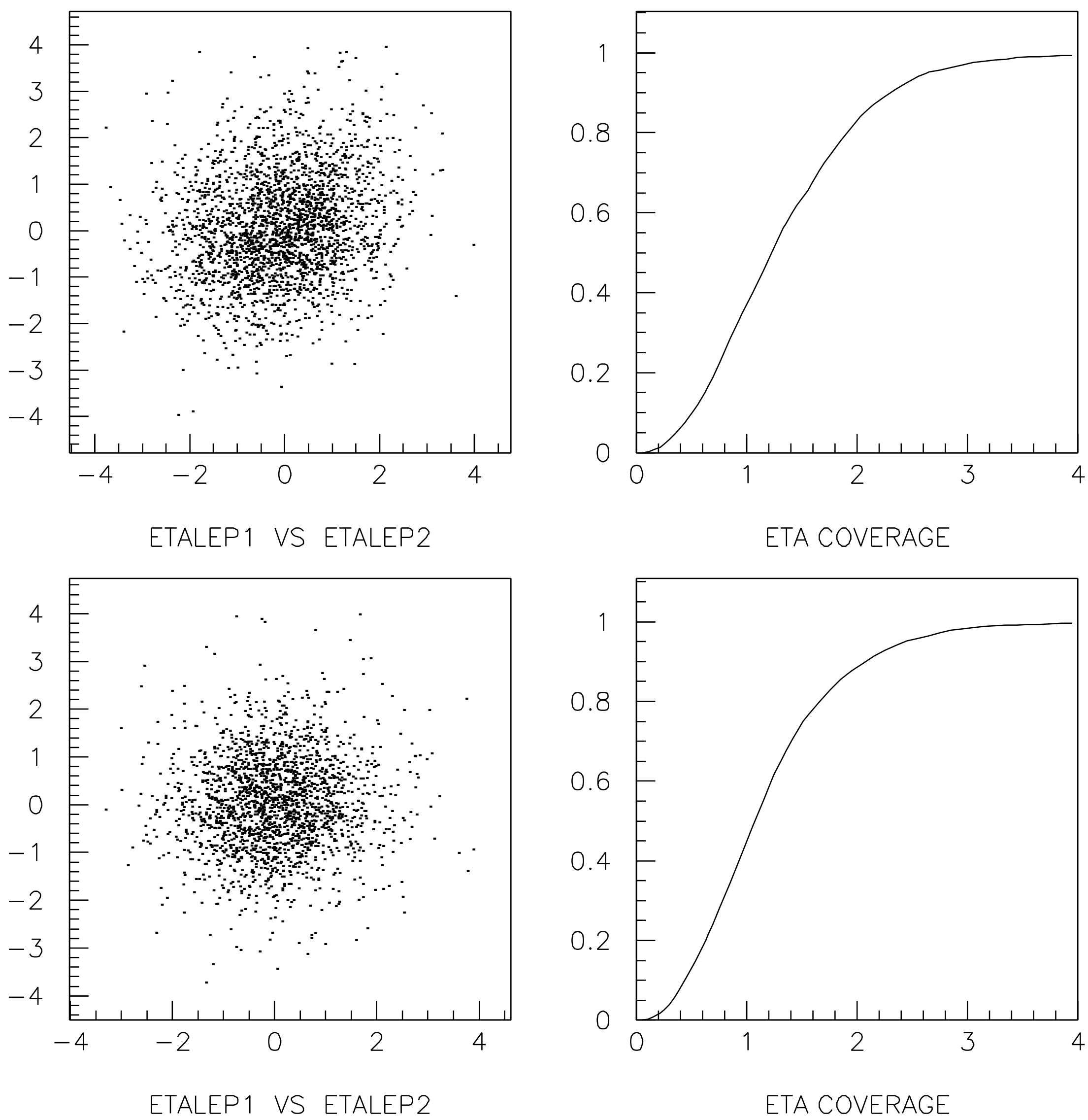


Figure 2: Shown (left upper and lower) are the $|\eta|$ distributions of muons from the decay of W's in WW production (upper) and $t\bar{t}$ ($M_{top} = 180$ GeV/c^2)(lower). The efficiency as a function of $|\eta|$ coverage of the muon detector is shown (right).

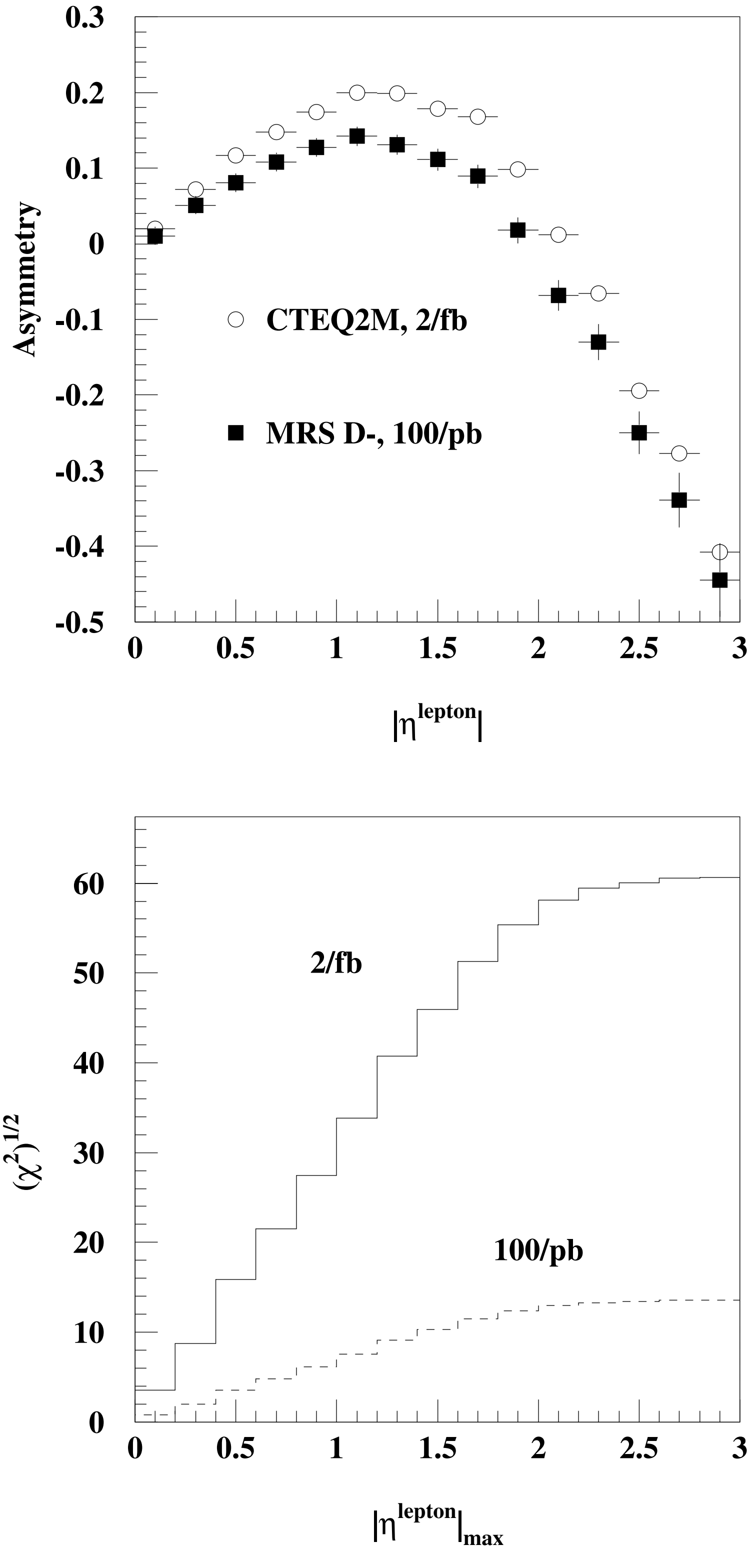


Figure 3: (Upper) The predicted lepton charge asymmetry for W decays is shown as a function of the lepton $|\eta|$. (Lower) The significance of the difference in the results from the CTEQ2M and MRSD- pdf's is plotted versus $|\eta|$ coverage.

For $1 < |\eta| < 2.0$, the PDTs will be replaced with Iarocci-tube based chambers. The tubes are square in cross section and 1 *cm* wide. They will be arranged in three planes (A,B,C) with (4,3,3) layers of tubes per plane. There will be three planes (A,B,C) of scintillator pixels arranged in an $R-\phi$ geometry. The trigger will be provided by a CFT*Pixel coincidence. As in the central region, a Run I-style trigger based on the Iarocci wires will also be implemented.

To summarize, we have converged on a new baseline design for the DØ muon system upgrade. The performance of this system will allow us to meet the challenges of Run II. However, this comes at a price: we will need new detectors for the forward region and, in order to provide enough shielding, we must restrict the forward coverage to $|\eta| \lesssim 2$. Therefore the SAMUS stations will be removed after Run I. The upgrade system will survive the harsh environment of Run II and hooks are available to also live with 10^{33} cm^{-2} s^{-1}. We are ready to complete the detailed design work and proceed to build the system.

The remainder of this document is organized as follows: Section 2 summarizes the studies of shielding, Section 3 will discuss the central region, Section 4 will detail the entirely new forward region, Section 5 deals with the front-end and DAQ electronics, and Section 6 outlines the Level 1 muon trigger.

2 Shielding

2.1 Introduction

An important part of the DØ muon system upgrade is the addition of shielding material to block non-muon background particles[9]. There are three important background sources to consider. The first two are due to scattered proton and antiproton fragments which interact with the exit of calorimeter or the beampipe and low-beta quadrupole magnet. The former produces a background in the central and forward muon A-layer, and the latter produces showers in the forward B and C-layers. The third source is the accelerator. However, halo from the tunnel became small compared to the contribution from interactions after shielding was installed in the tunnel during Run Ib [10]. Shielding these background sources is important because it will reduce the occupancy of the detectors. This decreases the fake trigger and track probabilities and increases the detector lifetime by reducing aging. It also provides insurance against the unpredictable effects of large background fluxes.

2.2 Forward Region B and C-Layer Shield

The main feature of the shield is a thick iron and polyethylene case surrounding the beampipe and low beta quadrupole magnet. The shield is shown in Fig. 4 extending from the calorimeter to the accelerator tunnel. The case is ~ 68 inches wide on the outside and has a hole ~ 20 to 25 inches wide on the inside for the accelerator equipment. A one inch thick layer of lead surrounds the outside of the case.

Iron is conventionally used as a hadron and electromagnetic absorber because it has reasonably short interaction length (16.8 cm) and radiation length (1.76 cm), and is relatively inexpensive. However, iron is almost transparent for low energy neutrons. Polyethylene is used as neutron absorber because it is rich in hydrogen, which is effective because it is a low mass nucleus. The appropriate thickness of the iron and polyethylene was determined by Monte Carlo simulation. A list of "source particles" was created from minimum-bias collisions in a `GEANT` Monte Carlo simulation of the DØ detector. This list was then used as input to a `MARS` Monte Carlo simulation of various shielding configurations. Figure 5 shows the energy deposition from hadrons and electromagnetic showers in the shielded detector. A luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} is assumed. Table 1 shows a list of total energy deposition in B and C-layer upgrade detectors for five shielding configurations relative to the protection offered by the Run I design (no special shield). Table 2 shows the partial energy depositions from low energy neutrons, excitation, electromagnetic showers and charged hadrons. In the Run I design, 45% of the energy comes from easily suppressed electromagnetic showers. Increasing the thickness of the iron further reduces the energy deposition by providing more protection against hadronic showers. Copper is a somewhat more effective shielding material than iron but is more than twice as expensive. Increasing the thickness of the polyethylene reduces the total energy deposition by decreasing the contribution of low energy neutrons. Figure 6 is the energy deposition from hadrons and electromagnetic showers in the shielded detector. As in Fig. 5, a luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} is assumed. The contrast with between Fig. 5 and Fig. 6 is striking.

The bottom line is that the energy deposition from proton and antiproton remnants is

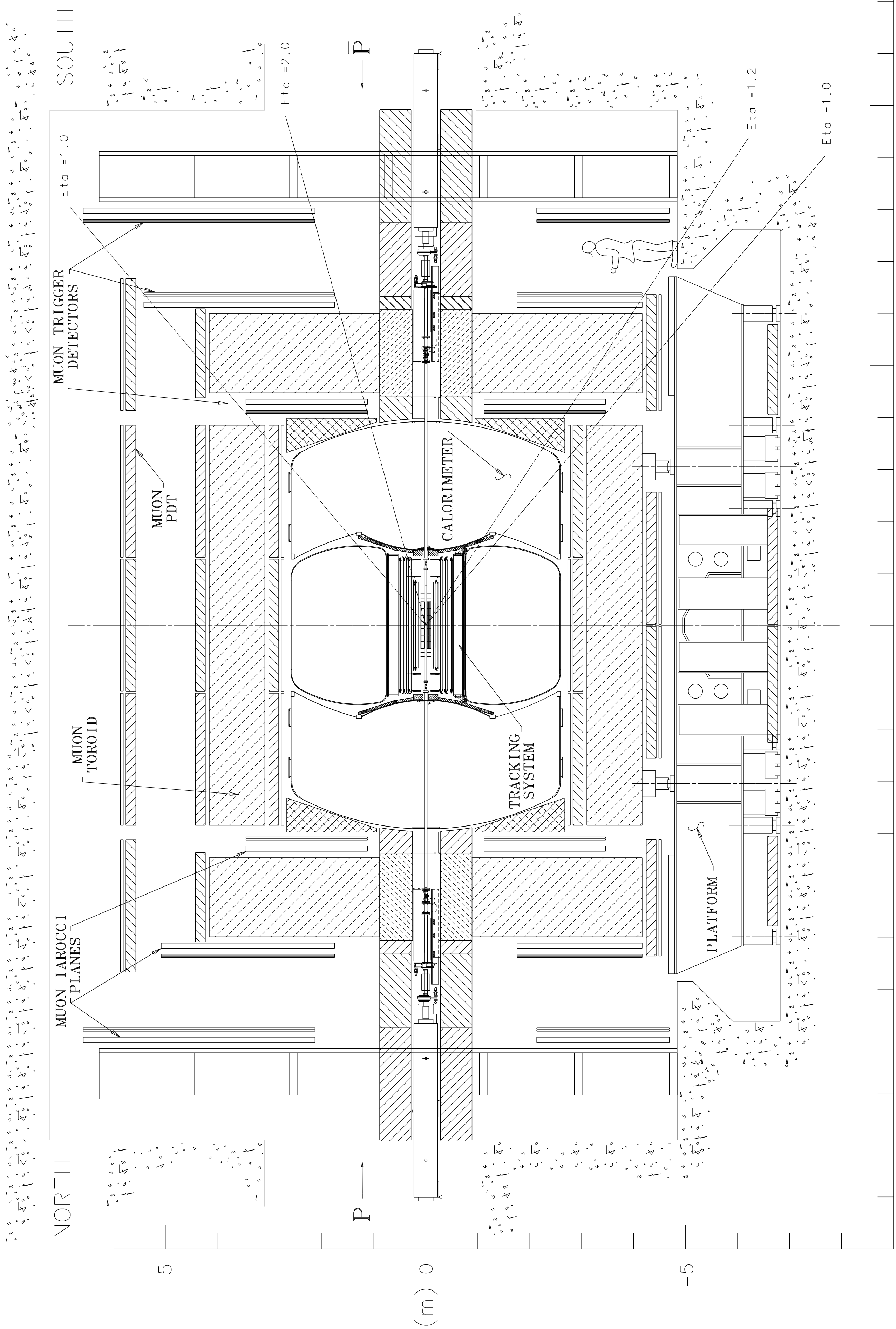
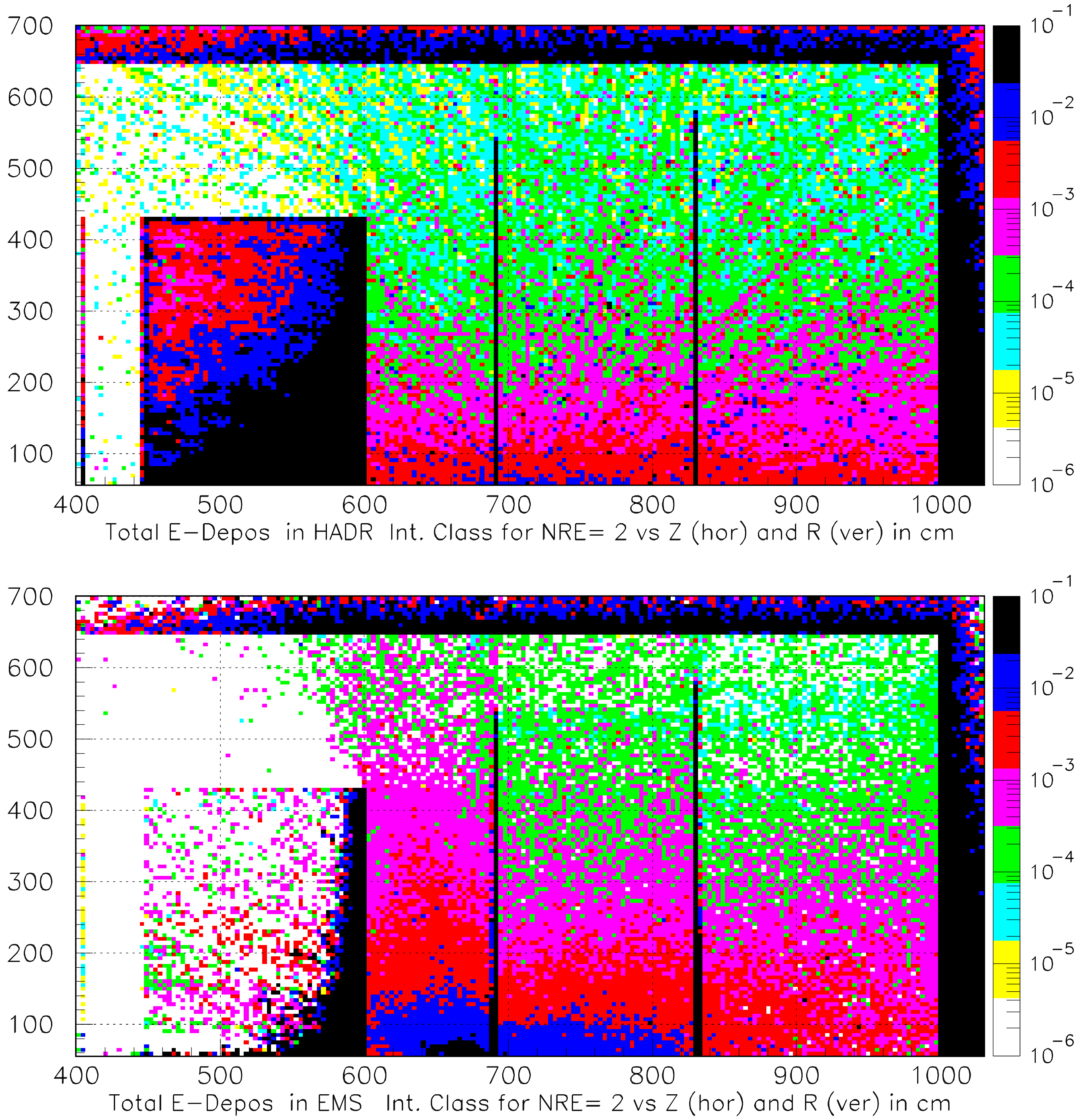


Figure 4: Side view of the DØ upgrade detector including the various elements of the muon system upgrade and the large scale shielding being considered.



In units of 10^n GeV/cm^3 per sec, where the color indicates the power n

Figure 5: Energy deposition from hadrons (upper) and electromagnetic showers (lower) in the unshielded detector. A luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} is assumed.

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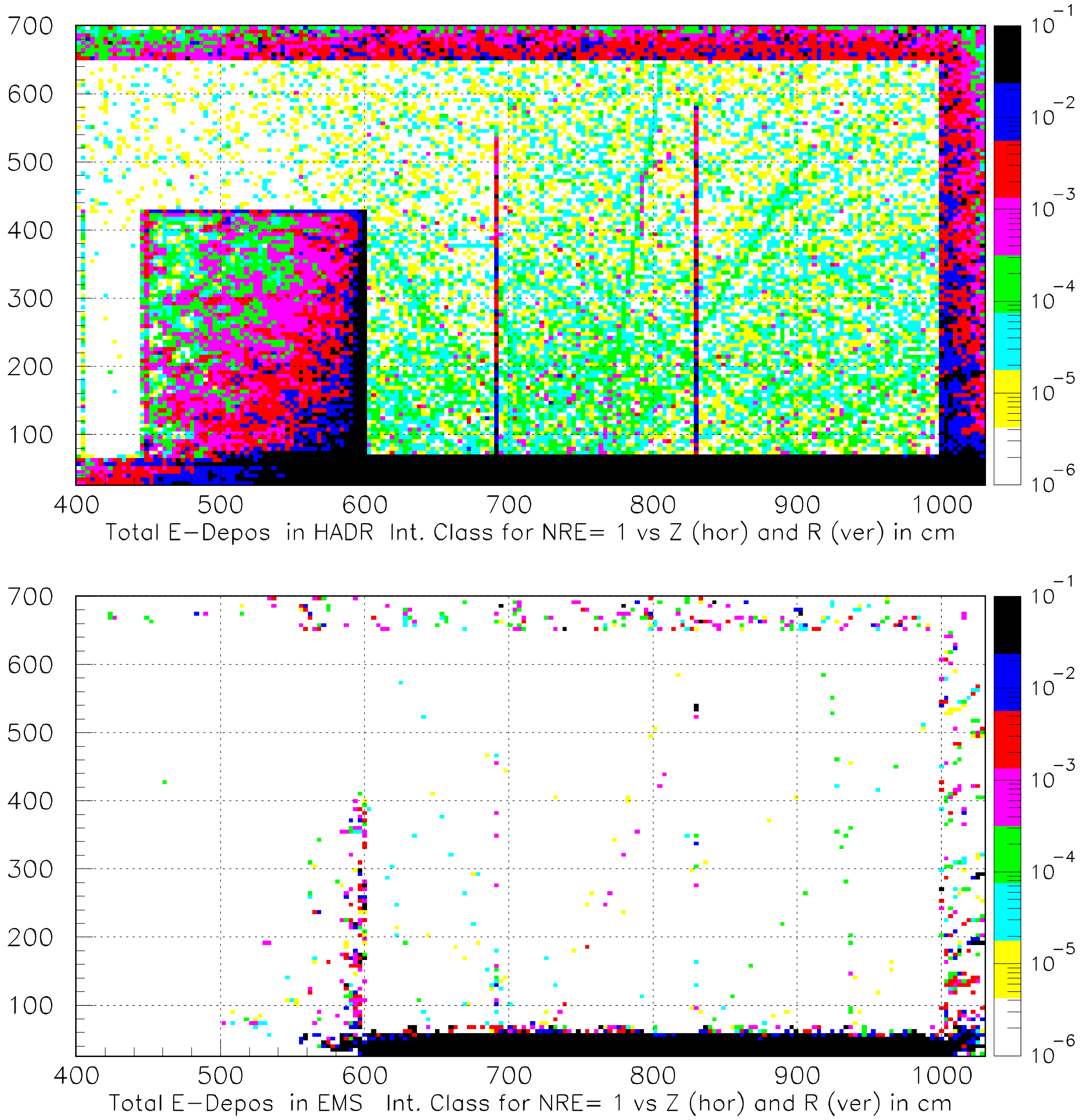

In units of 10^{n} GeV/cm^{3} per sec, where the color indicates the power n

Figure 6: Energy deposition from hadrons (upper) and electromagnetic showers (lower) in the shielded detector. A luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} is assumed.

Shielding Material (cm)	B-layer		C-layer	
	Iarocci Tubes	Scint. Counter	Iarocci Tubes	Scint. Counter
Run I	1	1	1	1
25 Fe + 5 CH	0.052	0.075	0.065	0.16
39 Fe + 5 CH	0.037	0.029	0.021	0.11
39 Cu + 5 CH	0.018	0.019	0.034	0.076
34 Fe + 10 CH	0.019	0.030	0.037	0.052
39 Fe + 15 CH	0.007	0.025	0.018	0.013

Table 1: Reduction in energy deposition for various shielding configurations.

Shielding Material (cm)	Low Energy Neutrons	d, t, α from excitation	Electromagnetic Showers	Charged Hadrons
Run I	0.11	0.23	0.45	0.21
25 Fe + 5 CH	0.40	0.31	0.037	0.25
39 Fe + 5 CH	0.42	0.29	0.008	0.28
39 Cu + 5 CH	0.31	0.33	0.10	0.26
34 Fe + 10 CH	0.23	0.49	0.053	0.23
39 Fe + 15 CH	0.18	0.44	0.002	0.38

Table 2: Partial energy deposition for various shielding configurations.

z (inches)	Minimum $\|\eta\|$	Maximum $\|\eta\|$
160	1.9	2.2
240	2.3	2.6
318	2.5	2.9
365	2.7	3.0

Table 3: Pseudorapidity edge of a square with side 70 inches long at various z locations corresponding approximately to the A, B, and C-layers of the forward muon detector.

reduced by approximately a factor of 50 with a shield comprised of 39 cm (15 inches) of iron and 15 cm (6 inches) of polyethylene. Continuation of these studies has indicated that an additional 3.2 inches of iron located on the inner core of the shield at the location from the exit of the toroid to the front of the low beta quadrupole magnet increases the shielding another factor of two to a total of $\sim 100\times$.

The shield necessarily occupies space at high pseudorapidity. To put a hole in it thick enough for a detector destroys the shield's effectiveness[12]-[13]. Table 3 indicates the minimum and maximum pseudorapidity covered by a square with side of length 70 inches (approximate size of the SAMUS magnet hole) at z locations corresponding approximately to the A, B and C-layers of the forward muon system.

We continue to study details of the shielding using the Monte Carlo simulations. We are concentrating on understanding the shielding effectiveness when scored with hits above threshold rather than with energy deposition.

2.3 Central Region A-Layer Shield

The A-Layer shielding will consist of two main parts, both located in between the end of the endcap cryostat and the EF toroid magnet. A polyethylene shield will be fitted to and mounted at the outer part of the cryostat just in front of the edge of the CF A-layer. The prototype shield mentioned in the previous section reduced the rate in the small test counters by a factor of five. The outer part of the shield shown in Fig. 4 (crosshatched part) has a radial thickness of $\sim$ 115 cm. It is necessary to put shielding just in front of the CF A-layer because there are otherwise unshieldable paths including in between the calorimeter vacuum vessels and through the liquid argon behind the hadron calorimeter. Polyethylene is good choice from both shielding and mechanical considerations.

Some of the particles can be blocked closer to the beampipe. In addition this shielding will reduce the flux in the forward scintillation counters and Iarocci tubes. Iron, polyethylene and lead with a geometry similar to the B and C layers will reduce the neutron and gamma flux by a factor of 2.5 to 4.5. Studies are underway to determine the optimal solution from the point of view of background rejection, detector operation and cost.

2.4 Summary

The upgrade of the DØ muon system will include the addition of shielding material. This shielding will reduce the occupancy of the detectors, the fake trigger and track probabilities, and reduce aging by suppressing the main background sources by approximately a factor of $50\times$.

Item	Layer		
	A	B	C
WAMUS PDTs (Drift Cells)	18 (1728)	38 (2424)	38 (2616)
Cosmic Cap Counters (PMTs)	-	-	240 (480)
CF Bottom B Counters (PMTS)	-	40 (80)	-
CF Bottom C Counters (PMTS)	-	-	40 (80)
EF Bottom B Counters (PMTS)	-	36 (72)	-
A-ϕ Counters (PMTS)	630 (630)	-	-

Table 4: Channel count for the various central muon upgrade detectors. These are sorted by layer. This does not include spare counters or electronics.

3 The Central Region

3.1 Introduction

The DØ muon detector is composed of sub-detectors with a "barrel" geometry in the central region and "planar" geometry in the forward and backward end regions. The pseudorapidity boundary between the two regions is at approximately $|\eta| = 1.0$. While muon detection for the forward and backward regions is being completely redesigned for Run II, we are retaining much of the present system in the central region. The 94 CF WAMUS drift chambers and the 480 scintillation counters of the C-layer "Cosmic Cap" will receive new electronics. The new detectors are scintillation counters added to the Bottom B and C-layers and to the CF A-layer.

3.2 Detectors

This section contains a description of the detectors planned for the upgrade of the central muon system. This includes the WAMUS PDTs, the Cosmic Cap and CF Bottom B and C-layer counters, and the "A-ϕ" and EF Bottom B-layer counters. These are shown in Fig. 4 and a channel count is provided in Table 4.

3.2.1 WAMUS

The WAMUS central region consists of three layers of drift chambers, one layer inside and two layers outside an iron toroid magnet. The purpose is to provide muon identification and a momentum measurement independent of the central tracking. The drift chambers produce the following measurements for each hit: the drift-time T perpendicular to the anode wire, the difference ΔT in the arrival time of the hit between a hit cell and the neighbor connected to it at the far end, providing the distance along the wire, and the charge deposition on inner and outer vernier pads, providing a more accurate measure of the distance in the direction along the wire. A detailed description is available [14]-[15]. The Run Ib gas mixture is composed of 90% Argon, 6% CF_4 and 4% CO_2. The maximum drift time is 750 ns for a 5 cm drift with the wires operating at 4.56 kV and the pads operating at 2.3 kV. In order to reduce the number of crossings which occur during one drift interval, we are considering using a faster gas mixture during Run II. The gain, drift-time-to-distance and aging characteristics of 80% Argon, 10% CF_4 and 10% CH_4 are being studied. Preliminary results indicate the maximum drift time can be reduced to 450 ns with the wires operating at $\sim$ 5.0kV and the pads operating at $\sim$ 2.5kV. The contribution to the hit uncertainty due to diffusion is estimated as less than 500 microns, worse than the present 300 microns, but smaller than the 700 micron residual typically achieved in WAMUS chambers during Run I. The trade-off in resolution is offset by the reduced occupancy and benefits to triggering achieved by decreasing the number of crossings in one drift time from 6 to 4 for 132 ns bunch spacing operation.

As discussed in Section 5, the electronics will be modified to provide a deadtimeless front-end readout with either 396 or 132 ns bunch spacing. We plan to readout the times and Δtimes from all of the chambers. Although not instrumented initially in all chambers, hooks are built in to allow readout of the pad information. The latched hit cells will be available for the muon Level 1 trigger.

3.2.2 Cosmic Cap and Cosmic Bottom Counters

The Cosmic Cap counters [18] cover the top and sides of the central region with 12 divisions in ϕ and 20 divisions in $\hat{z}$. The purpose is to provide a fast trigger detector outside of the toroid magnet and to tag the crossing for hits in the WAMUS CF B and C-layers. The background rate is small in comparison with other detector regions; very tight timing is not necessary to achieve adequate rejection. The counters on top are 113 inches long. The counters on the sides are 108 or 81.5 inches long, with the shorter counters closer to the floor. All of the counters are 25 inches wide. Thus the counters have their long dimension along ϕ and their short dimension along $\hat{z}$. This gives eight scintillation counters per PDT. These counters have already been built and are presently used during Run I. The counters are made from Bicron 404a scintillating material 1/2 inches thick. The light is collected by wavelength shifting fibers (Bicron CF91a and Kurary Y11) and read out with two EMI 9902 KA (1.5 inch) phototubes per counter. They have achieved timing resolution of 2.5 ns after offline corrections. Without the offline corrections the counters have timing resolution of $\gtrsim$ 5 ns.

The bottom of the central region has not been covered with scintillation counters during Run I and must be covered for Run II. The "Cosmic Bottom" includes the the CF Bottom B and C-layer counters and the EF Bottom B-layer counters. The general design is similar to the Cosmic Cap: scintillator sheets with waveshifter fibers for the light collection. Forty counters will be located on the B-layer chambers underneath the muon toroid. These are referred to as the "CF B-layer Bottom" counters. A minor difference between these counters and the Cosmic Cap is that these counters will be oriented with the short dimension along ϕ so that they cover a slice approximately $4\frac{1}{2}$ degrees wide. The smaller ϕ segmentation is advantageous for matching with the CFT trigger tracks. The counters come in two sizes: $15\frac{3}{4}$ inches wide or $22\frac{3}{8}$ inches wide and $98\frac{1}{8}$ inches long. The skinnier counters are located directly under the calorimeter pedestal where there is no A-layer coverage. A complete description of the mechanical design is available as a DØNote [19]. A full-size prototype has been constructed and tested. Construction of these counters will begin in Tata in February, 1996. The EF B-layer bottom, located on the pdts just underneath the North and South EF toroid magnets, consists of 36 counter expected to be $\sim$ 88 inches long and $\sim$ $15\frac{3}{4}$ inches wide. The CF C-layer bottom is located underneath the North and South ends of the platform and consists of approximately 40 counters with a design will be similar to those described above.

3.2.3 A-ϕ Scintillation Counters

The "A-ϕ" scintillation counters [20] are to be located in between the central calorimeter and the WAMUS central A-layer PDTs. The purpose is to provide a ϕ measurement for matching with the central tracking chamber for high and low p_T triggers and to reject out-of-time backgrounds originating at/near the exit of the calorimeter. The counters divide the A-layer into rows covering $\sim 4\frac{1}{2}$ degrees of ϕ. Each row contains 9 counters a little more than 33 inches long so that three columns of counters cover each 100 inch wide pdt. Because the geometry is box-like, the counter widths vary from 10 to 17 inches. Figure 7 shows a view of the A-ϕ scintillator array on the east or west A-layer wall. The scintillator is $\frac{1}{2}$ inch thick Bicron 404a. Light collection is accomplished with Bicron G2 waveshifter fiber. This waveshifter has a fast (2.5 ns) decay time and is well-matched to the scintillator and PMTs. The photomultipliers are Moscow Electric 115M tubes which have a 1" diameter.

We have built and tested a 36" x 13" prototype. The timing resolution, $\sim$ 2 ns, of the new design is sufficient to reject the out-of-time backgrounds.

The design of the A-ϕ counters has evolved recently. The University of Maryland built and tested some 100" x 16" counters which used custom, adiabatic lightguides, two PMTs and a mean-timer circuit. These counters were installed during the September 1995 shutdown. While these counters had better timing resolution, the new design is less expensive, easier to build and handle, and has only 2/9 of the counters in the A-layer "hotspot" discussed in Section 2. No mean-timers are necessary because the counters are much shorter.

We have been operating test counters in the CF A-layer during this collider run. Centered on $\eta = 0$ was a 50 inch long, 16 inch wide 1/2 inch thick scintillation counter with 2 inch PMTs on each end. Four small counters were located on the edge of the A-layer at $\hat{y} = 0$ in the high rate region of backscatter from the calorimeter exit. Two of these were on the North side and two on the South side. The two counters on the South side were located behind a 75 cm thick polyethylene shield [11]. The signals from the counters were latched and their time was recorded by TVCs located on PDT 127. For the large counter, the time is the mean time of the hit in the two PMTs. This eliminates the light propagation time in the counter. Figure 8, the result of offline analysis, shows the arrival time for three-layer calorimeter-confirmed muons, for background and A-layer only muons as measured in the big counter, and for background in one small counter. The time scale has an overall offset of $\sim$ 90 ns. The muons are well separated from the background. This is a milestone for the A-ϕ detector for it demonstrates that our Monte Carlo predictions [20] were correct.

All these counters will be outfitted with new, pipelined electronics for a deadtimeless readout. A hit "in-time" with a short gate will be latched and the time will be measured with a TDC. The latched hits will be used in the Level 1 trigger. An electronics pulser and an LED light pulser will be used for time and gain calibration.

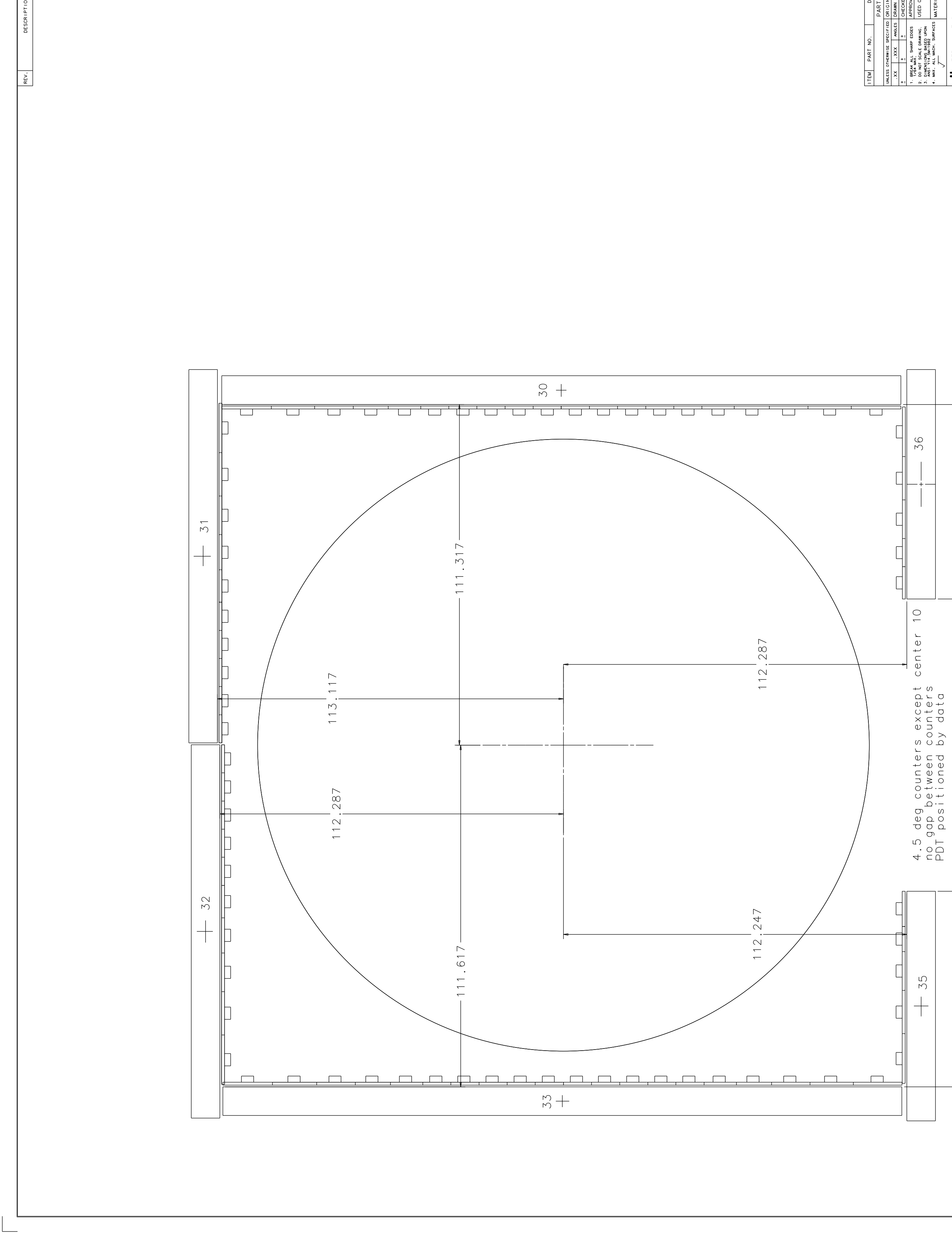

Figure 7: The A-ϕ counter array.

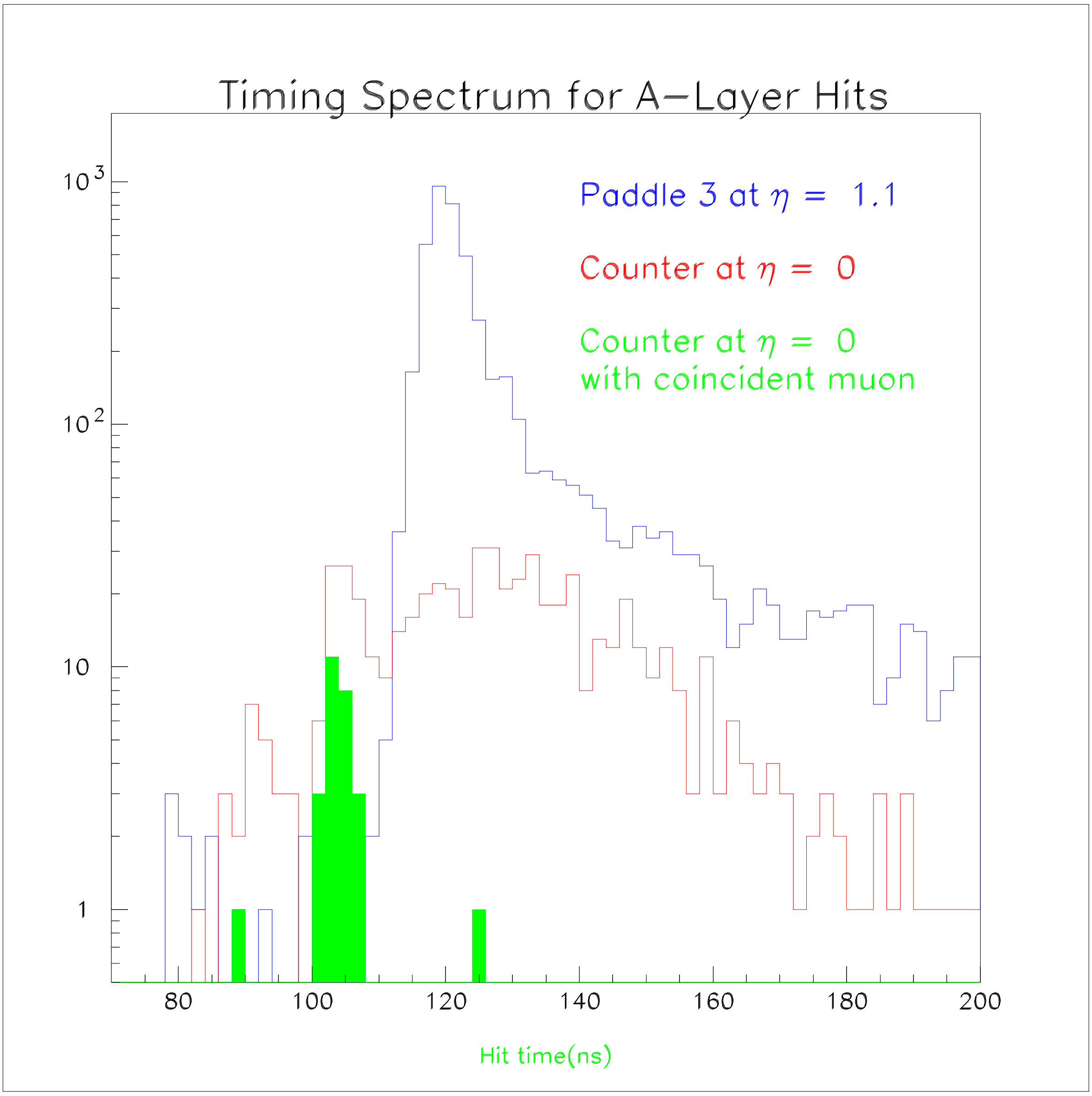

Figure 8: Time of flight results from A-ϕ test counters. The shaded peak is from 3-layer muons in a test counter centered at $\eta = 0$. The lower histogram is background from that counter. The upper histogram is for a small counter located on the edge of the CF A-layer.

4 The Forward Region

4.1 Introduction

Detection of muons in the forward region can considerably increase DØ efficiency for high p_T as well as b-physics. There is natural gap between central and forward muon detectors in the DØ detector: central (CF) and forward (EF) magnets, Fig. 4. The EF toroids provide magnetic field (B=1.9 T) to measure muon momentum and absorb punchthrough particles from hadronic showers.

Most of the hits in the forward muon detectors are due to remnants of hadronic and electromagnetic showers around the beam pipe [21, 22, 23]. Major improvements in the detector operation: reduced aging, trigger rates and fake track reconstruction probability can be achieved by additional shielding in the region of the beam pipe [9, 13, 21, 23].

Currently used for muon triggering and track reconstruction, WAMUS drift chambers will not withstand the high radiation doses of the upgraded Tevatron. They will age quickly - anode wires will be covered by a non-conductive layer. Due to long maximum electron drift time (around 500 ns for the fastest known gas mixture [24], around 750 ns for the mixture used in Run Ib) the occupancy of individual cell will be high and muon hits from different beam crossings (132 ns or 396 ns bunch spacing) will pile up. There are clearly significant advantages, both in triggering and reconstruction, for a forward detector with a maximum drift time less than the bunch crossing interval.

In order to trigger on real muons efficiently with high background rejection, a pixel-type detector is an advantage. Taking into account background rejection due to high time resolution (see below), scintillation pixel counters become a natural choice for the forward region muon trigger detector.

The proposed layout of the forward muon detectors is presented in Fig. 4. It consists of the following major parts:

1. Shielding around the beam pipe from calorimeter to the accelerator tunnel
2. 3 layers of Iarocci tubes working in proportional mode
3. 3 layers of scintillation pixel counters

4.2 Coordinate Detector - Iarocci Tubes

We selected Iarocci-type proportional tubes as coordinate detector for the forward muon system. The selected design has 10×10 mm^2 internal cross section with 50 μm anode wire in the center of each cell. The tubes in packs of 8 are made from plastic extrusion up to 5 m long. The internal surface of the tubes is covered with conductive paint (1 kΩ/cm^2) which provides cathode electrode. This type of tube have been extensively used in collider experiments [26]. Filled with a fast gas mixture (such as Ar(80%)+CF_4(10%)+CH_4(10%) such tubes will provide maximum electron drift time of 60 ns. The planned gate width of 100 ns is well within 132 ns bunch spacing time.

The layout of one Iarocci plane is shown in Fig. 9. The tubes are oriented along magnetic field lines (the field shape in EF toroids is more "square" than "circular"). The flux of particles drops with increasing distance from the beam pipe. Using geometry shown in Fig. 9 the occupancy of individual tubes will be the same over the entire plane within a factor of two. This geometry also minimizes number of channels per layer taking into account that tubes can be rather long.

Typical time distribution of hits in C-layer muon detectors is shown in Fig. 10 (with shielding discussed above). This figure is obtained for a single bunch crossing. There is a "long time tail" with decay time around 2 μs. Overlap of these tails from many crossings provides almost uniform background not shown on Fig. 10. The ratio of number of hits per event (gate) for the WAMUS chambers and Iarocci tubes (taking long time tail into account) is around 4 for 132 ns bunch spacing and $\mathcal{L} = 2 \cdot 10^{32}$ cm^{-2} s^{-1}. The average number of hits for 500 ns gate (WAMUS chambers with fast gas) is around 30/layer at $\mathcal{L} = 2 \cdot 10^{32}$ cm^{-2} s^{-1}.

Additional advantage of Iarocci drift tubes is small gas volume. They have 5 times lower sensitivity to fast neutrons than WAMUS chambers [27].

The efficiency of the individual Iarocci tube is near to 100%, but due to 1 mm walls between extruded tubes the efficiency of plane is 90% (1 mm wall/10 mm cell). In order to have track segment from each layer the planes will be separated by 10-20 mm, see Fig. 11. The energy of electrons from neutron interactions is below 1 MeV. The range out cut for such electrons is around 5 mm of polyethylene. The gap between Iarocci planes will be filled with polyethylene plates in order to reduce probability of track segment formation by low energy electrons.

To reconstruct muon track segment at least 2 hits per layer are needed. Taking into account 90% efficiency of one plane overall segment finding efficiency for 2 planes per layer will be around 80% only (2-out-of-2 combination). The 3 layers muon reconstruction efficiency will be below 50%. For 3 planes per layer (as shown in Fig. 11) the 2 out of 3 efficiency is 97%. For B and C layers we propose to use 3 planes of Iarocci tubes per layer. Number of planes in A-layer is equal to 4. The A-layer background flux is a factor of 3 higher than for B and C. In order to detect soft muons (ranging out in EF toroid) we will use 3 points on track segment: two to find segment and the third to confirm it (any two hits will provide "segment"). The 3-out-of-3 efficiency is 72% only, but 3-out-of-4 is above 91%. The reasonably large number of points on track will improve coordinate accuracy of the track reconstruction (improve momentum resolution and match with central detector) and make track reconstruction algorithms more robust. We propose 4(A)+3(B)+3(C) design - similar to central WAMUS design.

Momentum resolution of the magnetic spectrometer is limited by multiple scattering and coordinate resolution of muon detector. The typical coordinate resolution of WAMUS and SAMUS detectors (per layer) in Run I was around 1 mm. Mechanical inaccuracies, survey problems, as well as time-to-distance calibration, are the major resolution limiting factors. For 3 planes of Iarocci tubes, the per layer effective coordinate resolution is around 1.4 mm. In the upgraded DØ detector we will have momentum measurement from the fiber tracker and SVX: there are at least two central fiber tracker layers until $|\eta|$=2.0. The overall momentum resolution will be significantly better than in Run I. Monte Carlo studies of muon momentum resolution vs. η and muon momentum are under way.

The total number of Iarocci 8-tube modules is 6k (48k individual channels). They will be produced at the JINR (Dubna) factory, tested and shipped for final assembly to FNAL.

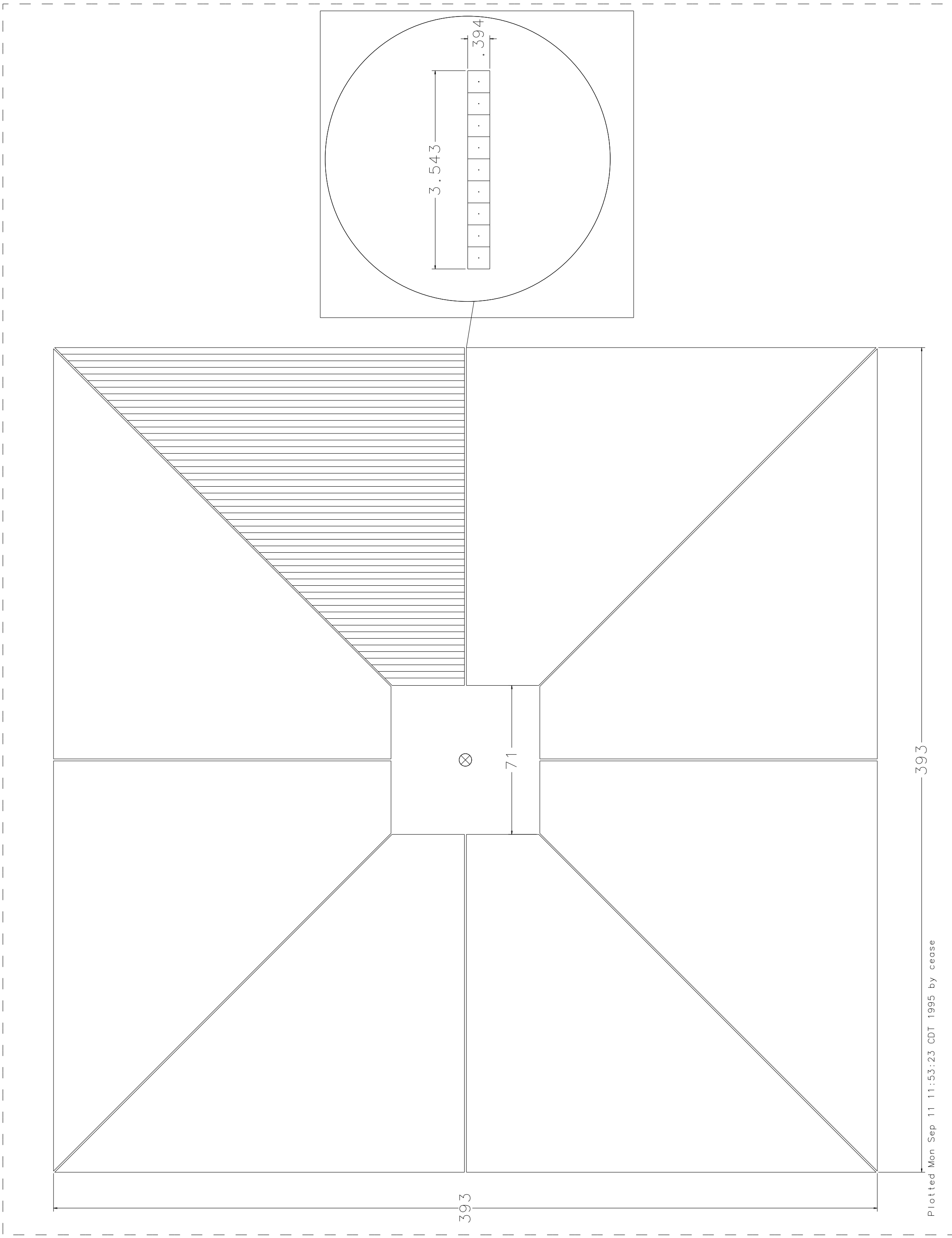

Figure 9: Iarocci proportional tubes: individual 8 tubes module and one plane design.

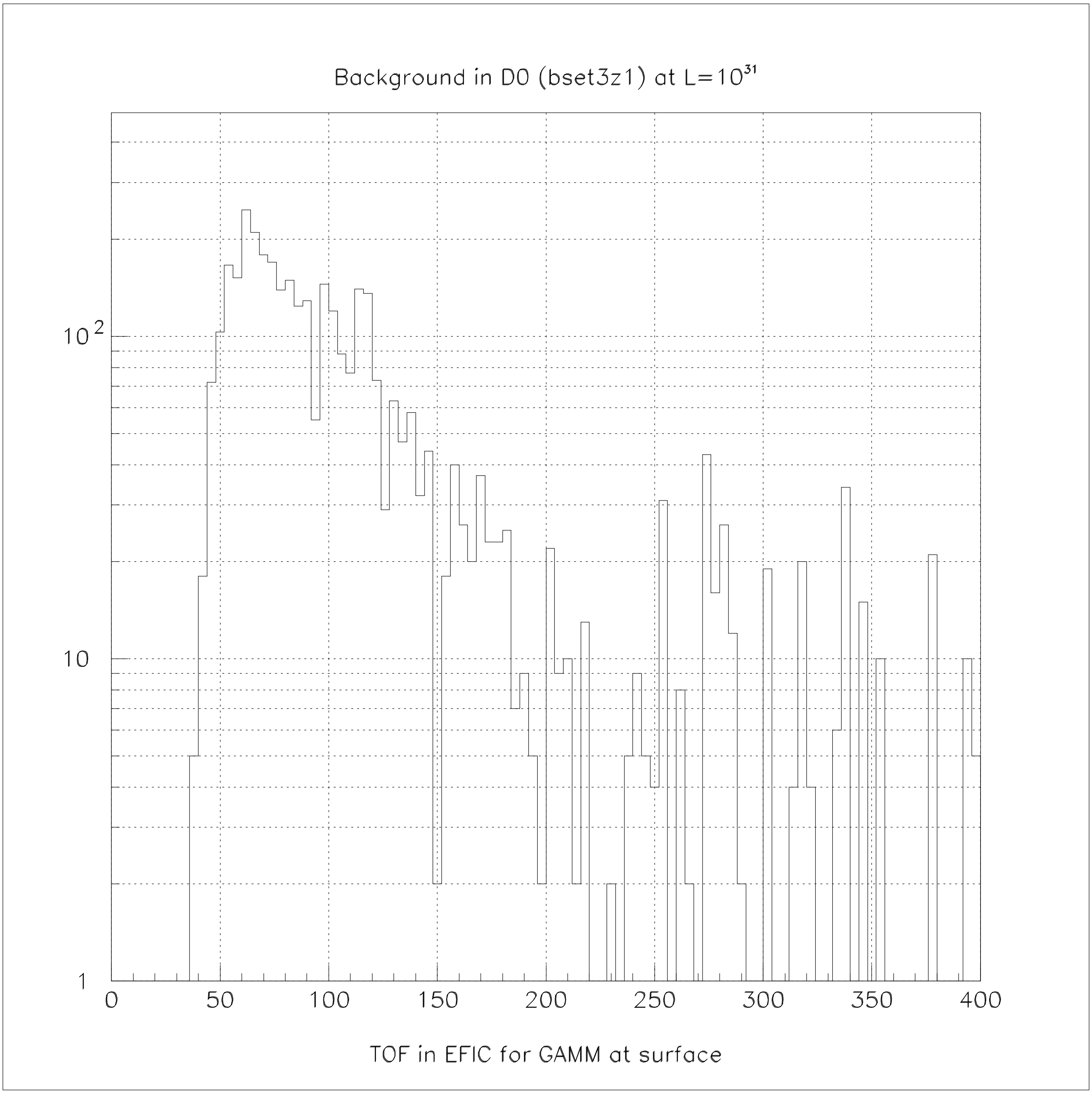

Figure 10: Time distribution of hits in C-layer of muon detectors. The real muon peak is at 27 ± 7 ns.

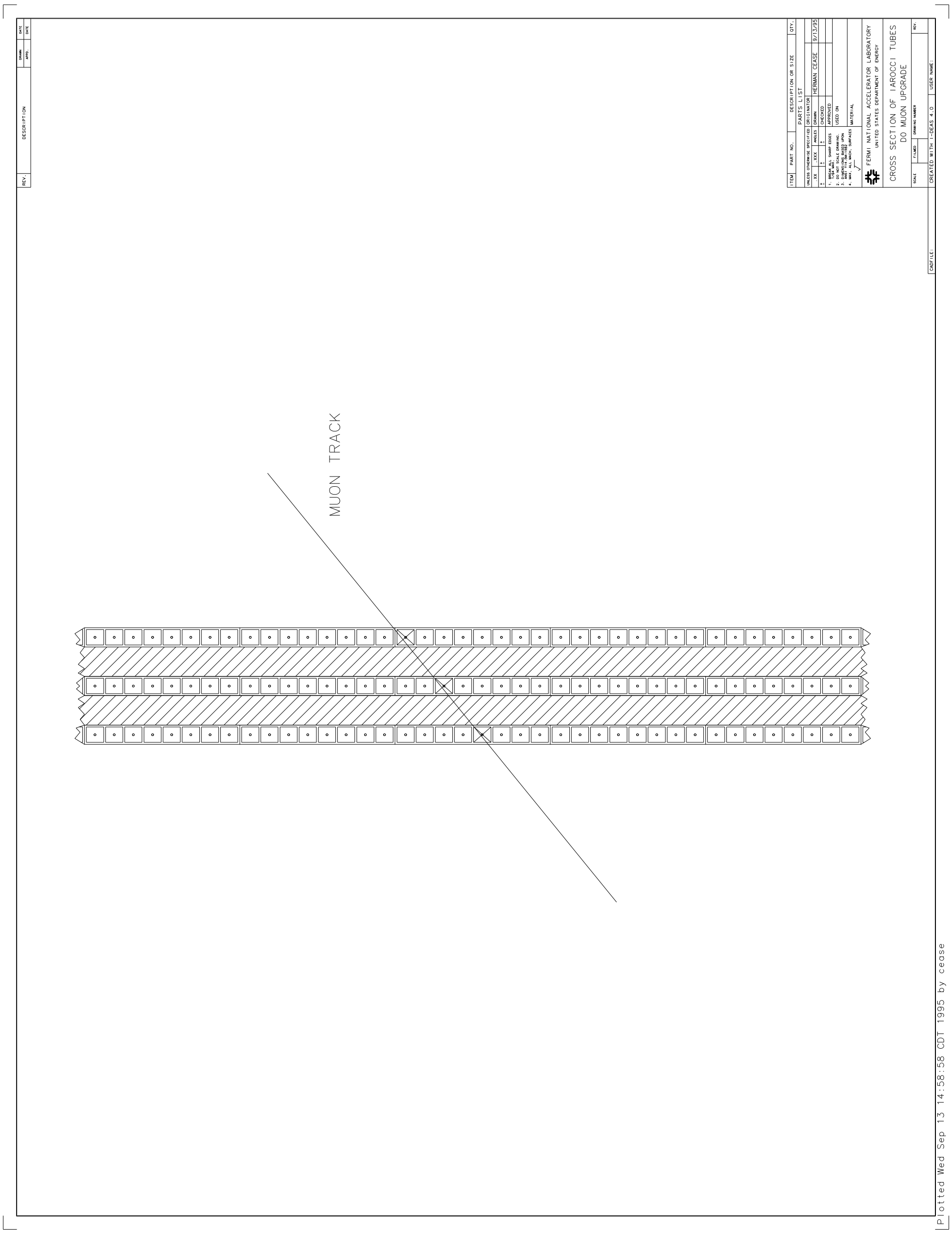

Figure 11: Iarocci B and C-layers design

Estimated time needed for production of all tubes is 6 months.

We plan to use existing SAMUS High Voltage (HV) and gas systems. HV power supplies can produce currents sufficient for operation at Run II design luminosity. In total, 48 HV channels will be used: one per octant (see Fig. 9).

We plan to use Iarocci tubes for track reconstruction and triggering. Due to the reason that gate width can be set below the 132 ns bunch crossing time, simple amplifiers/latches can be used. Use of $R-\phi$ pads on the surface of Iarocci planes (pick up electrodes) can be used for additional background trigger rejection. Studies are in progress to estimate the efficiency of such pick up electrodes.

Using a simple 4 bit TDC, the coordinate accuracy of Iarocci tubes can be improved to σ = 0.3 mm. In this case survey and other problems mentioned above will limit muon detectors coordinate accuracy.

The experience with SAMUS tubes shows that integrated charge of 50 C/cm of anode wire can be accumulated without changes in gas amplification using freon-methane gas mixture (similar to one we propose to use for Iarocci tubes). The preliminary studies of Iarocci tubes show that there is no outgassing from their internal surfaces. These facts let us predict that Iarocci tubes can run for many years at $\mathcal{L} = 1 \cdot 10^{33}$ cm^{-2} s^{-1} without aging. Study of Iarocci tubes aging with selected mixture in proportional mode is under way.

Although major characteristics of Iarocci tubes are pretty well known there is a list of important tests to be done before mass production will be started:

1. Studies of tube aging
2. Detection of signals from tubes up to 5 m long
3. Mechanical accuracies of large planes of Iarocci tubes
4. Optimization of gas mixture
5. Study the sensitivity of Iarocci tubes to neutrons and gammas

4.3 Scintillation Pixel Counters

Time and energy spectra of background particles are substantially different from similar distributions for muons. Scintillation counters will count substantially less background hits than other types of detectors [28, 20]. Use of 20 ns gate instead of 100 ns reduces the number of background hits per plane by ten times (keeping 100% efficiency of muon detection). The MIP energy deposition in 1/2" plastic is 2.5 MeV. Setting detection threshold at 0.5 MeV will reduce counting rate due to neutrons by a factor of 3 [29]. Scintillation counters will be substantially (factor of 10-30) less sensitive to backgrounds than Iarocci tubes.

We propose to install 3 layers of scintillation counters (A, B and C-layers) with 4.5 degree in ϕ and 0.1 in η segmentation (Fig. 12). This segmentation looks attractive taking into account multiple scattering, match with fiber tracker (4.5 degree), minimum range out muon momentum, background trigger rates, and number of channels [7]. Each plane consist of two sub-planes used to remove dead zones between counters. The maximum counter size is 60×110 cm^2.

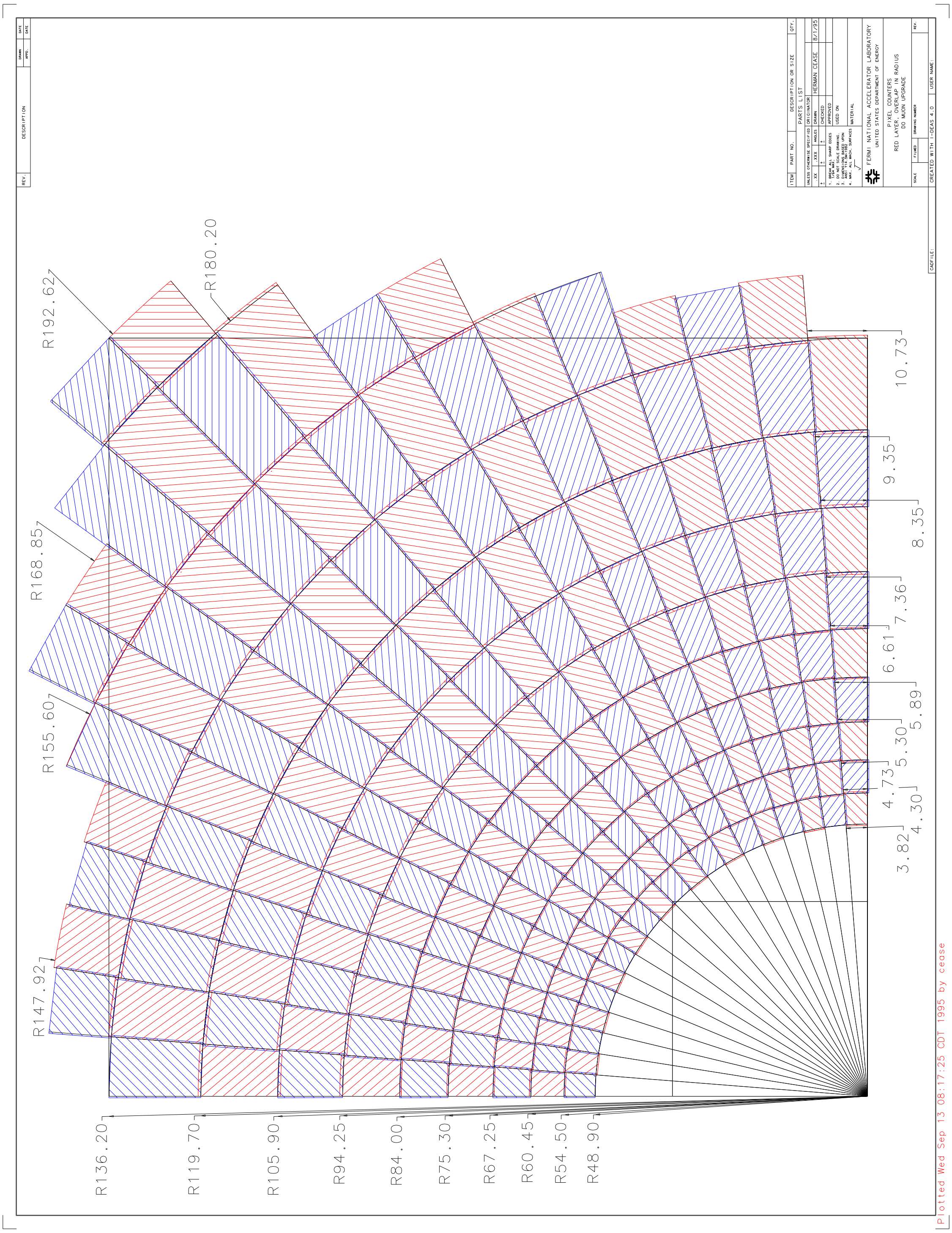

Figure 12: One quadrant of scintillation pixel plane.

There are two options for the pixel counters design which are under detailed studies now. The first is based on two WLS bars used for collection of light onto the photomultiplier photocathode [28], see Fig. 13. The high transparency of Bicron BC404A 1/2" scintillator provides a large number of photoelectrons (more than 60 even for the largest counters) and good uniformity (around 10%). In the second design 12 1 mm diameter WLS fibers (Bicron G2 fibers with decay time of 2.7ns) are installed over counter perimeter to collect light from 4 sides of the plastic. This design has the advantage of better photomultiplier connection and counter design, but less photoelectrons and a more complex assembly/production procedure. A time resolution of 0.8-1.4 ns has been obtained for test counters. Both counter designs use 1" photomultipliers 115M from the MELZ factory.

Vertex position, interaction time, different time of flight between interaction point and scintillation counter limit the required time resolution to 1-1.5 ns. In order to be fully efficient to muons, a gate width around 15-20 ns will be used.

In order to make an efficient energy deposition cut, the response of the counters should be uniform over its surface and the number of photoelectrons should be sufficient (> 30). Uniformity studies of prototype counters are in progress.

The photomultipliers are the most sensitive element to aging in the scintillation pixel design. The typical integrated anode charge after 3 years of operation at $\mathcal{L} = 1 \cdot 10^{33}$ cm^{-2} s^{-1} is $2 \cdot 10^2$ C. In Fig. 14 the typical aging curve for the PM 115M is shown. The drop in gain is less than 20% for $2 \cdot 10^2$ C and can be compensated by an increase in HV.

The total number of counters in the proposed system is 4.8k. They are grouped into octants matching Iarocci octants. There are around 96 counters per octant (this number slightly depends upon the corner-filling method).

The typical HV for photomultipliers is 1.8-2.2 kV and base current is around 0.2 mA. We plan to connect 16 photomultipliers (preselected with similar operational HV) to a single HV channel. The energy threshold for individual counters will be adjusted using variable electronics threshold (similar to existing Cosmic Cap electronics). The HV modules used for the DØ central tracking detectors in Run I are planned to be used. Some additional number of HV modules/crates may be needed - we will specify requirements after prototype counters are studied.

Calibration of scintillation counters (time scale and amplitude) is necessary in order to keep high efficiency of muon detection. There are two options under consideration now: use of a special calibration system (based on generator driving LEDs) or use of muons with low p_T (around 3 GeV/c) produced at interaction region. At $\mathcal{L} = 2 \cdot 10^{32}$ cm^{-2} s^{-1}, the inclusive muon rate will be of order $1{\cdot}10^2$ Hz. Estimates show that we can collect around $5{\cdot}10^2$ events per counter during a 30 minute calibration run. In order to select appropriate calibration scheme we plan to perform long term stability studies using pixel prototype counters.

The following is our plan for pixel counter studies:

1. Study characteristics of prototype counters and select pixel design
2. Perform long term stability (gain and time) studies and specify calibration system requirements
3. Perform aging studies of large sample of photomultipliers

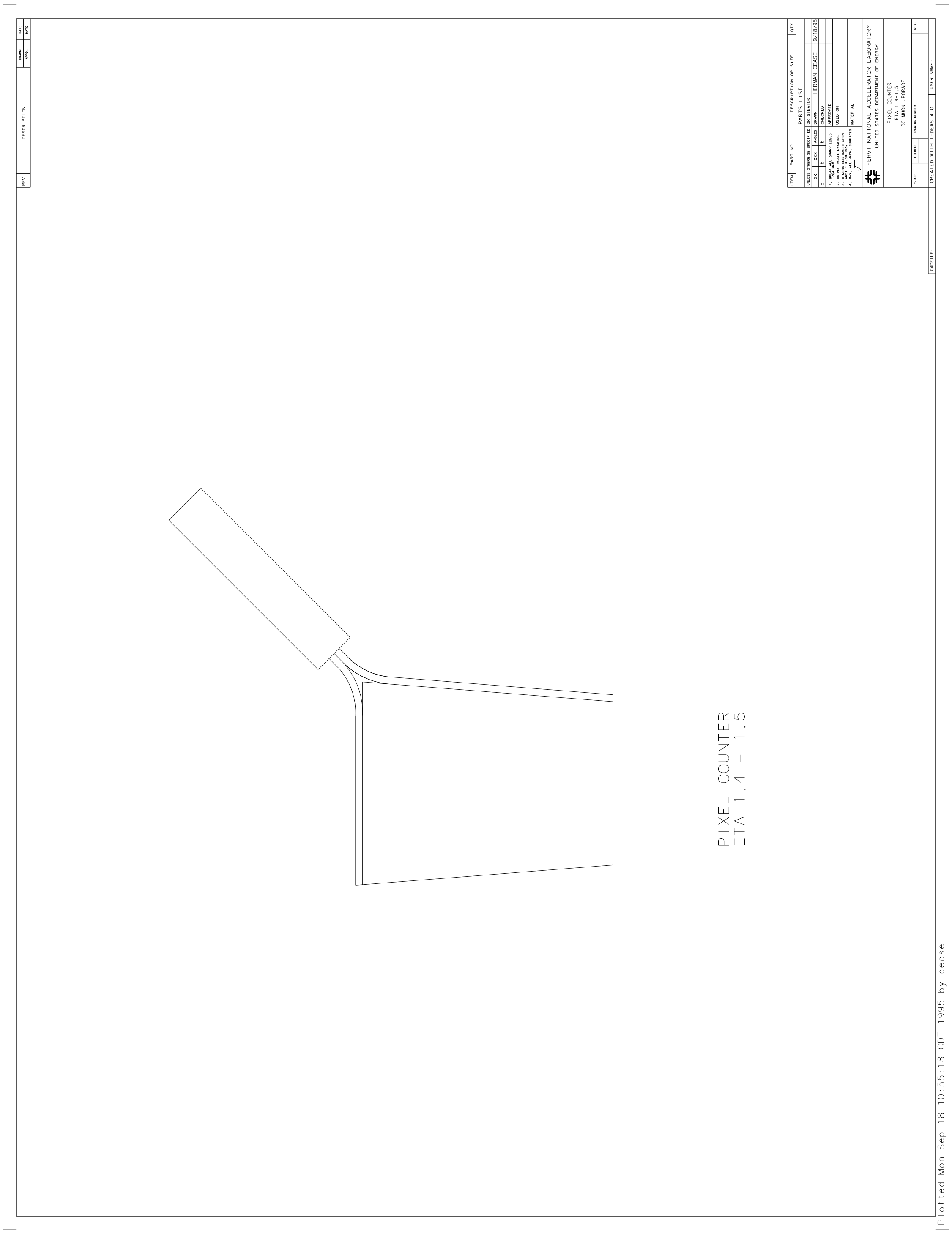

Figure 13: Design of pixel counter based on WLS bars.

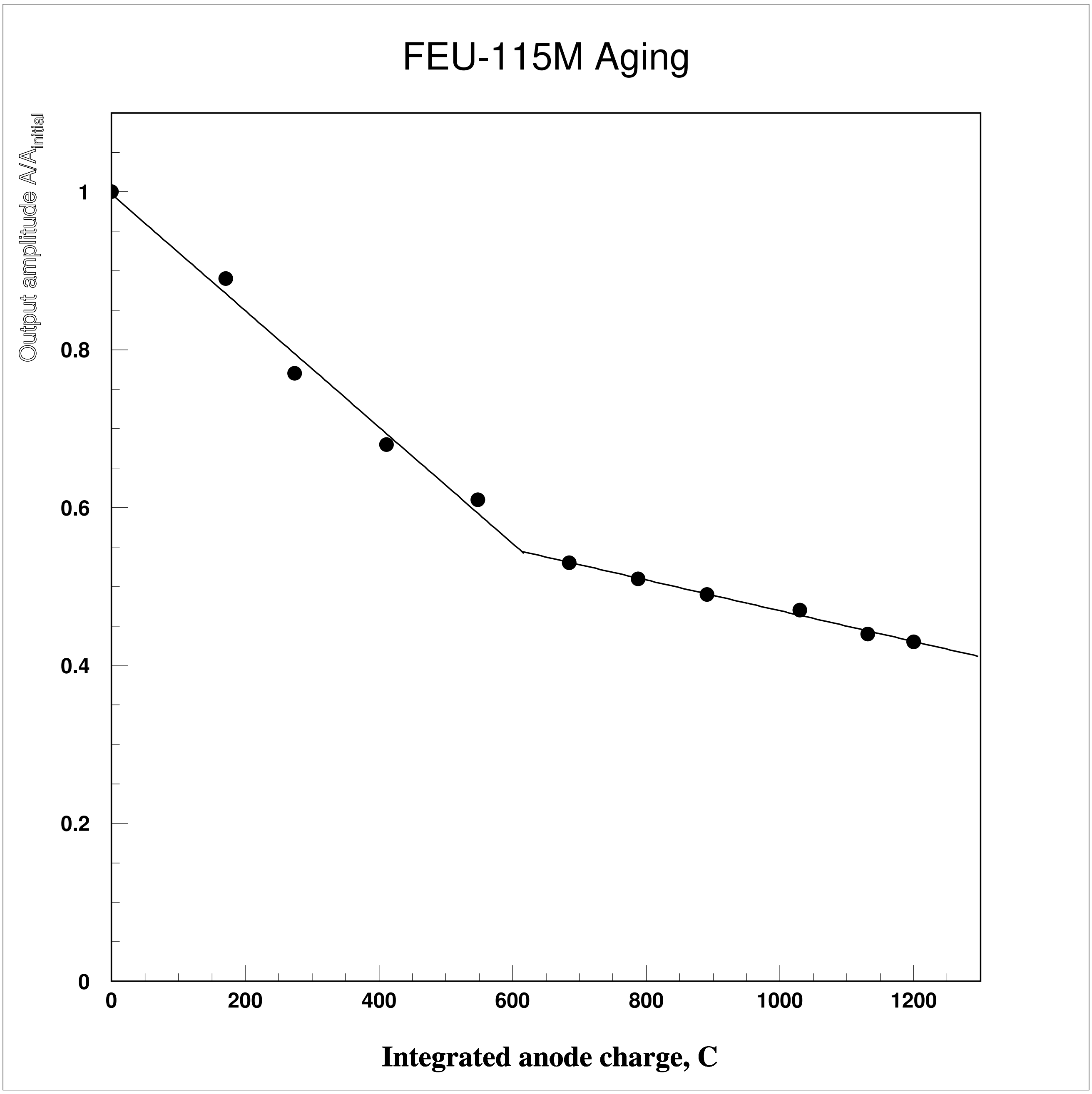

Figure 14: Gain as a function of integrated anode charge for PM 115M.

4. Optimize base current and specify HV system requirements
5. Optimize magnetic shielding design (maximum field in the region of photomultipliers is around 380 Gauss)

4.4 Triggering and Background Rejection

There are two major components in the trigger rate at a given luminosity: real muon rates (π/K decays, heavy quark decays, W/Z, Drell-Yan, *etc.*) and background (combinatoric) rates. The single inclusive muon rates can be estimated with high precision using measured muon cross sections at $\sqrt{s} = 1.8$ TeV [30]. The typical single muon rate for $p_T > 3$ GeV/c is of order $1{\cdot}10^2$ Hz at $\mathcal{L} = 2 \cdot 10^{32}$ cm^{-2} s^{-1}. The real muon rate is reduced to a few Hz for p_T above 10 GeV/c threshold. The combinatoric background is considerably more difficult to estimate. The typical rejection needed from inclusive muon trigger is $1{\cdot}10^6$ and therefore $1{\cdot}10^6$ Monte Carlo events are needed in order to make direct calculations. Clearly this method is impossible to use. There are methods of background trigger rates estimation which use different methods of simplification: assuming absence of correlations between hits in different planes [7, 8] or performing Monte Carlo calculations at high background levels (where trigger rejection is lower) and extrapolating to lower background levels [28].

All background rates estimations are sensitive to number of interactions per crossing, shielding, timing rejection of backgrounds, and tails in multiplicity distributions. The combinatoric rates for three planes of pixel counters are proportional to the third power of individual counter occupancy. So an increase in background rates by a factor of 2 will cause almost an order of magnitude increase in the combinatoric trigger rate.

Typical fluxes of electrons/positrons vs. distance to the beam axis are presented in Fig. 15. For $|\eta|$=2, the distance from beam pipe is around 1.5 m. In this region the variation of background fluxes are relatively small. Using average flux from Fig. 15 and method from Ref. [7], we can estimate the single muon trigger combinatoric rates for pixel counters. For $\mathcal{L} = 2 \cdot 10^{32}$ cm^{-2} s^{-1} and bunch spacing of 396 ns, the rate will be around $2{\cdot}10^2$ Hz ($1.0 < |\eta| < 2.0$). The accidental coincidence rate is proportional, in our case, to $\mathcal{L}^3$ (where $\mathcal{L}$ is $p\bar{p}$ luminosity) while real muon rate increases only linearly with luminosity. Any correlations between hits in the A, B and C-layers will increase background trigger rates. Extensive studies are needed in order to make more accurate background rates estimations. The direct measurements of correlations are planned using test pixel counters installed in the collision hall for Run Ic.

The occupancy of individual counters at $|\eta|$=2.0 is around factor of 5 lower than at $|\eta|$=1.0 (due to much smaller counter size). Taking into account the relations mentioned above, the combinatoric trigger rate per unit η at $|\eta|$=1.0 will be $1{\cdot}10^2$ times higher than at $|\eta|$=2.0. This effect will be used in order to compensate for loss of CFT rejection power at $|\eta|$ above 1.6.

The muon Level 1 trigger will include scintillation pixel counters, Iarocci tubes, and the central fiber tracker. The same devices, with finer segmentation, will be used at Level 2 trigger. All DØ detector elements (including calorimeter for muon energy deposition confirmation and central tracking detectors) will be used for muon identification at Level 3 trigger.

Use of Iarocci tubes at Level 1 trigger has two substantial advantages: the possibility

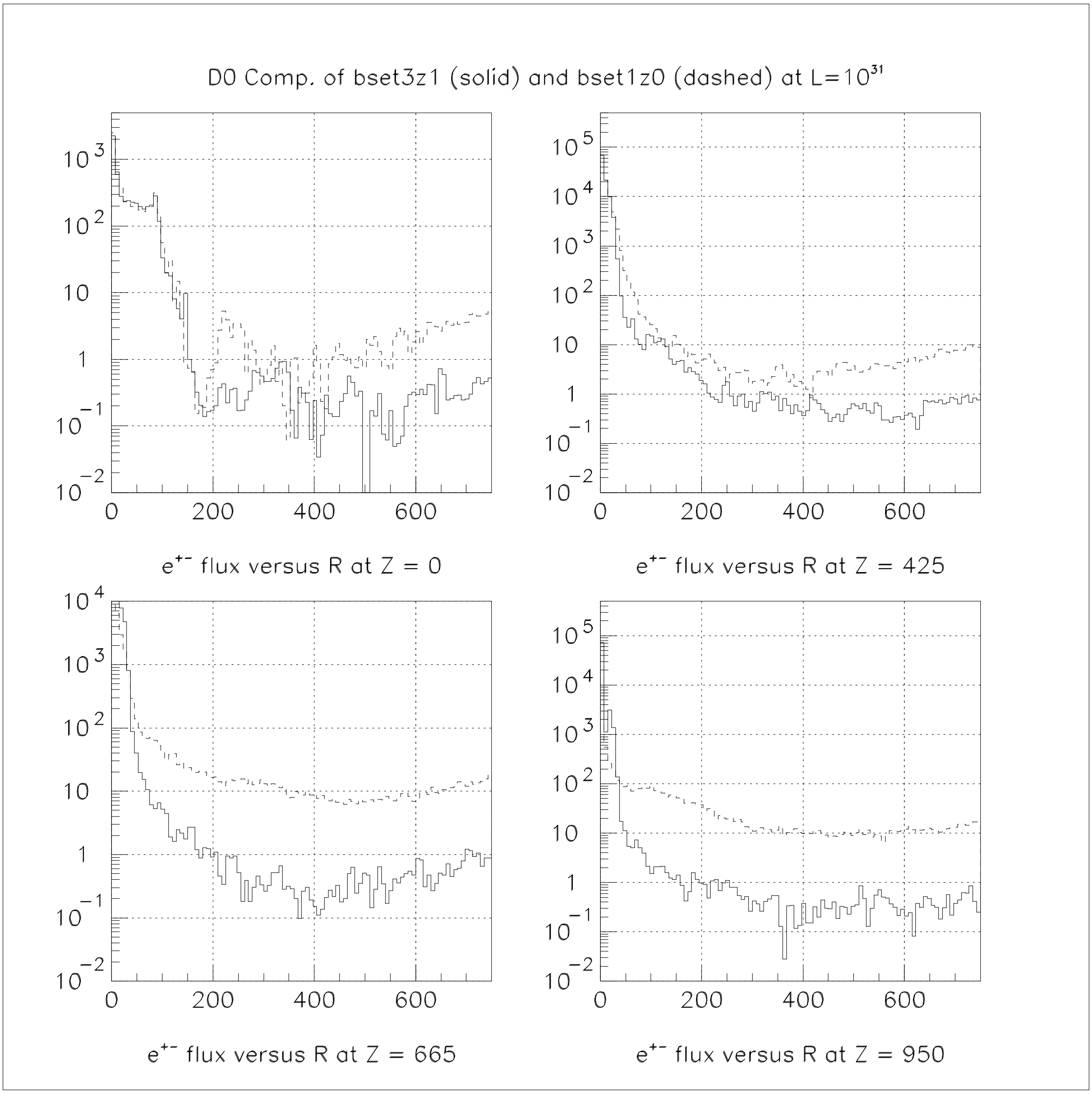

Figure 15: Radial (in cm) electron/positron flux distributions for different z positions: for unshielded (dotted) and shielded (solid) scenarios. The luminosity for this plot is $1 \cdot 10^{31}$ $\mathrm{cm}^{-2}\ \mathrm{s}^{-1}$.

to make high p_T trigger (scintillation pixel can provide p_T cut at 3 GeV/c or below) with edge around 10 GeV/c and additional reduction of combinatoric background. Even for the conservative assumption that hits in planes of one layer are 100% correlated, the method [7] gives us an Iarocci-based rejection of combinatoric background triggers by a factor of $1{\cdot}10^2$ ($\mathcal{L} = 2 \cdot 10^{32}$ cm^{-2} s^{-1}, 396 ns bunch crossing time). Taking into account possible match between Iarocci-octant and pixel-tower additional background rejection can be obtained.

4.5 Summary

Iarocci tube planes and scintillation pixel counters are proposed to be used for muon triggering and track reconstruction in the $|\eta|$ region 1.0-2.0 of the upgraded DØ detector.

We plan to install A-layer detectors using frames mounted on the EF surface. Use of existing EMB and EMC trusses is planned for installation of B and C-layer detectors. Mounting, cabling, survey and commissioning of detectors can be done almost completely before the detector rolls into collision hall. Front end electronics [17] for Iarocci tubes and pixel counters will be installed on the detectors (partly) and in VME crates situated in the collision hall.

The proposed detectors exploit the best features of the existing DØ detector (thick calorimeter and iron magnet, small π/K decay volume, high muon detector η coverage, etc.), and add additional unique features such as high rate capabilities, good time resolution and the absence of radiation damage. Our estimates show that the proposed detectors can be used for muon triggering and track reconstruction up to the $1 \cdot 10^{33}$ cm^{-2} s^{-1} range.

5 Electronics

5.1 Introduction

5.1.1 Use of Existing Systems

In order to operate the existing detectors at high luminosity, the existing "service boards" will need to be rebuilt, as the current limitation resistor-capacitor networks are inappropriate to the Main Injector rates [31]. As for the cable plant, we plan to use the existing coaxial cable runs in order to serially transmit front end data to the Movable Counting House (MCH) and the Level 2 trigger system. The Level 1 trigger system will now reside in the platform under the detector, and the use of newly available serial data links will greatly simplify the problem of installing the cable plant carrying trigger system inputs. The slow control system using the 1553B protocol will continue in service.

Obviously the plan is to use as much of the existing infrastructure as is possible, while taking care to use new technology where it solves an existing problem, *e.g.* serial data transfer to the Level 1 trigger.

5.2 WAMUS Electronics Design

This is most developed part of the project. Intensive studies has been made during 1994 to understand the changes in the electronics design we propose. The readout part of the WAMUS electronics is the basic model for the fast trigger detectors design. We have also attempted, with transformer isolation and bandwidth limitation, to achieve lower discriminator thresholds. The goal is to run at lower gas gain, to minimize integrated charge at the high luminosity expected.

5.2.1 Wire Amplifier Design and Tests

The existing amplifiers are implemented as thick film hybrids. They are physically very fragile and would be very difficult to remove from the present mother boards for use elsewhere. It is now possible to make preamps of comparable performance taking significantly less power, using fewer discrete components. We have tested many wire amplifier candidates and the most promising of these is shown in Fig. 16. The design proposed draws 15mA per channel from $\pm$5V supplies as opposed to the 47mA from the present wire amps. The noise performance is essentially unchanged but is achieved with ICs rather than discrete components. We measure a signal to noise of about 12:1 with a 1 μA pulse. The differential inputs will guarantee better immunity to parasitic crosstalk from the digital part of the board. The rise time can be adjusted in a range from about 6 to 15 ns with a single integrating capacitor. We have studied the effect of changing the rise time of the existing version of the wire amplifier. The ΔT resolution improves with a slower rise time at the expense of time resolution. The contribution to the measurement error from the electronics time slewing is less than that due to diffusion effects in the gas ($\sim 250\mu m$ or $\sim$ 3 ns in fast gas), which means that we have some margin to work with. An optimum point needs to be found and the appropriate rise time set on the amplifier. The discriminator used has excellent 2x to 20x over threshold delay skew characteristics of less than 2 ns as compared to more than 5 ns for our present comparators. A feedback capacitor on the discriminator fixes its output width at 40 ns. The total component cost is around $10 per channel and off the shelf commercial components are used. It is our intention to mount the amplifier components directly on the large front end boards of WAMUS. A 16 channel double density section has been laid out and tested. This is the possible solution in case of limited PC board space.

Ground loops have proved troublesome in the present system. As a result of this experience, we are adding transformer coupling at the service boards to provide true differential connection and avoid a low impedance ground path between the chambers and the preamplifier inputs.

5.2.2 Wire Triggering - Delay Line and L/R Ambiguities

Presently, the trigger information comes from discriminated and latched pad signals. That scheme necessitates the equalization of the wire and pad thresholds and a long plateau as the two pads which share the signal are discriminated and then logically "ORed".

We have studied the use of a lumped constant delay line in series with the jumper between the far ends of the tube pair, shown in Fig. 17. By separating the time of arrival by about 20 ns, it is easy to use a "first arrival wins" circuit to determine which tube was hit. A sample delay has been ordered and tested, with satisfactory ΔT resolution on the test chambers in the assembly hall. A plot demonstrating the ability to separate a hit within a pair using this separation scheme is shown in Fig. 18.

5.2.3 TMC Chip - Performance Specifications and Tests

Presently, the drift time is measured in time-to-voltage analog circuits (TVCs), while the time difference between adjacent wires which are tied together is measured in distinct ΔTVC analog circuits. The analog electronics requires a comprehensive calibration scheme for the time measurements. The proposed digital scheme essentially requires no calibration.

Yasuo Arai leads a group at KEK that has developed a four channel pipelined digital TDC chip called a TMC (Time Memory Cell) [34] which matches our needs very closely. It has a 32 bin interpolator that cycles once per external clock. This 32 wide bit map is encoded to 5 bits and written to an internal dual port memory once per clock cycle. At each clock cycle, a new 5 bit word appears at the output delayed by a specified number of clock cycles up to 128. The bin width when run at 26 MHz is 1.2 ns and the maximum delay is 4.8 μs, enough to cover the stated Level 1 trigger latency of DØ of 4.1 μs. The pipeline can store one hit per clock cycle, which in a practical sense, means that there is no limit to the maximum number of wire hits recorded during one drift time interval.

The time of arrival difference between each end of the tube pairs is used to break the ambiguities of the repetitive pad pattern. For a least count time ΔT, the resolution is $\sim c \cdot \Delta T/5$. Therefore, to resolve the pads (L = 61 cm), with a resolution of 30 cm, means a least count of $\sim$ 5 ns. We propose to calculate ΔT by subtracting time values from adjacent tubes. We have modified the time channel of a test tube pair by connecting two TVCs to its ends to test this idea. The comparison of the resulting resolution to that of the ΔTVC data shows no significant difference.

The drift times themselves are the information containing the greatest physics content

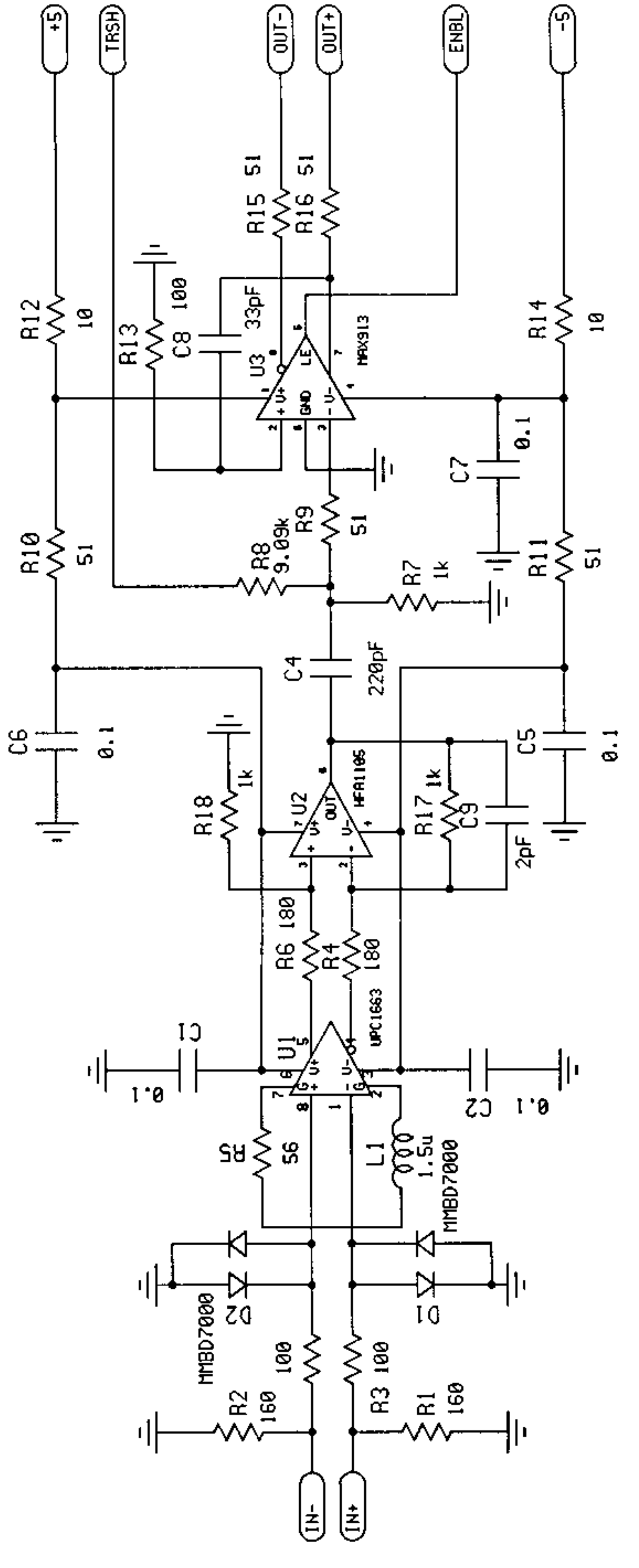

Figure 16: Wire signal amplifier schematic diagram.

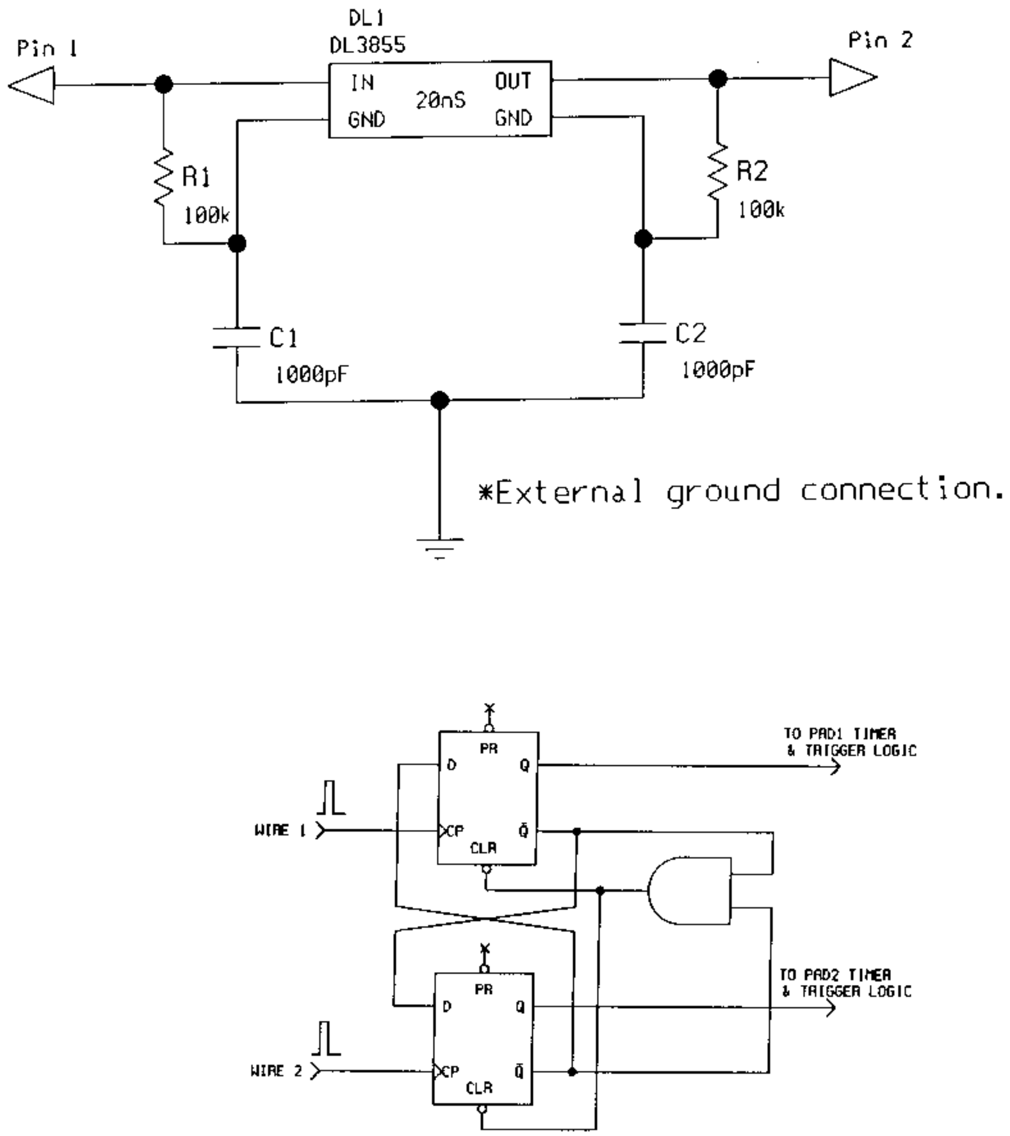

Figure 17: Delay line jumper schematic diagram.

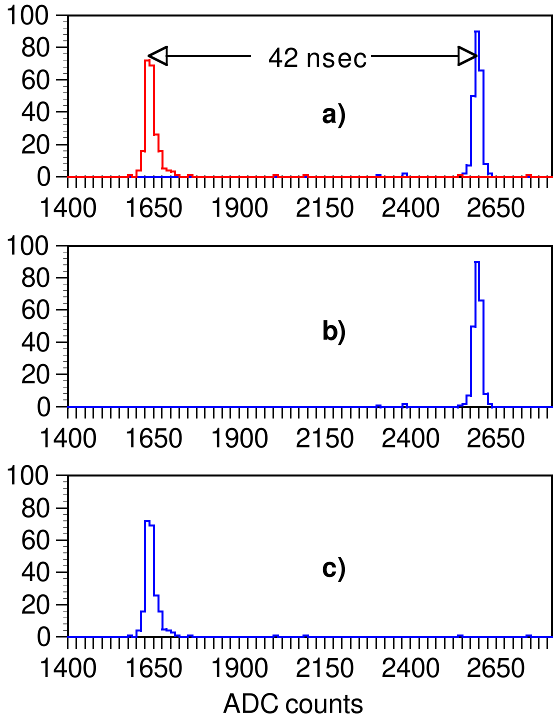

Figure 18: ΔT distribution with a $10{\times}10$ cm^2 scintillator trigger at one end: (a) No tags, (b) Wire 1 tag, and (c) Wire 2 tag.

within the muon system since they determine the muon momentum. On a test chamber using cosmic rays, we achieved a 0.4 mm resolution. For WAMUS, even with a fast gas (V_d^{-1} = 16 ns/mm), this implies a time resolution of 6.4 ns or a least count of 22 ns. Clearly, the time difference requirement drives the specification and the TMC resolution makes a small contribution to the drift distance measurement error.

Since the data from the TMC is only 5 bits, an external counter keeping track of the number of elapsed 1/26 MHz cycles with enough range to span the maximum drift time will be required. This counter is common to all channels, so only one per several channels will be needed. Level 1 accepts can arrive on any 53 MHz cycle, either at the beginning or the middle of a 1/26 MHz cycle. We will attach the eight-bit crossing-number from the Level 1.0 accept signal to the event data and use its least significant bit as a marker to delineate between "even" and "odd" triggers.

We have 200 TMC chips on hand, and additional 3500 have been ordered. We have received test results of differential non-linearity (the dominant error source in this type of design) from William Burton at IONWERKS Inc. The TMC chips show very good agreement with their original specifications. The standard deviation from a linear fit is measured to be less than or equal to the bin width. This confirms the results of a similar test performed by Arai. He measured 0.3 ns RMS for 40 MHz operation [35].For a scalar based timing device such as this, the integral non-linearity is the change in frequency of the clock that occurs during the measuring interval; in our case a negligible value. Obviously there is no need for time calibration for the TMC chip. The time scale is determined by the clock frequency of the chip which is synchronized to accelerator RF.

The cost of the TMC in small quantities is quoted to be about $12.75 per channel. The input and clock signals are differential CMOS levels ($\pm$100mV at $V_{cc}/2$). This should help reduce digital interference with the low level signals. It should be noted that this device gives us the ability to build a dead-timeless readout, so long as any buffers placed downstream in the data path do not fill.

We are in the process of completing the design for our so called Front End Board (FEB). We should begin the laying out of a prototype shortly. We will then be able to perform system level tests on the TMCs.

5.2.4 Pad Amplifier/Gated Integrator - Design and Tests

At present pad charges are sampled synchronously with the bunch crossings. This scheme only works when the beam crossing intervals are longer than the drift time, and the likelihood of multiple hits per crossing is small. This is clearly not the case for Run II. The pad charge sensitive preamplifier (CSP) takes nearly 1 μs to fully collect the charge from the pad signal and has a decay time constant of 40 μs which limits the counting rate of the channel to a few kHz. This long time constant has already been a source of major problems in Run I at 1/10 the luminosity of Run II. There are two components to the pad signal, the faster component appears to deliver the majority of the charge in about 350-400 ns. It is our plan to sample only for this length of time. As soon as we have some test channels, we will measure the resolution with short sampling times. If short times are to be used, it is important that the samples are more closely correlated to the arrival of the signal.

For the present run, we were forced to modify 8000 CSPs to shorten their integration time constants to prevent them from saturating. For this reason we will implement a reset switch on the next version of the charge integrator. We have reduced the input impedance of the new pad signal preamplifier in order to collect the pad charge as rapidly as possible. The intrinsic rise time of the old CSP with a lumped input capacitance of about 700 pF to represent the pads is measured on the bench to be about 150 ns which translates to an input impedance of about 65 Ω, a significant contribution to the collection time of the fast component. The impedance of our new CSP should be in the range of 45 Ω. After a series of studies a bipolar transistor input gated integrator has been designed and tested on the bench. We have traded away some noise performance for improved rise time and input impedance. An accurate noise comparison between the new and old design is difficult because of the differences in the sampling schemes. According to our measurements, the new pad integrator has about the same wide band RMS noise (1.2 mV) as the old CSP and the same gain (300 mV/pC). The recovery time of the integrator is about 20 ns which allows us to use a reset pulse 50 ns wide.

5.2.5 Pad Signal Processing - Pipelined ADC

The pulse height ratio in the pads yields the coordinate orthogonal to the drift distance. For the pad repeat pattern of L = 61 cm, we achieved a best resolution of $\sim$2 mm on a test chamber. In order to achieve that resolution we need to make a 1% measurement of the individual pad pulse heights.

We have done studies of the precision requirements for the pad measurements. Pad data with 12 bits of resolution from the present run was truncated by degrees and the resulting resolution was plotted. It is clear that there is no degradation in measurement accuracy at 10 bits. A 10 bit 15 Msps ADC costing less than $10 has recently become available which makes it practical to attach an ADC to each integrator output. The ADC is pipelined, that is, the digital value of for a particular input analog sample appears at the output after a three clock cycle delay. At a sampling rate of 13.25 (53/4 MHz) Msps, we have about 225 ns of latency to form the "base" tag bit which is appended to data word written to the buffer connected to the ADC output. After an interval equal to the charge collection time plus the ADC latency, a "peak" tag is appended. The block diagram of the pad channel and its timing are shown in Fig. 19. The discriminator signal is asynchronous with respect to the ADC clock, so that we have a signal time to sample time uncertainty of one sampling interval, or about 75 ns. After the pedestal and signal samples have been taken, the integrator is reset with a delayed copy of the wire trigger signal. The repetition rate of the pad digitizer circuit is limited to about 2 MHz per wire, a large increase over the few kHz rate presently sustainable. Two hits per drift time will be accommodated if they are at least 500 ns apart.

5.2.6 Trigger Logic

The complete hit map for a particular collision cannot be determined until the maximum drift time has elapsed. The strobe for the trigger logic must be a copy of the bunch crossing delayed accordingly. The separator outputs fire retriggerable digital one-shots clocked at 53 MHz, whose output width is set to the maximum drift time. The purpose of these one-shots is to lengthen the discriminator signals to such an extent that the signals from the shortest drift time persist until the sampling point. Since the storage time of the detectors is greater

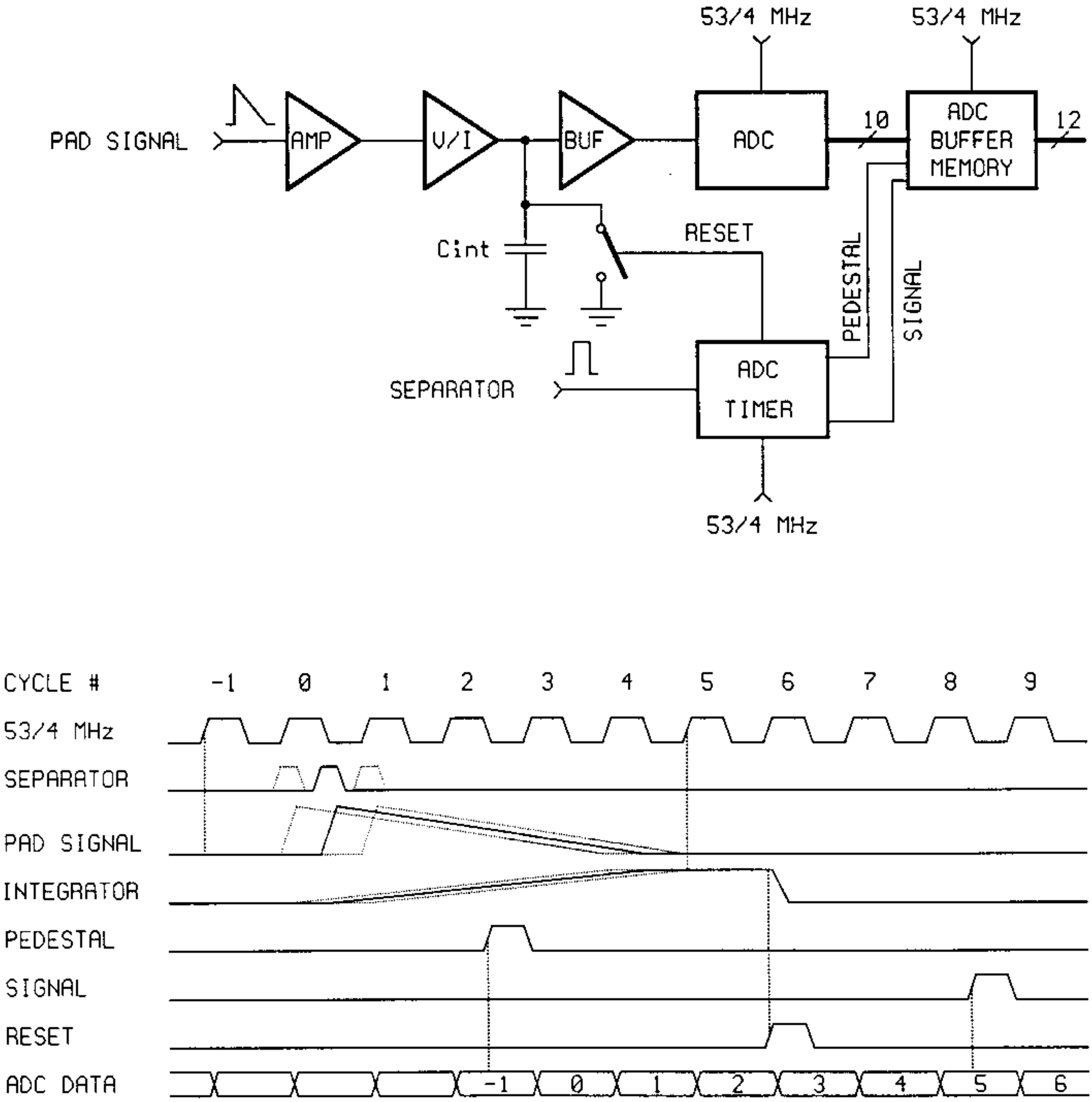

Figure 19: Pad channel schematic and signal processing timing diagram.

than the crossing interval, the trigger logic cannot correlate hits and crossings. It can only produce a list of trigger candidates. It is clear that for a longer drift time, more crossings will have elapsed, and thus more candidates will be present. The worst case trigger candidate rate will be greater than the single wire counting rate by some multiple of the ratio of the drift time to the crossing interval. The drift time for a track going through multiple layers is different for each layer. Therefore the one-shot outputs used to form the hit map will overlap for a fraction of the maximum drift interval. The collision from which the hits originated can only be resolved with the previously mentioned auxiliary detectors. The Level 1 trigger hardware will use the auxiliary fast detectors to weed out most of the false candidates.

5.2.7 Trigger Timing and Synchronization

The need to have high rejection and low dead time dictates the use of graduated levels of triggering along the lines presently used by DØ, now referred to as Level 1, Level 2 and Level 3. In order to eliminate deadtime, there must be a way of storing data long enough for a trigger decision to take place. For the TMC, this storage is already present in the chip. Data appears at the output of the device with tag bits to indicate which time slices of 1/26 MHz had a hit. For the ADCs, we must supply a pipeline and tag bits externally. If the inner and outer pad electrodes are being digitized at 13 MHz, the ADC outputs along with the appropriate tag bits (base, peak, overflow, underflow) can be interleaved into a single FIFO at 26 MHz. The depth of the FIFO is adjusted such that the Level 1 accept signal arrives approximately at the same time as the pertinent data shows up at the outputs. If the trigger latency is of order 4 μs, then the pipeline has to be about 100 locations deep.

When a Level 1 accept arrives from the framework, data emerging from the pipeline delays is examined for tag bits. Tagged data is written into a set of FIFOs which are the Level 1 buffers. We propose to use a microprocessor to handle all higher level buffer control operations. These include the transfer of data from the Level 1 buffers into the Level 2 buffers for each Level 1 accept command from the framework, the monitoring of the condition of the Level 1 and Level 2 buffers, and sending a Level 2 busy to the framework as necessary. A block diagram of the buffering scheme is shown in Fig. 20. Given the amount of digital logic within the TMCs and the logic required to pipeline the pad ADCs, the DSP and its logic represents a small increment in the complexity of the board.

In order to reduce the likelihood of synchronization problems and identify the crossing from which the trigger originated correctly, the trigger framework sends a crossing number down to the front ends. This number is compared to a locally generated crossing number, which is clocked through a pipelined delay in the same manner as the data. The data appearing at the output of the pipeline delays must be routed to the Level 1 FIFOs at the point in the past corresponding to the crossing responsible for the Level 1 accept. This could be done by adjusting the timing of all the trigger signals; however, it would not be easy to match all the lines to less than 18 ns over the entire system.

By comparing the values of the local counter and the Level 1 crossing number, the trigger timing is no longer critical, so long as the pipeline delay is greater than the trigger latency. The duration of the transfer from the pipeline delays to the Level 1 FIFOs is programmable and is equal to the maximum drift time for the TMC data. For the ADC, because of the rise time of the integrator signal and a one clock uncertainty in the arrival of the asynchronous

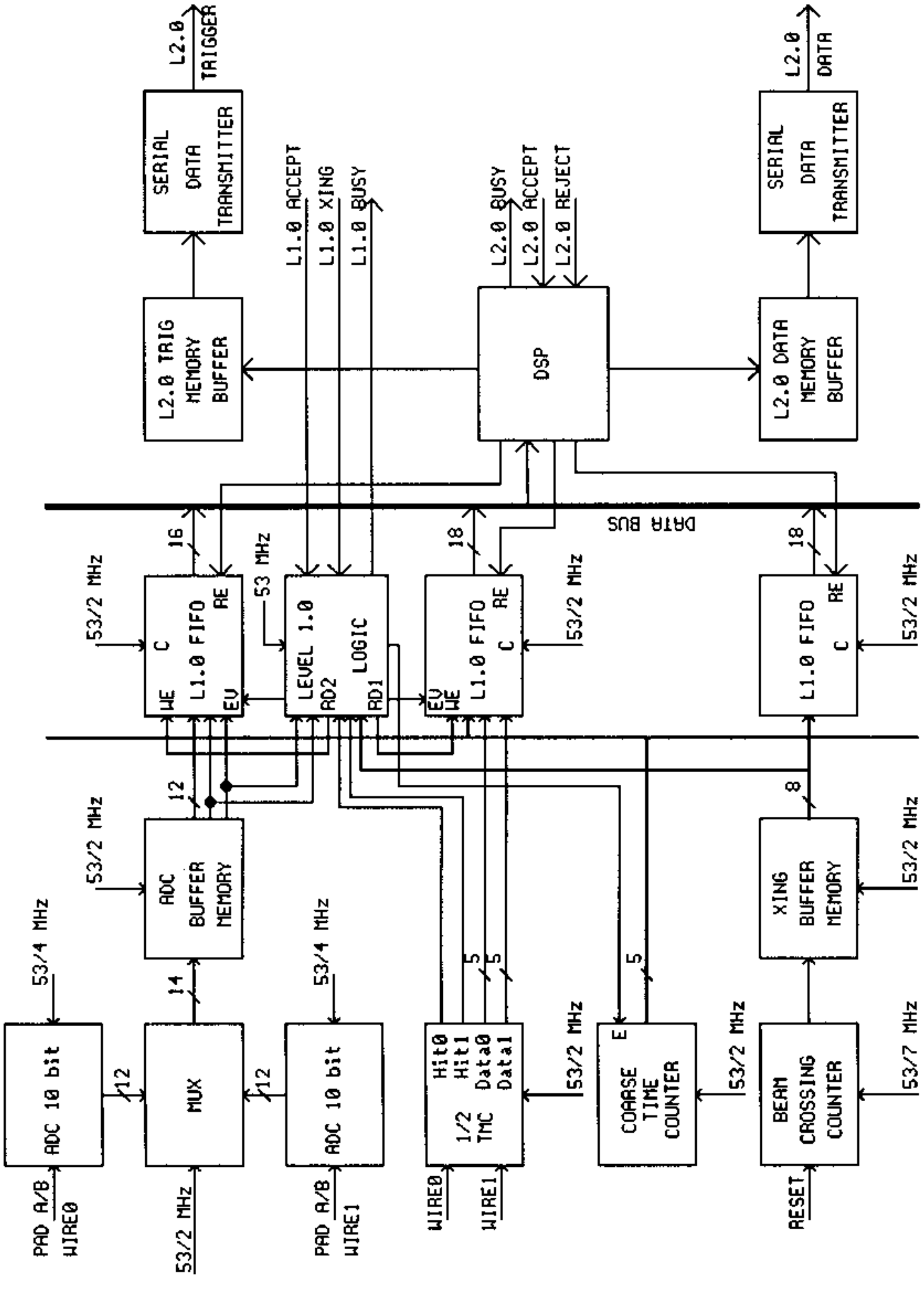

Figure 20: Muon system data buffering and processing.

pad signal, the transfer takes about 0.5 μs longer. There are event boundary words appended to the data stream to keep the events in the Level 1 buffer separate.

It is expected that the proposed Level 1 muon trigger system which has a granularity equal to the existing Level 1.5 trigger, will provide the necessary rejection factor and event selection. With a 100 μs minimum interval between Level 1 accepts this is in principle, due to the buffered nature of the system, the amount of time we have to send data to the Level 2 trigger processor. The finite depth of the system buffers places a limit lower than 100 μs on the transmit time. With 8 buffers as specified by the ECB, 50 μs of transmit time would introduce negligible additional dead time.

5.3 Readout Designs for Scintillator and Iarocci Tube Detectors

In Run Ib, the first of the new trigger detectors was already installed and made operational. The cosmic ray scintillator shield around CF was readout using the SCTB [36]. This board is a 16-fold amp/disc/latch chain with an analog time to voltage converter (TVC). It has a 1553B interface for monitoring of voltages and other quantities, and for downloading test patterns, thresholds, delays, *etc.*[37]. We plan to use the threshold control, pulser control, test mask, and other features in the CB as mentioned in the previous section.

As discussed elsewhere, the Level 1 trigger must report a unique bunch crossing as the source of the Level 1 trigger, and these fast detectors are the source of that ability to "time stamp" the trigger. The fast detectors consist of the Cosmic Cap and the A-ϕ counters for CF, and the Pixel counters for the EF. We also plan to have three planes of Iarocci tubes in the EFs. The electronics for these detectors is similar to that discussed in the previous sections for WAMUS drift tubes. Here we will outline only significantly different details.

5.3.1 Scintillator Counter Electronics

These counters report their TOF data to the appropriate control card. The latched output will be sent to the Level 1 trigger system, as fast timing is needed to break the ambiguities inherent in the WAMUS chambers at high bunch crossing rates. We propose to build a 48 channel Scintillator Counter Card as a 9U VME module. A VME Slave interface of this card will be used for downloading parameters and diagnostics. Each of the inputs will have an amplifier and discriminator with individually controlled thresholds. This feature allows independent control of the energy threshold while using a common HV source for several counters. The arrival time of the signal will be measured in a similar way by the TMC chips. Additional trigger logic will be used to generate trigger bits for the Level 1 system. A simplified block-diagram of the SCC is shown in Fig. 21. Due to the high time resolution of the scintillator counters it is possible to use synchronous gate of 20 ns to latch input signals at each bunch crossing.

The connections between the PMTs and front end card require high density connectors in order to keep single width of the cards. We propose to use RG58 cables to run signals from the PMT to the cards. A signal conversion from single ended signals to differential will be made by wide band transformers. From these transformers, high density ribbon cables will go to the VME cards.

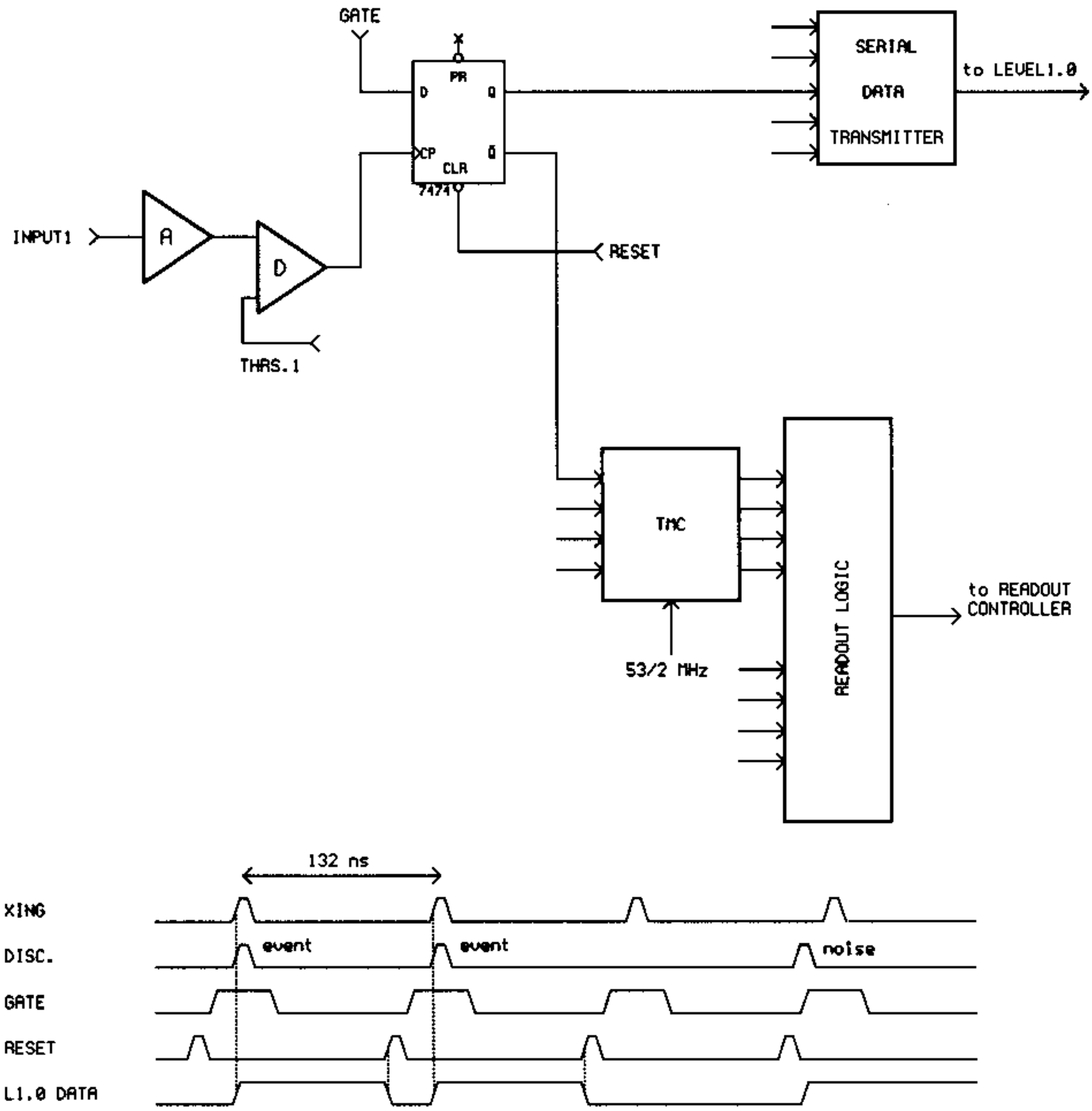

Figure 21: Block diagram of the scintillator detector electronics.

The SCCs will be located in VME crates on the platform. Each crate will have a commercial processor board and a Readout Controller Card RCC. The Readout Controller Card will have a design similar to the WAMUS Control Board. Non-VME J2/J3 backplane lines will be used for fast data readout. The processor board will be used as a ready-made VME master, thus eliminating the need to implement a VME master on the SCC and RCC. With this structure it is possible to accommodate up to 800 channels of scintillator counters per crate. Thus whole scintillator electronics will require only eight 9U VME crates.

5.3.2 Iarocci Chamber Electronics

The implementation of large numbers of electronics channels always pose system level challenges. For a 48,000 wire Iarocci tube system, a high density of the front end board is required. We propose to use 192 channel VME cards to process signals from the wires. Wire preamplifiers similar to WAMUS can be used. Preamplifiers and discriminators will be installed on the chambers and high density ribbon cables and connectors will be used to transfer logical signals to the front end cards. Each input channel will have a latch similar to the scintillator counter card design and digital delay based on commercial 18 bit FIFO instead of the TMC chip. This will allow to maintain the deadtimeless feature for all the components of the muon system. The structure of the front end crates is the same as for scintillator counters.The drift time of the tube is less than 132 ns which will allow fast triggering. High density front end card will accommodate up to 3072 channels in one crate. The whole system will require about 24 9U VME crates.

5.4 Data Processing, Transfer and Buffering

Data from adjacent regions has to be formatted correctly for the Level 1 trigger system. At present, the WAMUS chambers produce up to 96 bits and they are overlapped within the so called MTC10 cards. For scintillator counters there is no overlap implemented in MTC05 cards. The solution is the use of additional data concentrator cards which will combine the operations of merging data from several 48 channel SC cards and provide overlap between neighboring regions.

The outputs of the Level 1 FIFOs are attached to a data bus controlled by a DSP processor. We have simulated various readout and data processing algorithms for two Analog Devices processors ADSP-2181 and ADSP-21060. The latter one is significantly more powerful but has pipelined archtecture which doesn't fit well to our tasks. Because of that we finally decided to make our choice with the ADSP-2181 which in our particular environment has only 20 to 30 percent slower performance. On the receipt of a Level 1 accept, the processor is interrupted and starts its readout sequence, performing the necessary checking of the tag bits and event boundary markers. One event worth of data is added to the Level 2 input queue within the memory of the processor. On a Level 2 accept, the event is moved from the Level 2 input to Level 2 output queue. High level processing is performed here before the events are sent on to the next processing stage. On a Level 2 reject, the appropriate event in the input queue is removed. The time to transfer an event from the Level 1 FIFOs into the Level 2 input queue should not be too large a fraction of the total processing bandwidth available. The mean rate for all Level 1 accepts is stated to be a maximum of 10 kHz and for Level

2 accepts, 1 kHz. This sets the time available for these operations. Some initial simulator results show that the transfer of a representative event to the Level 2 input queue can be done in about 30 μs. In addition to the transfers there are small overheads associated with managing the Level 2 queues. We believe there is still a reasonable fraction of the processing bandwidth available to perform higher level processing.

As far as the Level 1 reads are concerned, there is a trade- off between processor loading and the complexity of the ancillary logic. The above estimate assumes only very simple address decoding logic is used. Hardware that supplies the processor with a leading word count followed by that number of valid data words without requiring the processor to check any tag bits can in principle be built. Under these circumstances, the processor could transfer an event in probably less than 5 μs, but the readout logic is much more complicated.

There are several possible high level processing algorithms that could be performed. The first priorities would be generating an efficient data format and optimal parameterization for the next level of processing. The pad calibration constants can be derived and stored locally. Pedestal subtraction, calculation of the longitudinal coordinate using ΔT and digitized pad charges, and the matching of hits through multiple layers to form a vector are examples of the tasks that could be performed.

From the front ends, the data is sent to the Muon Readout Card (MRC). This card is capable of handling data from two sources. These are two chambers in the WAMUS case or two crates for other detectors. The MRC relays trigger and timing information received from the trigger framework via the Muon Fanout Card (MFC) and receives serial data from the front ends. The card is a VME slave with block read functions specifically tailored to the operation of the DØ VBD card.

The MFC card receives trigger and timing information from the trigger framework and re-drives these signals on the readout crate backplane. It monitors the state of each MRC card and updates a series of internal diagnostic registers. In the event of an error (loss of synchronization for example), these registers can be read as an aid to pin pointing the source of the error. The module keeps track of the crossing number, the Level 1 and Level 2 trigger numbers and appends this information to data sent to the VBD.

5.5 Serial Data Transmission

The trigger logic generates a new candidate list of hit bits at a 53/7 MHz rate (in the case of 132 ns crossings). The need to send trigger bits to the Level 1 processor at this speed defines the bandwidth requirements for the highest speed link in the muon system. One WAMUS chamber can generate a maximum of 96 hit bits. Six 16 bit words must then be sent every 132 ns which is 90 Mbytes/s as compared to our present Level 1 rate of 0.6 Mbytes/s. Until recently, the only reasonably priced option for data transmission of this bandwidth would be a ribbon cable of 50 or more conductors. Even with 0.5 mm pitch cable, routing cables from 160 chamber into modules occupying a few crates would be a very difficult mechanical problem. At most eight such cables could be routed into the front and rear of a standard electronics module. For each Level 1 trigger card, 24 such inputs are required.

Relatively low cost serial links with rates as high as 1 Gbit/s developed for telecommunications have recently become available. These links meet the Level 1 bandwidth requirements and carry data on a single coaxial cable or optical fiber. The plan is to locate the Level 1 system near the detector, with relatively short interconnects, which means the conversion to optical is not necessary.

The Level 2 input bandwidth requirements will be much lower than the Level 1. In the worst case WAMUS chamber can produce 32 hits (30% occupancy). These hits could be encoded in about 120 bytes. If we assume a link bandwidth of 10 Mbyte/s, the event is transferred to the Level 2 processor in about 12 μs, a fraction of the 100 μs Level 1 accept rate. Tests have been performed to determine the maximum bit rate sustainable on the coaxial cables presently used for sending analog data to the MCH from the platform. It appears that 160 Mbit/s rates can be transmitted over these lines, a rate more than adequate for the Level 2 trigger requirements.

For the transmission of the events accepted by Level 2, the bandwidth is even less. The stated maximum mean rate is 1 kHz for Level 2 accepts. If again a 10 Mbyte/s link was used, it is obvious that at 12 μs per event transfer time, a small fraction of the link bandwidth would be used. It is clear that there is no need to go to optical conversion, which would require the installation of a new set of optical fibers between the MCH and the muon chambers. We can easily transmit data on the cables already installed.

Fig. 22 shows general block diagram of the proposed muon system. There will be number of geographic sectors (GS) associated with particular parts of the muon detectors. The exact structure of such a division has to be optimized yet. In general, each geographic sector is a separate VME crate in MCH responsible for transferring data from detector system to the Level 3 farm. Each GS has a Fanout Card which is connected and controlled by the DØ Trigger Framework (TF). According to the current specification, the TF will provide timing and control information to the Fanout Card in order to maintain independent readout from each GS. Each GS can have several Muon Readout Cards (MRC) associated with smaller segments of the muon detectors like WAMUS chambers, Scintillator Counter front end crates, Level 1.0 trigger system *etc.* The connection between MRC and electronics on the detector platform is provided by existing twisted and flat cables and wide bandwidth coaxial cables. Each MRC has two independent section and uses two 50 conductors ribbon cables and eight coaxial cables. Our studies show that using tail cancelation technique one can transmit 20 ns pulses via the flat cable and up to 160 MHz via the coaxial cable for the distances over 75 meters.

5.6 Services and Slow Controls/Monitoring

The LV is supplied locally to the chambers and consists of $\pm$ 5V, and $\pm$12V. We plan to use +5V very heavily, with only minor loads required of the other LV supplies. We believe that almost sufficient current capability exists if the supplies used in Run I are reused. Until real preproduction prototypes are designed, this issue must remain open. We will try to use 3V logic with its 60% reduction in power consumption over equivalent 5V logic as much as possible. The TMC chips are already 3V. The FIFOs we plan to use have just now come out in 3V versions. We would expect that the majority of the logic components would available in 3V form by the time we need to buy components for the whole detector.

The cable plant established for Run I was quite extensive and is in fact much more than what we will need for Run II muon system. It appears that a single 50 wide ribbon cable from each chamber to the MCH should be sufficient to carry the slow digital signals, the Level 1

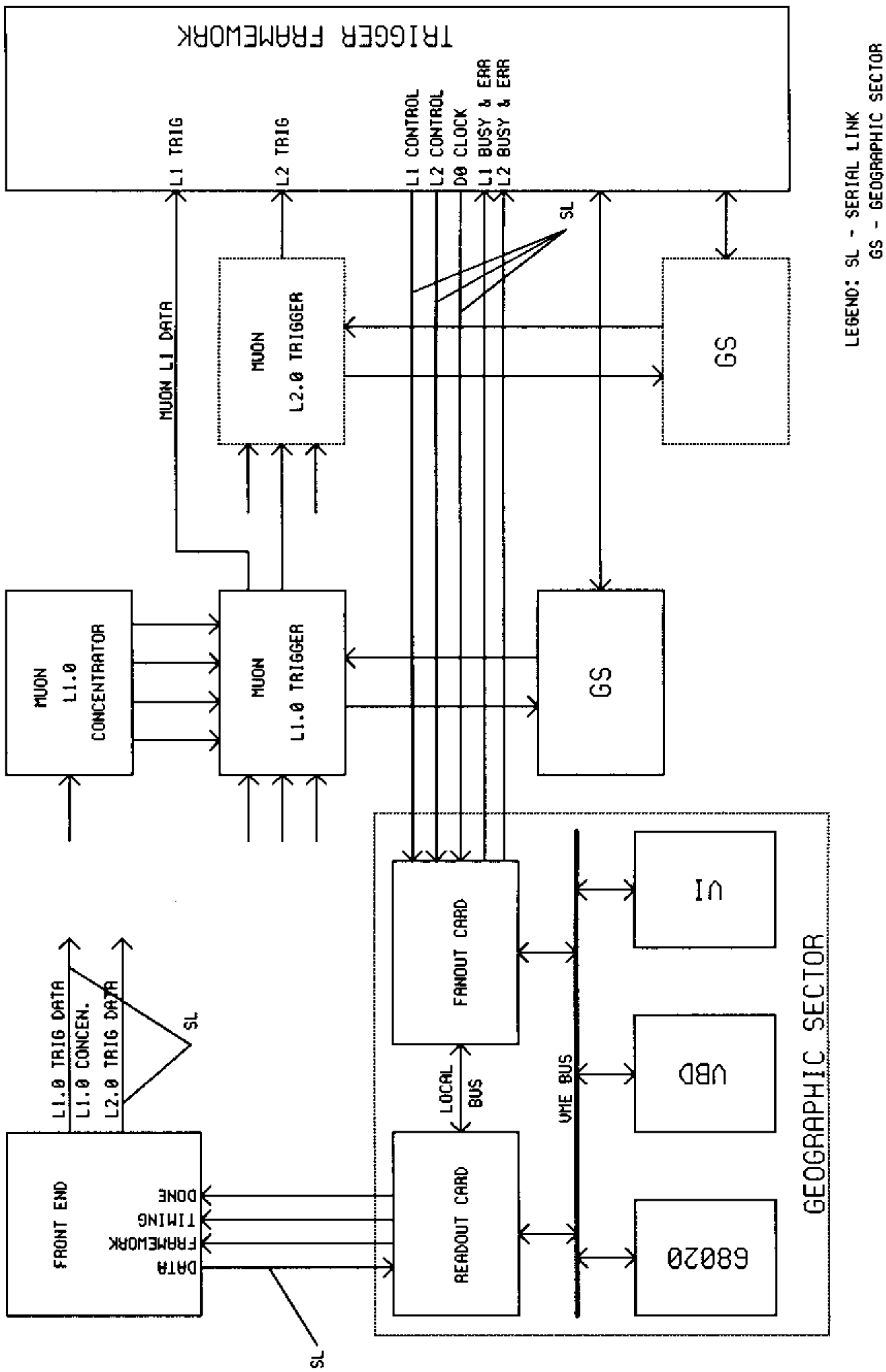

Figure 22: Block diagram of the muon trigger system.

and Level 2 trigger protocol signals and the test pulses. The 53 MHz clock, the accelerator bunch crossing sequence and Level 2 and Level 3 data will be transferred via wide band 75 ohm analog signal cables. These cables now have substandard terminations and will require completely new connectors. Because of the new detector systems that will be installed, the extra cables from the old muon system will be very useful. High speed transmission will be required for communication between the chambers and the Level 1 trigger system. The Level 1 cable plant is likely to be copper and the total number of new cables (one per chamber) will be small.

Packaging of the on-chamber electronics will be improved. At present for WAMUS, there is a Service Board (SB) bussing HV and carrying decoupling capacitors and current limiting resistors. This card is connected to the Mother Board (MB) containing the sample and hold time and pad measurement thick film hybrids. The sending of the analog data and hit bit map to the MCH is the province of the Control Board (CB). All slow controls are handled by a separate Monitor Board (MonBo). Finally, subsidiary detectors are treated as pseudo chamber cells in a Scintillator Counter Trigger Board (SCTB). The new front end boards does not have any hybrids and is therefore christened with the three letter acronym FEB.

The plan is to rebuild the WAMUS SB addressing the problem of higher currents by changing the current limiting resistors. We also suspect that the HV blocking capacitors were susceptible to radiation damage. We are studying more robust components since the existing caps are already dying in the forward regions in Run I.

The major element implicated in system failures in Run I has been the cable interconnects. We plan to package the on-chamber electronics so as to minimize the interconnects. The SB signal output will be connected to a small intermediate bus, thus making it possible to change a FEB without disconnecting SB cables. The FEB will connect to the signal input bus and to an output bus carrying data and muon triggers, LV, and control lines. That bus will serve as input to the new CB. The CB connection to the MCH will use the existing 50 wide data cable along with serial links to the Level 1 muon trigger, any Level 2 processors, and the VBD. The MonBo functions will be absorbed into the CB including the 1553B connection.

The MonBo functionality will be maintained, so that thresholds, pulser amplitude controls, and input test pulse masking will be available. As more intelligence migrates out onto the platform it is crucial to simplify the system. For that reason, an extensive set of remote tests is envisioned. The use of all digital systems should also greatly simplify operation. The design for Run II allows a full test of every aspect of the system operation.

6 The Level 1 Muon Trigger System

6.1 System Overview

The Level 1 muon trigger for the upgraded DØ detector uses all the detector elements described in the previous sections to provide inclusive muon and dimuon triggers with as low a p_T^μ threshold as possible. In addition, the Level 1 muon trigger is fully pipelined for deadtimeless operation. Elements of the Level 1 muon trigger are briefly described below. Technical details of the Level 1 muon trigger can be found in the specification document associated with each type of muon trigger card.

An overview of the muon trigger system is shown in Fig. 23. Presently there are three VME crates of muon trigger cards corresponding to the central, north, and south regions. Within each crate there are eight level 0.5 muon trigger cards (MTC05 cards) and eight corresponding Level 1.0 muon trigger cards (MTC10 cards). The number eight comes from the fact that each region (central, north, and south) is divided into octants. Thus by card level trigger we mean a trigger found in an octant of a given region. Note the names 05 and 10 do not really represent different levels of triggering but rather distinguish between trigger decisions made with fast (scintillator) detector elements and those made predominantly with wire information. The Level 1 muon trigger uses both types of information in a user defined manner in order to determine whether a good Level 1 muon trigger has occurred.

The flow of trigger information is from muon detector front ends and CFT tracker trigger to bit concentrators. Such concentrators are necessary in order to condense the bit patterns from the muon front ends onto a smaller number of cables as well as to fanout those patterns where necessary. Examples are the CFT tracker trigger data which must be sent to each of the central, north, and south crates and APHI and PIXEL data which must be sent to two octants in the region of octant boundaries. From the concentrators bit patters are sent to the MTC05 and MTC10 cards. These cards provide a muon trigger at the card level (an octant in a given region).

Inputs to the MTC05 cards in the CF region (central crate) include information from the CFT tracker, APHI counters and CS counters. Inputs to the MTC05 cards in the EF region (north and south crates) include data from the CFT tracker and A, B, and C layer PIXEL counters. Our present design does not extend beyond $|\eta| > 2.0$ however this could be easily accommodated by straightforward extension.

The MTC10 cards handle wire information and as such are reminiscent of the OTC trigger in Run I (however the architecture is completely dissimilar). At the same time though the MTC10 cards have access to many of the fast (scintillator) muon detection elements as well as information from the corresponding MTC05 card level trigger decision. Thus one may confirm hits (crudely) in the PDTs or Iarocci tubes with the fast detector elements. This is needed in any case to tie different views together. Thus in the CF region (central crate) inputs to the MTC10 cards are A, B, and C layer PDT centroids and APHI and CS counters. In the EF region centroids from A, B, and C layer Iarocci tubes serve as input along with A, B, and C PIXEL hits. Also input to the MTC10 cards is 64 bits of trigger information from the corresponding MTC05 cards. Each MTC05 and MTC10 card produces 12 bits of trigger information which is user defined.

The 12 bits of trigger information from each MTC05 and MTC10 cards in a given crate

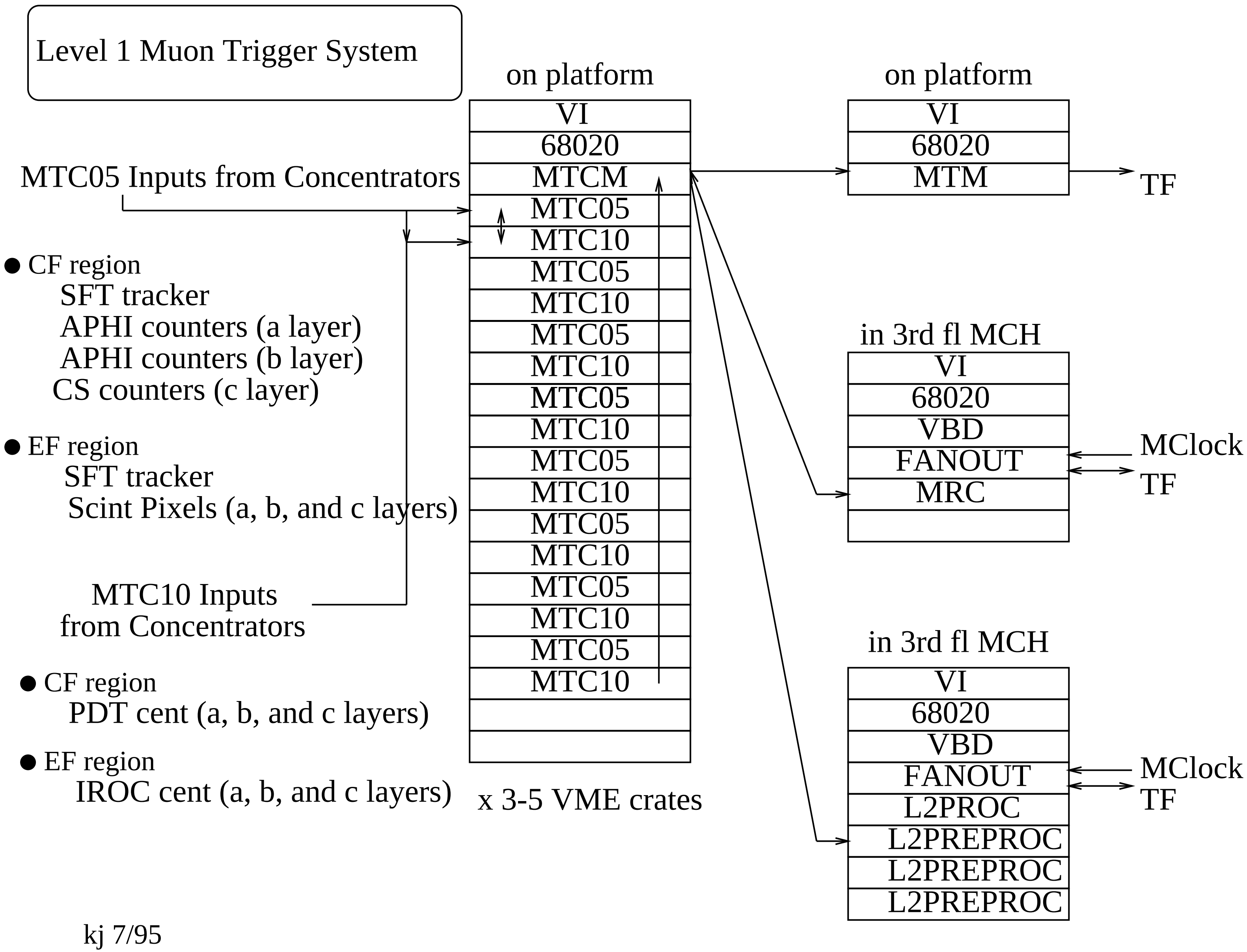

Figure 23: The Level 1 Muon Trigger System.

are read by the muon trigger crate manager (MTCM card) which produces 16 bits of user defined crate level trigger information. By crate level trigger we mean a trigger corresponding to a given region (central, north, or south). Finally, each MTCM card sends its 16 bits of trigger information to the muon trigger manager (MTM card) which produces 16 bits of user defined global Level 1 muon trigger information which is sent to the Level 1 trigger framework.

Upon receipt of a Level 1 trigger accept, card level trigger information which has been read from the MTC05 and MTC10 cards by the MTCM card and the MTCM crate level trigger decision are sent to any Level 2 preprocessor crates which desire them. One can imagine that unpacking or track segment finding might be driven by details of these local Level 1 muon trigger decisions. Upon receipt of a Level 2 trigger accept, all inputs to the MTC05 and MTC10 cards, card level and crate level trigger decisions, and status and error information from the MTC05, MTC10, and MTCM cards are sent via the MTCM to the MRC cards for possible use in the Level 3 muon trigger as well as to record the entire trigger decision process in the event data block should the event be selected to be written to tape.

6.2 Concentrator Cards (MCON Cards)

The purpose of the muon concentrator (MCON) cards is accept data from muon detector front ends and condense that data onto a smaller of cables which are sent to the MTC05 and MTC10 cards. Typically the muon front end electronics consists of cards which are 64 or 128 channels wide. In addition, the concentrators serve as fanouts in that they allow bits to be sent to several cards. This is necessary for the CFT tracker trigger data which must be sent to each of the Central, North, and South crates. It is also necessary for scintillator data which typically must be sent to each of three octants to allow triggering with full efficiency at octant boundaries. Finally, in the case of the PDT and Iarocci tube data, the concentrators also form centroids from individual tube hits. Data is received in and transmitted out via serial links capable of 16 bit transfers at 53 MHz.

6.3 Muon Level 0.5 Trigger Cards (MTC05 Cards)

The purpose of the MTC05 cards is to form a muon trigger (which we call the level 0.5 trigger) which is input into the Level 1 muon trigger decision. Inputs to the MTC05 cards are data from fast detector elements such as the CFT tracker or other scintillation counters (APHI, CS, or PIXEL counters) which we sometimes call level 0.5 detectors. Transmission of data from these detectors to the MTC05 cards is via the concentrator cards over copper using serial links capable of 16 bit transfers at 53 MHz. Trigger decisions are reached via combinatorial logic implemented on high density FPGA's such as Altera's FLEX series. The MTC05 cards send 64 bits of trigger information to its corresponding MTC10 card for use in creating the MTC10 card level trigger decision. The 12 bits of MTC05 card level trigger decision is used by the MTCM card in order to produce a crate level trigger decision. The MTC05 card level trigger decision is available for use both by the Level 2 and Level 3 trigger engines. Inputs to and status of the MTC05 card are buffered on the card and readout to Level 3 for use in monitoring the Level 1 muon trigger system. The trigger logic on board is

Input	Total Bits	Bits/Octant	Cables/Card	Bits/Cable
CFT tracker	7680	960	10	96
APHI (a layer)	210	30	1	96
APHI (b layer)	80	40	1	96
CS	240	40	1	96

Table 5: CF MTC05 Card Inputs

Input	Total Bits	Bits/Octant	Cables/Card	Bits/Cable
CFT tracker	7680	960	10	96
APIXEL	1800	112	2	96
BPIXEL	1800	112	2	96
CPIXEL	1800	112	2	96

Table 6: EF MTC05 Card Inputs

fully field programmable and sufficient buffering exists for the 1 ms duration of the Level 2 trigger decision.

In the CF region, inputs to the MTC05 cards are from the CFT tracker, APHI counters, and CS counters. For each MTC05 card in the CF crate we have the inputs shown in Table 5. In the EF region, inputs to the MTC05 cards are from the CFT tracker and the PIXEL counters in the A, B, and C layers. For each MTC05 card in the EF region we have the inputs shown in Table 6.

6.4 Muon Level 1.0 Trigger Cards (MTC10 Cards)

The purpose of the MTC10 cards is to form a muon trigger (which we call the Level 1.0 trigger) which is input into the Level 1 muon trigger decision. Inputs to the MTC10 cards are primarily data from wire chambers, either PDTs or Iarocci tubes. Depending upon channel count, it may be possible to have as input some of the fast detector data (APHI, CS, or PIXEL counters) as well. Transmission of data from these detectors to the MTC10 cards is via the concentrator cards over copper using serial links capable of 16 bit transfers at 53 MHz. Trigger decisions are reached via combinatorial logic implemented on high density FPGA's. The MTC10 cards also receive 64 bits of trigger information from its corresponding MTC05 card for use in creating its card level trigger decision. The 12 bits of MTC10 card level trigger decision is used by the MTCM card in order to produce a crate level trigger decision. The MTC10 card level trigger decision is available for use both by the Level 2 and Level 3 trigger engines. Inputs to and status of the MTC10 card are buffered on the card and readout to Level 3 for use in monitoring the Level 1 muon trigger system. The trigger logic on board is fully field programmable and sufficient buffering exists for the 1 ms duration of the Level 2 trigger decision.

In the CF region, inputs to the MTC10 cards are from the CFT tracker, APHI counters, CS counters, and WAMUS PDTs. For each MTC10 card in the CF crate we have the inputs shown in Table 7. In the EF region, inputs to the MTC10 cards are from the PIXEL counters and Iarocci tubes in the A, B, and C layers. For each MTC10 card in the EF region we have

Input	Total Bits	Bits/Octant	Cables/Card	Bits/Cable
APDT	864	144	3	48
BPDT	1824	240	5	48
CPDT	1824	240	5	48
APHI (a layer)	210	30	1	96
APHI (b layer)	80	40	1	96
CS	240	40	1	96

Table 7: CF MTC10 Card Inputs

Input	Total Bits	Bits/Octant	Cables/Card	Bits/Cable
AIarocci	14400	300	4	75
BIarocci	18240	380	4	96
CIarocci	19200	400	4	50
APIXEL	1800	112	2	96
BPIXEL	1800	112	2	96
CPIXEL	1800	112	2	96

Table 8: EF MTC10 Card Inputs

the inputs shown in Table 8.

6.5 Muon Crate Manager Cards (MTCM Cards)

The purpose of the MTCM cards is to form a crate level muon trigger which corresponds to a trigger in the central, north or south regions. The MTCM crate level trigger decision is formed by simple processing (essentially combinatorial logic) of the MTC05 and MTC10 card level trigger decisions which are read by the MTCM card. The MTCM card buffers the MTC05 and MTC10 card level trigger decisions and makes them available to Level 2 preprocessors upon Level 1 accepts. The MTCM card reads out MTC05 and MTC10 card inputs, status, and errors upon Level 2 accepts and makes this information (along with the MTC05 and MTC10 card level and its own crate level trigger decision) available to the Level 3 trigger engine. Transmission of data to both Level 2 preprocessors and MRC cards (for readout by VBD's into Level 3) is over copper using serial links. The bandwidth required to transmit to Level 2 preprocessors is approximately 16 bits $\cdot$ 17 cards $\cdot$ 10kHz = 2.7 Mbits/s (neglecting 8b/10b overhead). The bandwidth required to transmit to the MRC cards is approximately 7 clock cycles $\cdot$ 16 bits $\cdot$ 16 inputs $\cdot$ 16 cards $\cdot$ 1kHz = 28.6 Mbits / s (neglecting 8b/10b overhead). In fact, the effective transfer rate to the Level 2 preprocessors is 110 Mbits / s thus data is transferred to the Level 2 preprocessors in 2.3 μs. The effective transfer rate to the MRC card (upon Level 2 accepts) is 121 Mbits / s thus data is transferred to the MRC card in 243 μs.

The MTCM also receives clock signals (53 MHz clock, RESET, GAP) from the MRC card, creates / n clocks as needed (such as the bunch crossing clock), and fans out these signals to the MTC05 and MTC10 cards. The MTCM also receives the 7 bytes of serial link words from the trigger framework. Presently we envision these 7 bytes of information will be sent by the muon trigger fanout (MTF) card over serial link to the MTCM card. The trigger framework bytes translated by a daughter card common to DØ. In this way then the MTCM card receives Level 1 accepts and rejects, Level 2 accepts and rejects, crossing and trig numbers associated with these commands, and other commands sent by the trigger framework. The MTCM fans out these commands and numbers to the MTC05 and MTC10 cards as needed. The MTCM compares its internal crossing and trig numbers against those sent by the trigger framework and generates errors in the case of disagreements. The MTCM also fans in busy and error signals from each of the MTC05 and MTC10 cards and sends them to the trigger framework via the MRC cards.

6.6 Muon Readout Cards (MRC Cards)

The purpose of the MRC cards is to receive data from both the muon front end electronics and muon trigger cards which are located under the DØ platform. The MRC cards reside on the 3rd floor MCH and receive data using serial links via copper cable. Data received by the MRC cards is sent to the Level 3 trigger engine via readout of collected data by the VBD's in each crate.

6.7 Muon Fanout Cards (MFC Cards)

The purpose of the muon fanout cards (MFC cards) is to receive the 7 bytes of control data from the Level 1 trigger framework (via serial link over copper or optical cable) and transmit this data to each of the MTCM cards (via 50c wide twist n flat). This data contains commands from the trigger frameworks (Level 1 accept, Level 1 reject, Level 2 accept, Level 2 reject, initialize, etc.) as well as crossing numbers and trigger numbers associated with Level 1 and Level 2 accepts. The MFC card also receives busy and error information from the MTCM cards and sends these signals to the trigger framework. The MFC card also receives accelerator clock information (possibly transmitted on the same serial link) and transmits the 53 MHz clock, Reset, and Gap signals to the MTCM cards via Astro cable.

6.8 Muon Trigger Manager Cards (MTM Card)

The purpose of the MTM card is to provide trigger decision data to the Level 1 trigger framework. The MTM serves as a fan in to the trigger framework by collecting and processing muon crate level trigger decisions which are sent over serial link using copper cable. This global muon trigger decision data is subsequently sent to the Level 1 trigger framework for inclusion in the global physics trigger decision. The trigger decision bits are sent over twist-and-flat cables via differential ECL to the Level 1 trigger framework.

6.9 System Timing

The MTC05 timing is given in Table 9. The MTC10 timing is given in Table 10.

Delay	Δ Time (ns)	Total Time (ns)
BC to SFT4	2	2
RO and SFT	132	134
Serialize at SFT	132	266
Xmit and Rec	132	398
De-serialize at MTC05	57	455
Synch	264	719
MTC05 trigger logic	396	1115
Xmit to MTC10	20	1135

Table 9: MTC05 System Timing

Delay	Δ Time (ns)	Total Time (ns)
BC to c layer	40	40
Drift	800	840
Centroid Processing	132	972
Serialize	132	1104
Xmit and Rec	132	1236
De-serialize at MTC10	57	1293
Synch	264	1557
MTC10 trigger logic	528	2085
Xmit to MTCM	20	2105
Synch all MTC10	132	2237
MTCM trigger logic	132	2369
Xmit to MTM	38	2407
Synch all MTCM	132	2539
MTM trigger logic	132	2671
Xmit to TF	200	2871

Table 10: MTC10 System Timing

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