Characterization of the Silicon Dioxide Film Growth by Plasma Enhanced Chemical Vapor Deposition (PECVD)

Thomas Woodson
Advisors: Dr. Helena Gleskova and Dr. Sigurd Wagner
Funded by the Princeton Plasma Physics Laboratory Summer Program 2004

Abstract:

The purpose of this study was to examine how certain parameters like temperature, pressure, and gas composition affect the film growth of SiO_2 when using Plasma Enhanced Chemical Vapor Deposition (PECVD). Overall the goal was to develop a recipe guide that will assist researchers by showing how these parameters change the deposition rate, etch rate, index of refraction and the pinhole density of the SiO_2 film. All the recipes used can be found on the Plasmatherm 790 under C:\sysmom\process \programs\twoodson

Introduction:

A thin layer of insulating film (SiO_2 in our case) is crucial to the performance of integrated circuits (IC). The dielectric film acts as a barrier in order to isolate conductive regions. Without the SiO_2, there would not be an insulating area.

Since this film is so important, many methods have been developed to deposit it. Some of the more popular techniques are thermal oxidation, Chemical Vapor Deposition (CVD), Low Pressure Chemical Vapor Deposition (LPCVD) and Photo-induced Chemical Vapor Deposition (PHCVD). The method in this experiment, PECVD, uses excited gases, a plasma, from which SiO_2 grows on the surface of the substrate placed in the chamber. This technique is often faster than other methods.

Procedure:

Growing the film

In order to characterize the deposition we had to grow the film. The first recipe that was run was a deposition preparation step (DepPrep). The DepPrep's main function is to clean out the residual oxides that are in the chamber from previous depositions. It uses a combination of $CF_4 + O_2$ and argon. The $CF_4 + O_2$ etches the oxides and organic materials in the chamber. The argon is used as a "mechanical method" to clean the chamber because it bombards the surfaces with its heavy atoms, stripping all of the possible contaminants. When this recipe is run, neither the samples nor the platform wafer are in the chamber.


Plasmatherm 790

After the DepPrep, a pre-deposition step is run with a platform wafer in the chamber. The platform wafer acts as a stage so that the sample will not be directly on the surface of the PECVD (When the sample is directly touching the PEVCD the growth of the film is affected). The PreDep coats the chamber with the particular layer of the SiO_2 that the trial will be using. This acts as a layer of protection so that the sample will not be contaminated. Finally we put the actual

sample, which consists of a silicon wafer, a glass slide with a chromium film deposited on the surface and a clear glass slide, into the chamber and run the recipe.

Adding Photoresist and etching

Once the recipe is complete, the chromium glass slide is cut into several pieces and photoresist strips are added. This experiment used AZ 5214 as the photoresist. Once the photoresist has been baked on, the chromium glass slides are etched in Buffered Oxide Etch (BOE) 10:1, varying the etch time for each piece of the chromium slide. The slides are then transferred to Photo Resist Stripper 1000 to remove the photoresist.

KLA- Tencor

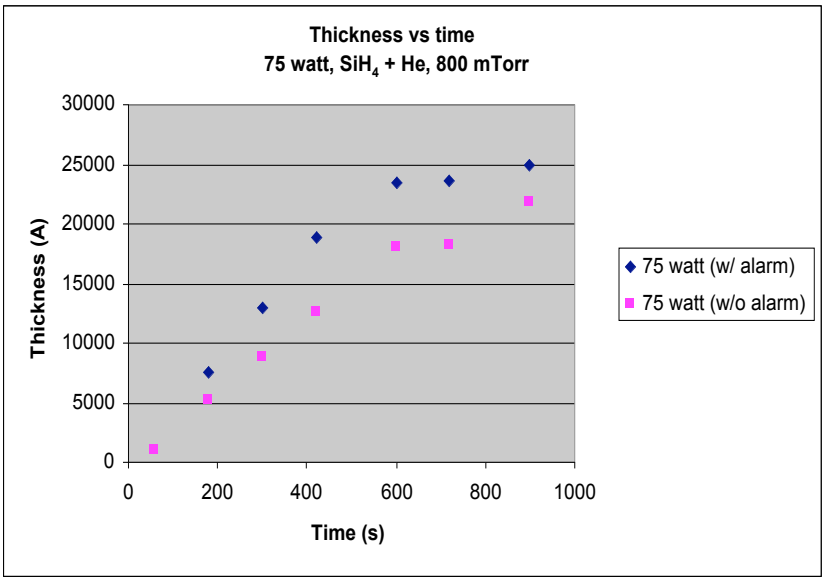
Measuring

Once the physical manipulation of the samples is finished, they are analyzed using the KLA-15 Tencor surface profiler and an ellipsometer. The Tencor takes a profile measurement of the chromium slide to determine the amount of oxide etched away and the ellipsometer measures the index of refraction and the total thickness of the oxide on the silicon wafer. The clear glass slide is simply used to insure that the oxide is transparent.

The pinhole density is measured by counting the number of pinholes in a mm^2 area. On samples where there were thousands of pinholes, the number of holes was extrapolated from a smaller area.

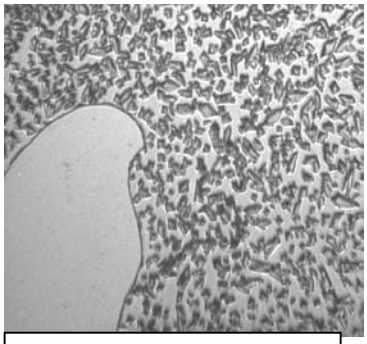
Problems:

Throughout the process there were several problems that occurred. One error while doing the actual deposition was that the gas pressure often dropped sharply causing an alarm to sound and the oxide to stop growing. This had noticeable effects on the film quality as seen on the characterization of the 75 watt, SiH4 + He recipe (graph to the left). Also, on a few occasions the DepPrep had to be run twice in order to certify that no oxides were remaining in the chamber.

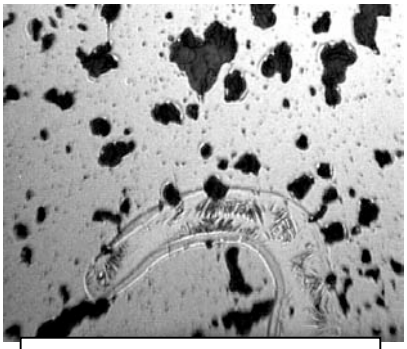


During etching a major concern was that all the oxide would be etch away completely. Due to the chromium backing, it was often hard to tell if the oxide was gone because at certain points during the etching the interference color of the oxide layer would match the silver color of the chromium. Another major setback during this stage of the experiment was that the photoresist would be attacked by the HF in the BOE. This would result in a premature removal of the photoresist and subsequently the oxide thickness could not be measured. The only remedy for this problem would be to bake the resist longer. Though

this often worked, there's still a chance that the photo resist would come off, especially when long etch times are used, i.e. over 10 minutes.



Sample 133: 3200+ holes, SiH4 + He at 600mTorr, 25 watts



Sample 119: Chromium glass is etching away. 125 watt, 800mTorr SiH4+N2

Similarly to the photoresist problem, the chromium also came off the slide (see sample 119). Again the HF attacked the chromium causing it to deteriorate, but unlike the photoresist, there is no way to prevent the chromium from etching away once it is deposited on the slide. Consequently, the slides with a thicker layer of chromium are better since there is a smaller chance that the HF will eat through it.

Finally during the measurement stage two main problems arose. First the ellipsometer often gave values for the total thickness that were inaccurate which then nullifies the values for the index of refraction. Since the thickness is calculated from the index of refraction, if the thickness that the ellipsometer reads is different than the KLA - Tencor and NanoSpec readings, then the index of refraction is incorrect. To keep the ellipsometer readings from skewing the data, the outliers were disregarded.

The second problem that arose while measuring the samples were the pinholes that appeared (see sample 133 above). Pinholes occur because of uneven deposition and etching which lead to "pillars" of oxide. If a pinhole is in the right place it can short out a transistor on a chip. A more detailed explanation of the pinhole trend is below.

Trends/Results:

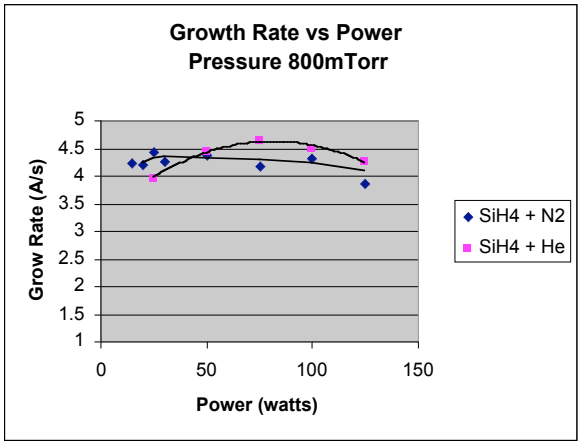
-All the data can be found on the spread sheets at the end of the report.
-Each trial flowed 35sccm of either SiH_4 + He or SiH_4 + N_2 and 160sccm of N_2O. The pressure was varied between 200mTorr and 800mTorr. The power was varied between 15 watts and 125 watts. The temperature for all the trials was 250 C.

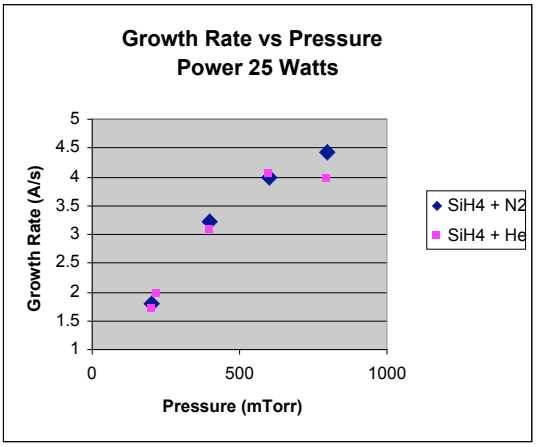
Color

All of the films that were deposited were clear.

Growth Rate

Growth Rate = total thickness/ (5400 sec)

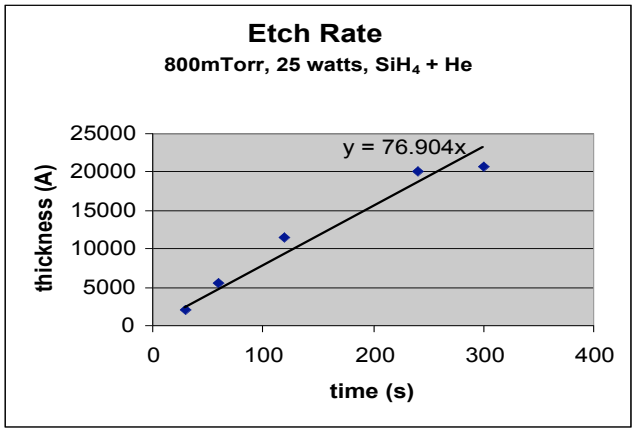




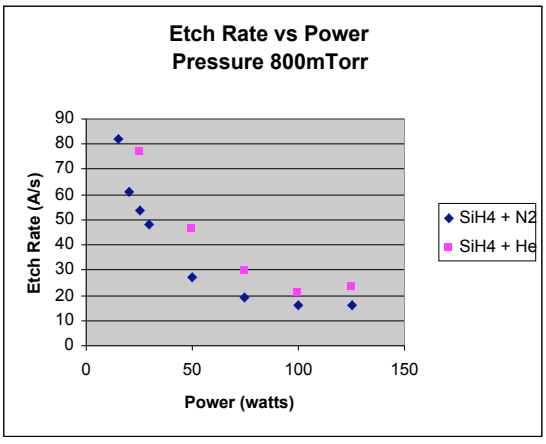
-The growth rate peaks at 75 watts for SiH_4 + He and around 25 watts for SiH_4 + N_2
-As the pressure increases the growth rate increases.

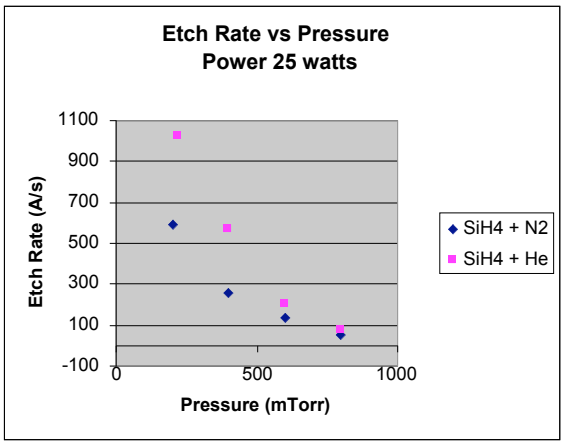
Etch Rate

-An individual etch rate is calculated by taking the slope of the linear regression line of the thickness versus time graph (as seen below).



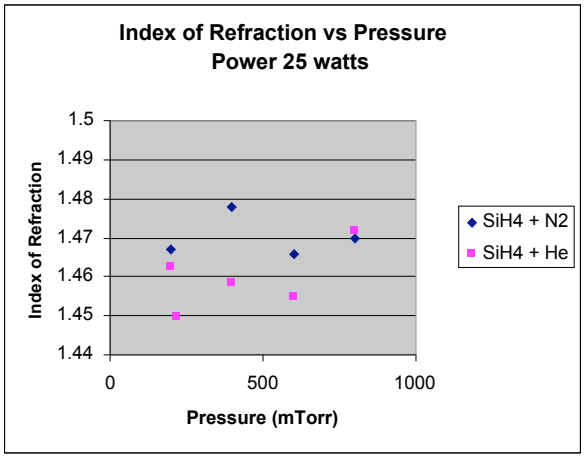
- The plots below are showing the etch rate vs the pressure or power. NOTICE the different scales.

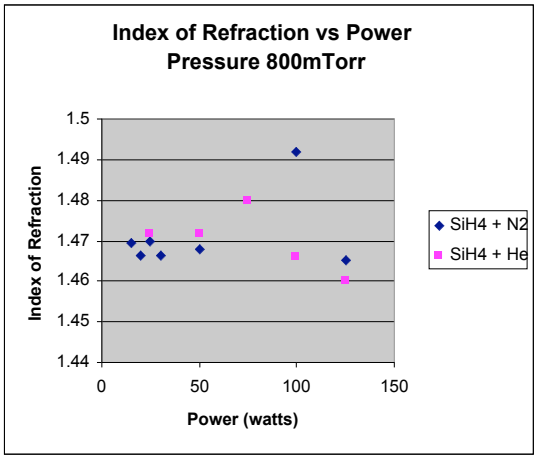




Index of Refraction

-There is no clear pattern how the index of refraction is affected by the power or pressure. The index of refraction does stay around 1.5 which is an acceptable value. SiO_2 films made by thermal oxidation have a value of 1.46.

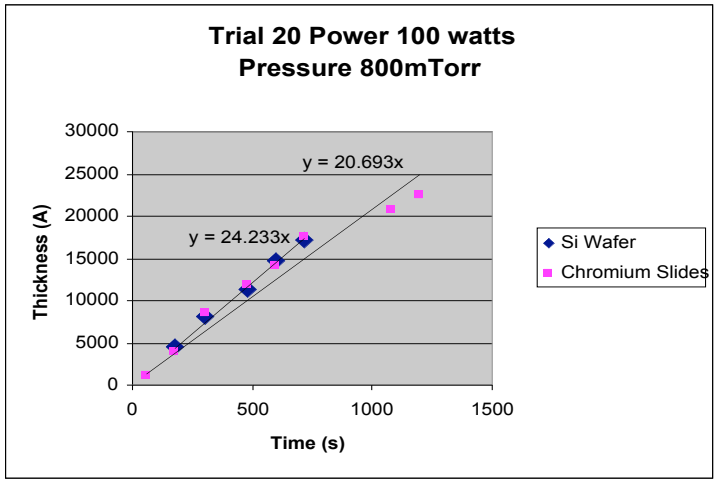




Substrates

-Two different substrates, Si wafers and Cr films on glass, were used in order to determine if the type of substrate affects the growth rate and the deposition rate. No significant trend was found between the substrate and the etch rate or deposition rate (see graph below).

-SiO_2 films deposited on silicon wafers have fewer pinholes. On average the silicon wafer has less than 15 pinholes per mm^2



Pinholes

-The pinholes are only a problem when using SiH_4 + He at low pressures. At 600mTorr and 400mTorr the pinholes are so numerous that extreme care had to be used when measuring the thickness. The 200mTorr sample etches so fast that the pinholes are etched away before they can be observed. Though the pinholes can not be perceived on the 200 mTorr film, the films at this pressure are very low quality. On the other hand, the SiH_4 + N_2 films at low pressures have a moderate to low pinhole problem. The pinholes on these samples are comparable to the SiH_4 + He films grown at 800mTorr.

Trend Overview

A. As *Pressure* ↑ *etch rate* ↓ ; *film quality* ↑

B. As *Pressure* ↑ the *growth rate* ↑

C. As *Power* ↑ *etch rate* ↓ ; *film quality* ↑

D. As *Power* ↑ the *growth rate* **stays constant**

E. As *Pressure* ↑ the *index of refraction* **stays constant**

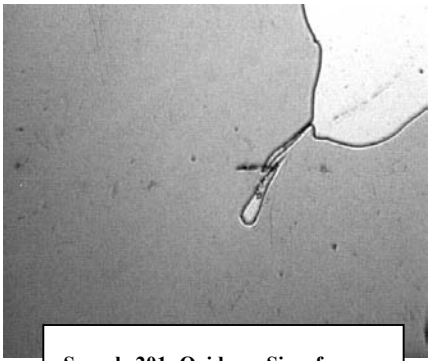
F. As *Power* ↑ the *index of refraction* **stays constant**

Conclusion:

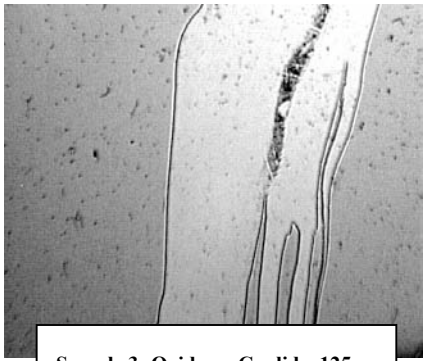
The best possible recipe would use a high pressure and a high voltage; at least 800mTorr and 100 watts respectively. At these values the growth rate is at its highest, and the quality of the film is maximized. Past these values, the change in etch rate and deposition rate is miniscule or it begins to have a negative affect.

The differences in the two gases are negligible when using high pressures. Both produce similar growth rates and etch rates and both produce the same amount of pinholes (about 60 holes per mm^2). But at low pressures, $SiH_4 + N_2$ is better because it produces fewer pinholes; it is possible to use $SiH_4 + N_2$ at pressures as low as 200mTorr to make good films, while SiH_4 + He only produces quality films at 800mTorr or higher.

The type of substrate used is also inconsequential when it comes to growth rate and etch rate. But the oxide grown on a silicon wafer has fewer pinholes (as seen below). The direct cause of this occurrence is not clear.



Sample 201: Oxide on Si wafer. 100 watts, 800mTorr SiH_4 + He



Sample 3: Oxide on Cr slide. 125 watts, 800mTorr SiH_4+N2

From the data collected, the index of refraction remained a little below 1.5 despite the changes made. It can be concluded that the variables tested have no affect on the index of refraction.

Acknowledgements:
Special thanks to

Dr. Helena Gleskova, Dr. Sigurd Wagner, Dr. Sam Cohen, Joseph E. Palmer, Princeton Plasma Physics Laboratory