3-D Simulation of SEU Hardening of SiGe HBTs Using Shared Dummy Collector

Muthubalan Varadharajaperumal, Guofu Niu, Xiaoyun Wei, Tong Zhang, John D. Cressler, Robert A. Reed, and Paul W. Marshall

***Abstract*—This paper presents a SEU hardening approach that uses a dummy collector to reduce charge collection in the main transistor. The dummy collector is obtained using the silicon space between adjacent HBTs. It is obtained without any process modification or area penalty. The simulations are performed for normal and angled strikes. The hardened device shows significant reduction in charge collection due to sharing of diffusive charge collection by the dummy collector. Multiple HBT arrays of regular and hardened HBT are simulated to study the simultaneous charge collection in multiple HBTs. With hardening, charge collection in multiple devices is suppressed considerably for normal and angled strikes as the shared dummy collector collects a large amount of charge.**

***Index Terms*—Critical charge, deep trench isolation (DTI), dummy collector, radiation hardening by design (RHBD), SiGe HBT, single event upset (SEU), SRH recombination.**

I. Introduction

SiGe HBT technology is a potential candidate for space applications because of its inherent robustness to total ionizing dose (TID) radiation [1]. Single Event Upset (SEU), however, is a concern, primarily due to charge collection through the collector-substrate (CS) junction [2], [3] and the relatively low substrate doping compared to digital CMOS processes. Various hardening techniques, like introduction of a back junction [4] or a heavily doped p-type buried layer [5] have been proposed to reduce charge collection. These techniques, however, require process changes. In this work, we propose a new SEU hardening approach that reduces charge collection through the use of a dummy collector/substrate (CS) junction and present 3-D simulation results. Like the RHBD techniques proposed earlier in [6], the hardening approach requires only layout changes. However, the new approach does not suffer area penalty when applied to integrated circuits, as the dummy CS junction can be obtained utilizing the silicon between adjacent devices. We will first examine charge collection in stand-alone HBTs, for both normal and angled deep strikes, and then examine simultaneous charge collection in multiple HBTs as found in circuits.

Manuscript received July 24, 2007; revised October 6, 2007. This work was supported by the Defense Threat Reduction Agency (DTRA) under the Radiation Hardened Microelectronics Program, NASA Goddard Space Flight Center (GSFC) under the NASA Electronic Parts and Packaging (NEPP) Program, the NASA Exploration Technology Development Program (ETDP), and the Alabama Microelectronics Science and Technology Center.

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Digital Object Identifier 10.1109/TNS.2007.910290

II. Device Structure and Layout

Fig. 1(a) shows the cross section of a typical regular SiGe HBT showing the deep-trench isolation and the CS junction. Fig. 1(b) shows a schematic of the layout. The deep-trench (DT) encircles the active device, and the NS layer defines the N^+ sub-collector. The silicon area inside DT thus determines the CS junction area. During an ion strike, the CS junction either directly collects deposited charges through drift within the potential funnel or indirectly collects charges after they arrive at the junction after diffusion.

Given that carrier diffusion lengths are on the orders of tens of microns or more in the lightly doped substrate of a typical SiGe HBT, a dummy CS junction placed outside the DT along the device perimeter should be able to at least reduce the amount of diffusive charge collection by the HBT collector, for charge deposited both inside and outside the DT isolation. A cross section and schematic layout are shown in Fig. 2(a) and (b). This dummy junction can be obtained by pulling out the NS layer in the regular HBT so that the NS encloses the outer DT edge by an amount W_d. As we will show below, a 1 μm wide dummy NS junction provides sufficient hardening. The dummy NS outside the DT is contacted through the same N+ sinker used for contacting the transistor NS. Fabrication of the hardened HBT is thus done with only a few layout changes. For a stand-alone device, one may be concerned about the extra silicon area. In integrated circuits, however, the proposed hardening approach does not really suffer area penalty. Devices are placed apart by several microns due to design rules, density requirement and other practical reasons. The unused silicon between neighboring devices can be utilized to create the dummy collector needed for SEU hardening.

Hardened devices have been fabricated in IBM 5AM technology and tested. Measured device characteristics are the same for regular and hardened HBT, showing no degradation in electrical characteristics, as the dummy CS junction is isolated from the main transistor. The measured breakdown voltage of the dummy CS junction is 21 V, which is more than sufficient for the technology.

Next we present 3-D simulation of the proposed SEU hardening approach, first using stand-alone single device, and then using arrays of HBTs to mimic the more realistic situations in an integrated circuit with HBTs placed together. Both normal strikes and angle strikes are simulated, with representative striking locations.

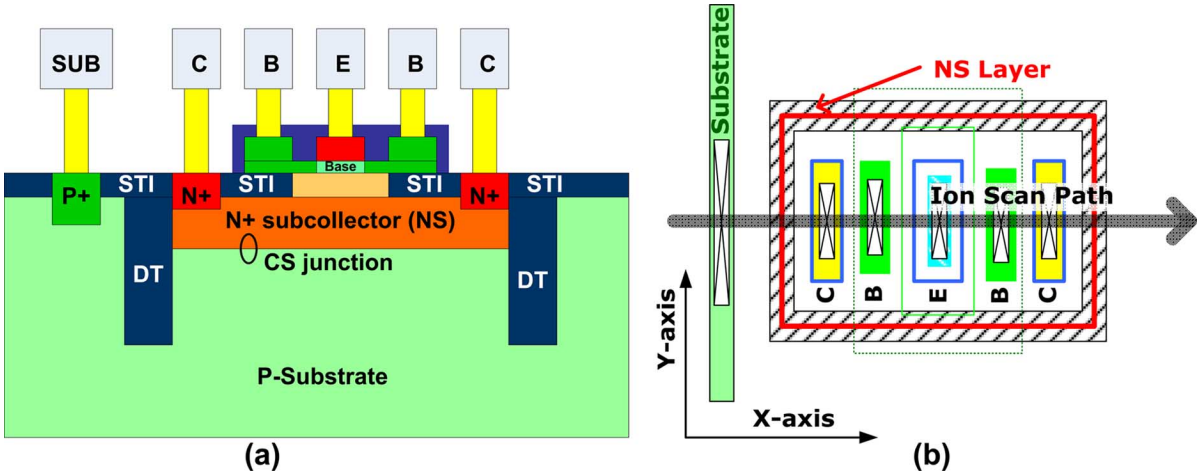

Fig. 1. (a) Schematic cross-section and (b) schematic of the layout of a SiGe HBT (not to scale). The ion travels in the XZ plane with a fixed y along the negative x direction. The simulated ion strikes will be located along the axis "ion scan path.".

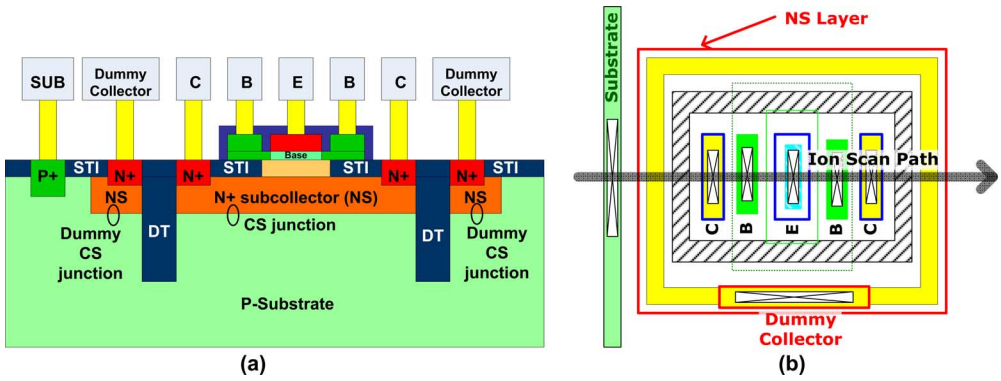

Fig. 2. (a) Schematic cross-section and (b) schematic of the layout of a hardened SiGe HBT (not to scale).

III. Stand-Alone Single Device

We first consider stand-alone single device, like those used in typical device characterization and microbeam testing. Devices are separated by 100 μm or more, and transistor active area is very small compared to the area needed for pads and interconnects leading to device terminals. Here we simulate a total silicon area of 35×35 μm^2, to mimic a stand-alone device.

The transistor is centered in the total silicon area. The 3D structure is 35 μm deep. The simulations were performed for various depths of the substrate for the same conditions. The charge collection was compared for the various depths and the minimum depth from which the charge collection remains constant was chosen as the depth of the substrate. This was done to ensure that the simulation results are not artificially dependent on the thickness of the substrate used in simulation, which is always much smaller than the actual substrate thickness to keep the number of grid points low.

Due to thick overlayers in modern silicon technologies, current heavy ions available for microbeam testing [5], [7], [8] cannot provide deep strike, particularly for angled incidence, therefore at present 3-D simulation is the only viable way of examining charge collection for deep strikes and large angled strikes. Here we use Sentaurus Device for 3-D simulation [9]. Charge track generation and physical models used are the same as in [3]. Deep strikes with an LET of 0.1 pC/μm (9.7 MeV-cm^2/mg) are simulated. The ion crosses the whole device. As the device size in the simulation is large, the amount of charge deposited in the simulated structure varies as the angle varies. However the amount of charge itself is not a meaningful parameter, as charge collection is not limited by the amount of charge deposited for these deep strikes.

We note that default SRH recombination model parameters are used, as opposed to those used in [5] for fitting microbeam data. The default parameters give longer lifetime, 9 μs for a substrate doping of 1×10^{15} cm^{-3}, and represent the worst case. Collector, emitter and base are grounded. $V_{substrate} = -4$ V. No difference is found for variation of V_{dummy} from 0 to 4 V. $V_{dummy} = 3$ V is used below.

As 3-D simulation is time consuming, we simulate only strikes along the x-axis, for a fixed y that is at the center of the device, as shown in Fig. 1(b). At each incident position, simulations are done for incident angles of $\theta = 0°$, 30°, 45° and 60°. The ion travels in the XZ plane with a fixed y along the negative x direction.

A. Regular HBTs

Fig. 3 shows collector charge versus ion incident position for various incident angles in the regular HBT. The worst charge collection occurs for normal strike, as expected. As the incident angle increases the area of large charge collection is reduced and

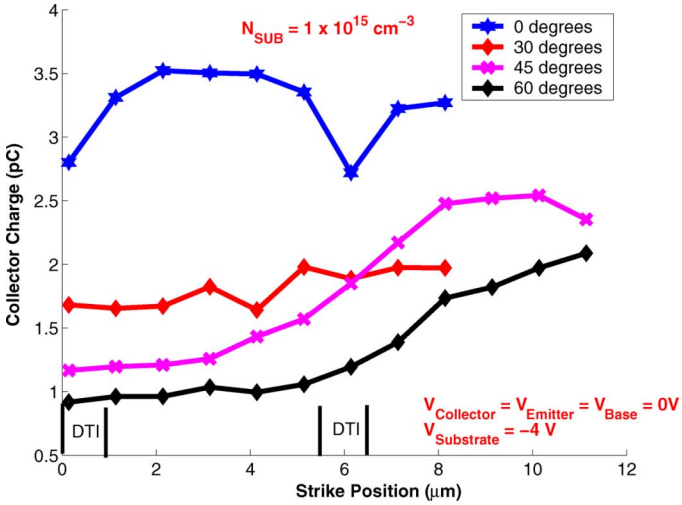

Fig. 3. Collector charge versus strike location for incident angles $\theta = 0°, 30°$, $45°$ and $60°$ in a regular HBT.

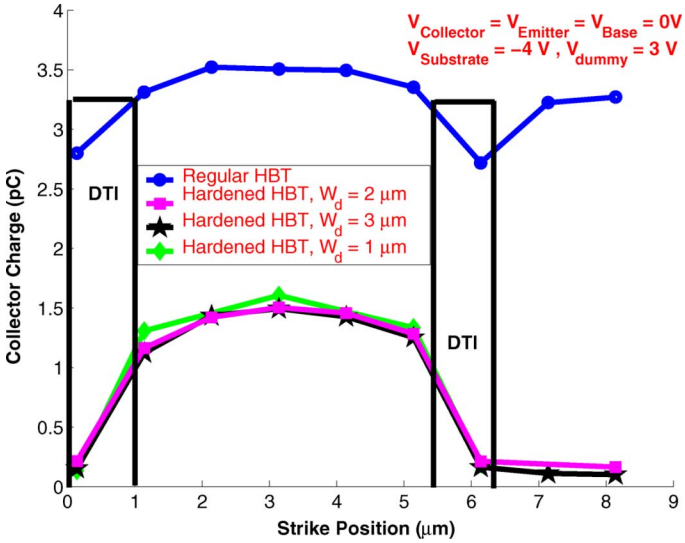

Fig. 4. Normal strike collector charge comparison between the regular HBT, and hardened HBT with $W_d = 1,\ 2$ and $3\ \mu$m.

area of lower charge collection increases [8]. The collector collects a large amount of charge for even strikes occurring outside DT because of the long lifetimes and large diffusion lengths.

B. Hardened HBTs

1) Normal Strike: Fig. 4 shows the normal strike charge collection comparison between the regular and hardened HBTs. Simulations were performed for different dummy collector widths (W_d) [see Fig. 2(a)]. Charge collection is approximately the same for $W_d = 1 - 3\ \mu$m, indicating that the typical 5 μm spacing between adjacent HBTs found in circuit design is more than sufficient for placing the dummy collector. This is good news, as no area penalty is involved. A width of 2 μm is used below. We note that the actual dummy CS junction area is larger than what W_d indicates, because of the existence of lateral junction between the N+ sub-collector and the surrounding p-substrate.

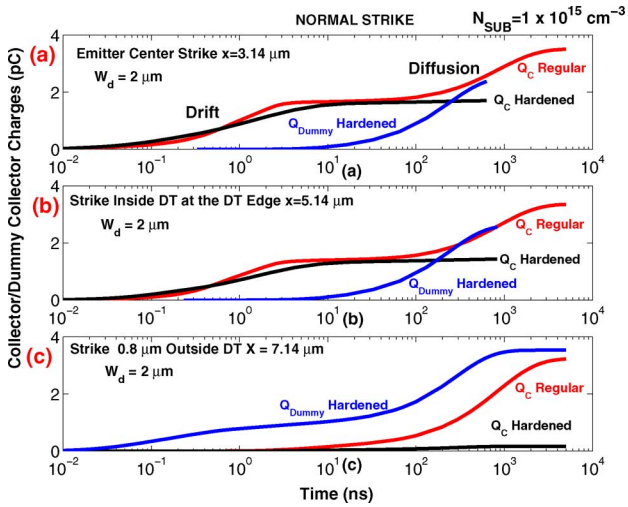

Fig. 5. Charge collection characteristics comparison for ion strike at (a) emitter center, (b) DT edge and (c) outside DT between the regular and hardened HBT.

We emphasize that the dummy collector should be placed around the DT isolation of the device to achieve the most effective hardening. The N^+ is highly conductive and in general the metal contact to the dummy collector can be placed anywhere on top of the N^+ dummy collector.

The hardened device reduces collector charge collection significantly, not only for strikes outside DT, but also for strikes inside DT. To further understand these results, we plot charge collection vs time at representative locations in Fig. 5.

For emitter center strike, the charge collection curve for the regular HBT shows two distinct regions: drift and diffusion [Fig. 5(a)]. The charge collected by each terminal is obtained by the integration of current in the terminal. The final collector charge at 1000 ns is 3.5 pC and 1.71 pC for the regular and hardened HBTs. The diffusive charge collections by the dummy collector and the collector of the regular HBT have not completely saturated, and a slightly higher charge is expected if simulations were done for a longer time. This, however, does not affect our conclusion, as charge collection by the hardened HBT collector has completely saturated. A longer simulation would lead to slightly higher charge collection by the regular HBT collector, but the same charge collection by the hardened HBT collector. The final dummy collector charge is 2.1 pC. The total charge collected with hardening ($Q_{dummy} + Q_C$ hardened) is higher than the Q_C in the regular HBT. The drift portion of the curves are approximately the same in the regular and hardened HBTs. The charges left in the substrate after drift collection start to diffuse outward towards the extrinsic portion of the device. In the hardened HBT, the diffusive charge collection is dominated by the dummy CS junction, as evidenced by the saturation of Q_C hardened and the increase of Q_{dummy} in Fig. 5(a). This leads to less charge collection by the CS junction of the active device. Fig. 5(b) shows charge collection vs time curves for a strike at the NS edge, which are similar to those for the center strike. Again, the dummy CS junction dominates diffusion charge collection.

For strikes outside DT, charge collection in the regular HBT is only through diffusion of charges generated outside DT towards

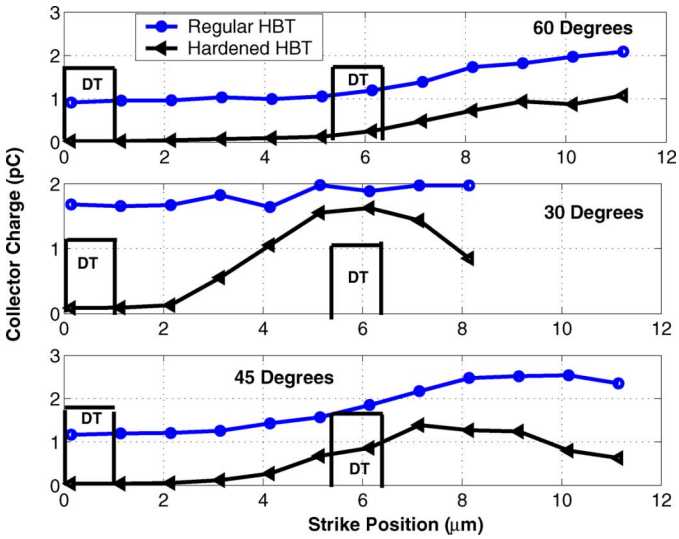

Fig. 6. Positional charge collection comparison between the regular and hardened HBT for angled strikes $\theta = 30°$, 45° and 60°.

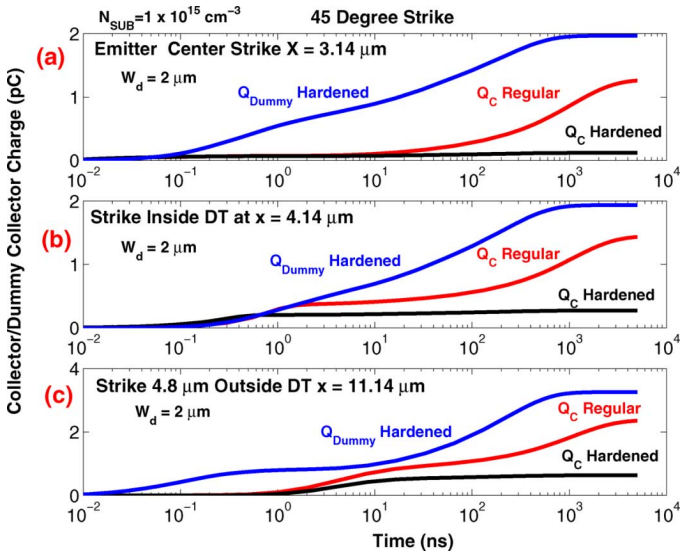

Fig. 7. Charge collection characteristics comparison for ion strike at (a) emitter center, (b) DT edge and (c) outside DT between the regular and hardened HBTs for $\theta = 45°$.

the CS junction inside the DT. Fig. 5(c) shows such a strike that is on the dummy collector. As expected, the dummy collector charge collection has a large drift component. The dummy collector collects 3.5 pC charge, and reduces collector charge from 3.2 pC in the regular HBT down to 0.17 pC in the hardened HBT. For strikes occurring W_d μm away from the outer DT edge, the lateral junction of the dummy CS junction will come into play.

To summarize, for all normal strikes, with hardening, the drift component of charge collection remains approximately the same, while the diffusion charge collection component is nearly completely suppressed.

2) Angled Strike: As large angles are of practical concern [10], [11] , we now examine the mechanisms of angled incidence charge collection.

Fig. 6 shows the angle strike comparison for $\theta = 30°$, 45° and 60°. The hardened HBT collects less charge than the regular HBT for all angles and all strike positions. The area of higher charge collection is reduced by a considerable amount in the hardened HBT. The improvement from hardening is overall more significant compared to normal incidence, and can be understood as follows. For normal incidence, the ion passes through either the transistor CS junction or the dummy CS junction. For large angle incidence, the ion either passes through one junction, or misses both CS junctions. Consequently, charge collection by the transistor CS junction is mainly through diffusion in most cases, and the dummy CS junction becomes more effective. This explanation is supported by simulated details of electron density n, hole density p, and potential ψ.

The charge collection vs time plots at representative strike points are shown in Fig. 7 for $\theta = 45°$. For the 3 locations, only the x = 4.14 μm [Fig. 7(b)] case shows a small amount of drift charge collection by the transistor collector, which is complete in 2 ns. For the outside DT strike at x = 11.14 μm, the ion passes through the dummy CS junction, causing a drift component in the dummy collector charge. Collector charge collection remains mainly by diffusion, and a significant reduction is achieved with hardening.

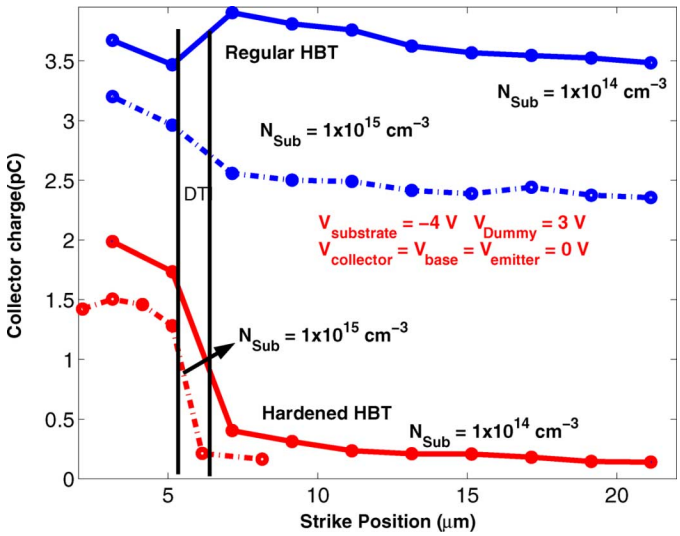

Fig. 8. Substrate doping comparison between 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3}. Normal strike.

3) High Resistivity Substrate: Substrate doping influences the charge collection for strikes outside DT by modifying the lifetime of the diffusing charges [12], [13] . Fig. 8 shows charge collection comparison for substrates with $N_{Sub} = 1 \times 10^{14}$ cm^{-3} and $N_{Sub} = 1 \times 10^{15}$ cm^{-3} for regular and hardened HBTs. Charge collection for $N_{Sub} = 1 \times 10^{14}$ cm^{-3} is higher than for $N_{Sub} = 1 \times 10^{15}$ cm^{-3} doping mainly because of the slightly increased lifetime from 9 μs to 10 μs.

IV. Simultaneous Charge Collection Issues in Multiple Devices

Previous simulations are done for a stand-alone single HBT with a large simulation area of 35 × 35 μm^2. This large area is necessary due to the large lifetime and large diffusion length in-

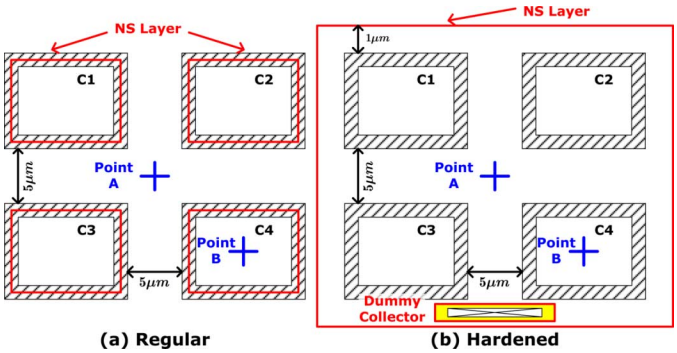

Fig. 9. (a) 2 × 2 regular HBT array and (b) 2 × 2 hardened HBT array.

volved. In circuits, however, the spacing between transistors is only several microns, which is comparable to or even less than the diffusion lengths. A single ion strike can then cause simultaneous charge collection in multiple devices near the strike location [13]. Thus we need to examine charge collection using realistic layout including multiple devices. From a hardening standpoint, we do not need to pull out the individual NS layer for individual devices. Instead, a effective way is to replace the NS of several devices by a single NS enclosing several devices, as shown below. As the ion path of angled strikes intersects with more neighbouring devices in an array of HBTs, we expect the shared dummy collector to work effectively for angled strikes and reduce charge collection in all devices. Simulation results on 2 × 2, 3 × 3 and 4 × 4 HBT arrays are presented below.

A. 2 × 2 HBT Array

Fig. 9 illustrates the layout of a 2 × 2 array for regular and hardened HBTs simulated. C1, C2, C3 and C4 are the collectors of individual devices. A 5 μm spacing, typical of circuit layouts using SiGe HBT technology, is used. Normal ion strike simulations are performed at points A and B. Point A is at equal distance from all devices, and represents the outside DT strike location for maximum charge collection sharing. Point B is the center of C4, and represents inside DT strikes.

Fig. 10 gives the charge collection comparison between the regular and hardened HBT arrays for strikes at point A and B. For a strike at point A, C1, C2, C3 and C4 of the regular HBTs collect 0.7759, 0.7758, 0.735 and 0.743 pC charges, respectively. These charges are large enough to cause simultaneous upsets in all four transistors if the critical charge is less than 0.73 pC for all of the transistors in question. The value of critical charge depends on the details of specific circuits, and a few tenths of pC is significant to cause upsets in SiGe HBT logic circuits [14].

In the 2 × 2 hardened HBT array, the dummy collector collects 3.5 pC charge through drift and diffusion, thereby reducing the C1, C2, C3 and C4 charge collection to 0.0866, 0.0863, 0.0786 and 0.079 pC, respectively, and reducing event and/or error rate. Depending on propagation of transistor upset towards circuit output, the overall circuit upset rate should be much reduced with hardening, as all four transistors are now collecting negligible amount of charge. In addition to reduced total amount of charge collection, the duration of transients is significantly

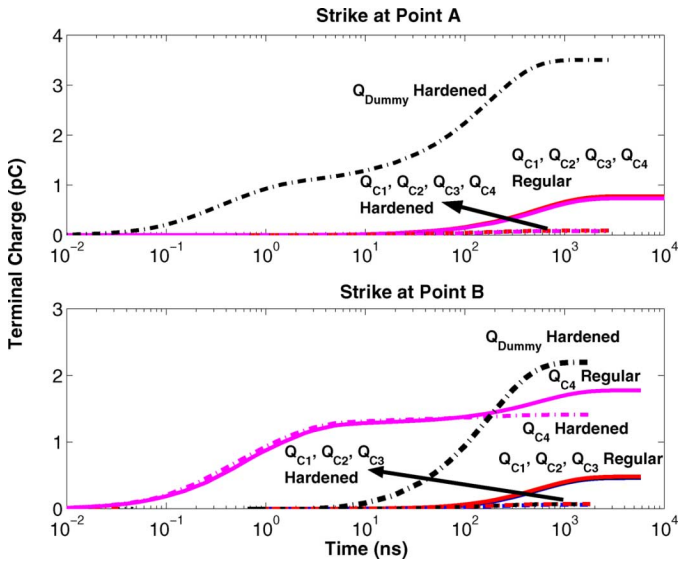

Fig. 10. Charge collection comparison between 2 × 2 regular and hardened HBT arrays for ion strikes at point A and B.

reduced, as shown earlier in the charge collection plots, because the slow diffusion charge collection by the HBT collector is suppressed. In particular, for analog and RF circuits, such as amplifiers and oscillators, we expect significant reduction of single-event transients in circuit output due to much shorter collector current transients. SEU testing of circuits with deep strikes will be needed to experimentally quantify the effectiveness of the proposed hardening approach.

For a strike at point B, the struck device C4 collects 1.7761 pC charge while C1, C2, C3 collect 0.46, 0.47 and 0.48 pC charges respectively in the regular HBT array. Even though the strike is in C4, other devices collect considerable charge through diffusion for the regular HBTs due to the long lifetimes. For a critical charge less than 0.45 pC, all of the four devices would be upset. Although the hardening approach does not significantly reduce charge collection in the struck device, it reduces the charge collection in the neighbouring devices C1, C2 and C3 down to 0.07, 0.069 and 0.058 pC, respectively, which is significant.

B. 3 × 3 HBT Array

We now examine a 3 × 3 array, with multiple incident angles. As illustrated in Fig. 11, as the angle of incidence increases, the ion path gets closer to the CS junction of adjacent devices in a regular HBT array, thereby causing more charge collection by adjacent devices. In the hardened HBT array, the ion path inevitably passes through or nearby the dummy CS junction that surrounds all of the HBTs. We therefore expect a significant reduction of charge collection overall in an array of HBTs for angle strikes as well.

Figs. 12 and 13 illustrate the layout of the 3 × 3 regular and hardened HBT arrays. Each HBT is identified with their row and column index (i, j), i = 1 : 3, and j = 1 : 3. For instance, A11 refers to the HBT at row 1 and column 1. Normal, 30°, and 45° ion strike simulations are performed at three representative points 1, 2 and 3. Point 1 is at the center of A32. Point 3 is at the center of A22, also the center of the HBT array. Point 2 is located outside the DT between A32 and A22.

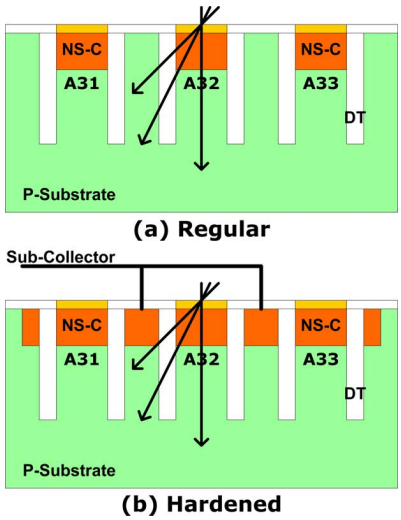

Fig. 11. A cartoon illustration of the cross-section of the regular and hardened HBT array showing the devices A31, A32 and A33 (not to scale). The ion path represents the normal and angled strikes.

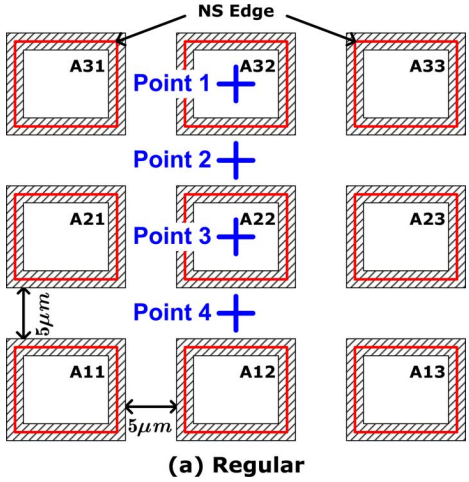

Fig. 12. 3 × 3 regular HBT array.

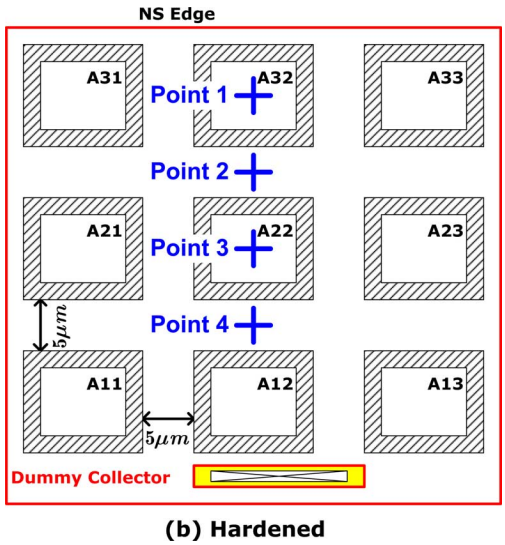

Fig. 13. 3 × 3 hardened HBT array.

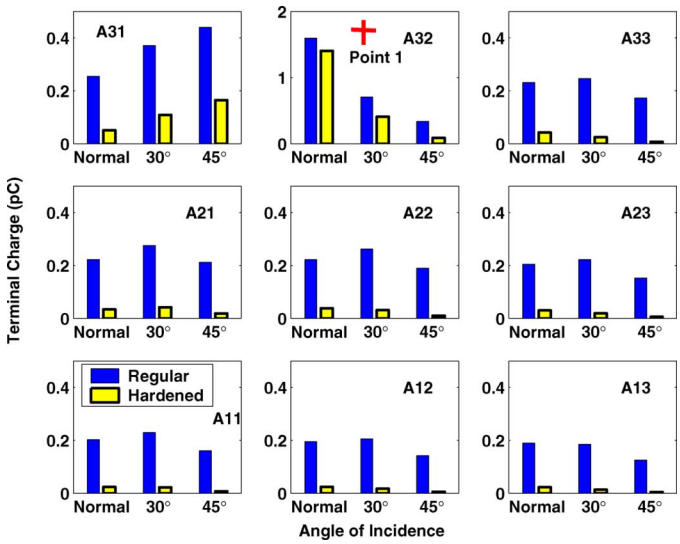

Fig. 14. Total charge comparison between 3 × 3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 1. The red cross indicates that the device A32 is hit by the ion.

Fig. 14 shows the total charge collected by all the devices of the regular and hardened HBT array for a strike at Point 1, that is, inside the DT of A32, indicated by a red cross. A32, the struck device in the 3 × 3 regular HBT array collects 1.59 pC, which is less than the 1.78 pC in the 2 × 2 regular HBT array and 3.5 pC in the stand-alone regular HBT. This clearly shows that without hardening the charge collected by the struck device decreases with increasing HBT array size, primarily because of charge sharing by adjacent HBTs. The total charge collected by all HBTs, on the other hand, *increases* with increasing HBT array size, as expected.

As in the 2 × 2 array, for normal and 30 degrees angle strikes, charge collection in the struck device is only slightly reduced by hardening. However, for every other device in the 3 × 3 array, a considerable reduction of charge collection has been achieved with hardening, as was in the 2 × 2 case, thanks to the presence of the dummy collector surrounding all of the HBTs. For 45 degree angle strike, a sizable reduction of charge collection in the struck device A32 is also observed and can be understood from examining how the ion path intersects different devices. Fig. 15 shows the total terminal charge comparison for a strike at point 3. The charge collection characteristic is similar to the charge collection at point 1.

Fig. 16 shows the 3 × 3 simulation results for a strike at Point 2, outside the DT, and in between devices A32 and A22. As charge collection is through diffusion in all of the devices in the regular HBT array, the dummy collector in the hardened HBT array yields a significant reduction in charge collection characteristic in all of the HBTs. We can therefore conclude that the shared dummy collector hardening approach works effectively for both inside and outside DT strikes, for both struck devices and neighboring devices,

C. 4 × 4 HBT Array

Fig. 17 shows the simulation results of a 4 × 4 HBT array, both regular and hardened. Only normal strikes are simulated.

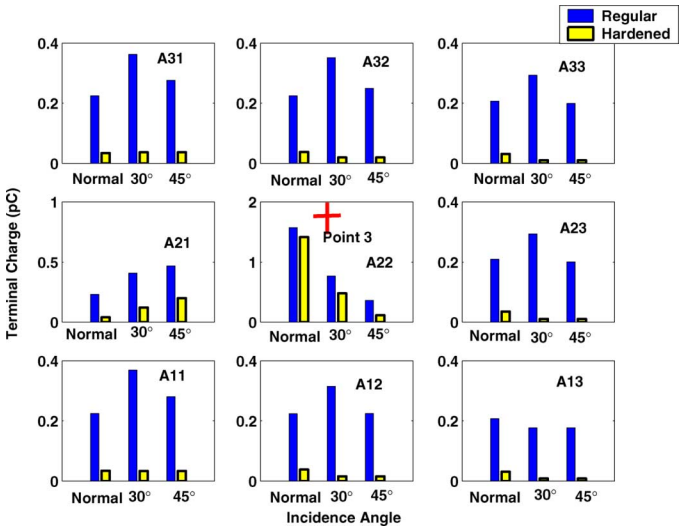

Fig. 15. Total charge comparison between 3×3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 3. The red cross indicates that the device A22 is hit by the ion.

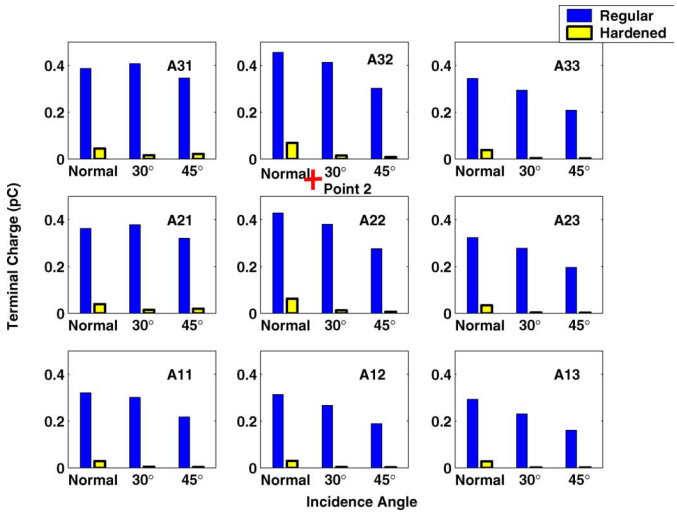

Fig. 16. Total charge comparison between 3×3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 2. The red cross indicates that the ion strike position is located between A32 and A22.

The 4 incident points are indicated by the "x"'s. P1 and P3 are inside DT. P2 and P4 are outside DT and in between devices. For the struck devices, A23 for P2 incidence, and A14 for P4 incidence, approximately 1.6 pC charge is collected without hardening. This number is about the same as the charge collected by struck devices in the 3×3 array, indicating that even though the amount of charge collected by a struck device decreases with increasing number of adjacent devices, due to charge collection sharing, the decrease becomes very gradual eventually.

Like in 2×2 and 3×3 arrays, even though hardening has only a small effect on the struck devices for inside DT incidence, it has a pronounced effect on other devices. For outside DT incidence (P1 and P3), hardening is effective in reducing charge collection by all devices.

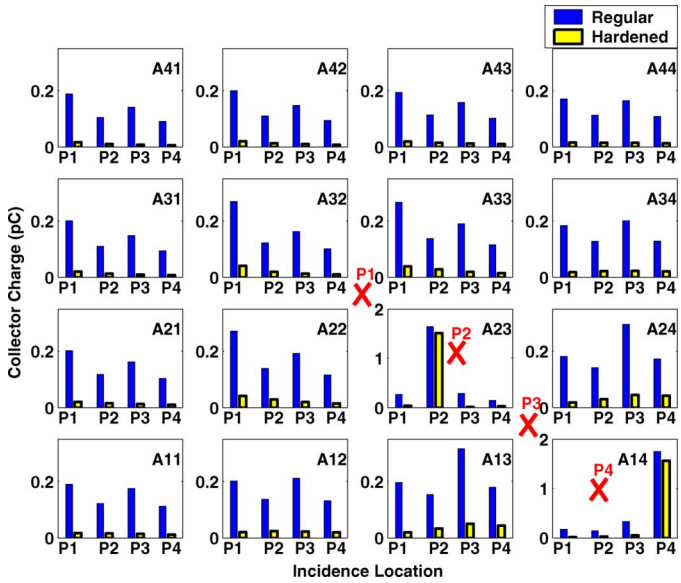

Fig. 17. Total charge comparison between 4×4 regular and hardened HBT arrays for 4 incident points.

V. Conclusions

We have proposed a SEU hardening approach that uses a dummy collector to reduce charge collection by the main transistor. The dummy collector can be obtained using existing silicon space between adjacent HBTs without process modification or area penalty, and can be shared by several adjacent devices. 3-D simulations of normal and angled incidence deep strikes are performed at representative strike locations to examine the effectiveness of the proposed approach. In all cases, the hardened devices show significant reduction of charge collection, primarily due to sharing of diffusive charge collection by the dummy collector. Impact of dummy collector width and substrate doping are examined as well. 2×2, 3×3 and 4×4 arrays of regular and hardened HBTs are simulated to examine simultaneous charge collection sharing between adjacent devices. With increasing HBT array size, the amount of charge collected by struck devices for inside DT incidence first decreases, and then stays at a significant value. Without hardening, significant charge collection sharing exists between adjacent devices, for both inside and outside DT strikes, leading to simultaneous upsets of multiple transistors. With hardening, significant simultaneous charge collection by multiple devices is suppressed considerably for normal and angled strikes, as the shared dummy collector collects a large amount of charges that would be shared by regular collectors.

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