CDF/DOC/TRACKING/GROUP/5062

An SVX3D Chip User's Companion

M. Bishai[a], M. Garcia-Sciveras[c], C. Hill[d], G. Pope[e],
J. Slaughter[f], R. St. Denis[b] T. Zimmerman[a],
Others as things develop...

(a) Fermilab, (b) Glasgow University, (c) Lawrence Berkeley Laboratories, (d) University of California - Davis,
(e) University of Pittsburg, (f) Yale University

CVS Version 2.4
July 21, 1999

Abstract

This document describes the operation and use of the SVX3D chip. The SVX3D chip is a custom 128-channel chip designed and fabricated for use in the CDF Run II silicon vertex detector. Each channel contains a preamplifer, an analog delay pipeline, ADC and data sparsification logic.

Disclaimer

This is an early draft of the document and there are no guarantees. Many figures need to be re-drawn and there are still inconsistencies and errors!. We hope that experts will read it and fix our mistakes. Please send all comments to Rick St. Denis (stdenis@fnal.gov) and Jean Slaughter (slaughter@fnal.gov).

Version 2.0 - new figures and appendices have been updated
Version 2.1 - many fixes from Rick St. Denis
Version 2.4 - partial implementation of corrections by Tom Zimmerman

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The SVX-3D Readout Device is a custom 128-channel analog to digital converter chip used by CDF in Run II to read out the silicon vertex detector. Each channel consists of an integrator (Front-End device, or FE) and a digitize/readout section (Back-End device, or BE). The input to each channel is sampled and temporarily stored in its own analog pipeline. Upon receiving a trigger signal, the relevant pipeline cell is reserved. Subsequent signals cause the data to be digitized and then read out, with a separate Wilkinson ADC for each channel. Salient features include (1)deadtimeless operation (continued acquisition during digitization and readout), (2)adjustable, loadable control parameters, including the integrator bandwidth and polarity, (3)sparsified readout with nearest neighbor logic, and (4)built-in charge injection for testing and calibration. Sampling, conversion and readout of the device are controlled by external lines while digitized data is read over a byte-wide parallel path. A unique chip identifier for each device is included in the data path as well as the identity of the pipeline cell; chips can be ganged together for daisy-chain operation.

This document is meant to familiarize the user with the functionality of the SVX3D and goes on to include detailed specifications, pinouts, timings and electrical information. It also compares a variety of methods used to read out the SVX3D, ranging from a stimulus system that sends patterns from multipurpose pattern generator to the CDF SVX DAQ. In preparing this document, sections from the "Beginner's Guide to the SVXIIE"[1] and the "Draft Device Specifications for the SVX 3 Readout Chip"[2] have been freely used and modified as required for the SVX3D.

The most significant differentce between the SVX2 and the SVX3 chips is that the SVX3 can run in a deadtimeless fashion, i.e. the front-end continues to acquire data into the pipeline while the back-end is digitizing and reading out. There were several prototype versions of the SVX3D chip, specifically the SVX3B, the SVX3C and the SVX3D-HP (radiation-soft Hewett-Packard). This document reflects the SVX3D Honeywell radiation hard version, as used by CDF in Run II. **Are there any significant changes from the rad soft D version? Tom Z. says no.**.

1.1 Historical Development

In the late 1980's, several versions of a fullly custom chip called SVX[3],[4],[5] were built and tested. The chip was designed by Stuart Kleinfelder and others at LBL and contained 128 channels of electronics. It was a second generation silicon strip readout chip, incorporating new features such as data sparsification, and was used in the CDF SVX detector in Run I.

As part of the Run II upgrade for both CDF and D0, the SVX2 was designed to meet the needs of the experiments by a collaboration of engineers at Fermilab and Lawrence Berkeley Laboratory[6],[7],[8],[9]. Requirements dictated that the device should be capable of operating at an interaction rate as fast as 132 nsec, that it have optimal performance for detector capacitances between 10 and 35 pF, and that it have an analog pipeline with a maximum delay of about 4 μsec to allow time to form a trigger signal. Initially the two experiments agreed that a deadtimeless data acquisition system with simultaneous analog and digital operations was not nexessary. Thus, when a trigger signal is sent to the SVX2 chip, data acquisition stops until the chip is completely read out. Separate acquisition and readout cycles allowed a reduced silicon area on an already overcrowded chip and significantly reduced the problem of coupling from the digital output section to the very sensitive analog input. As plans for Run II evolved, deadtime became an issue for CDF. A solution for the coupling problem was found[10] and used to develop the SVX3 chip[11]

A detailed description of the chip operation is given in Chapter 2. Its main feaures are summarized in Table 1.1 and in the list below.

The main features the SVX3D are:

1. 128 channels per chip
2. Maximum interaction rate equal to 132 nsecs
3. Optimized for capacitive loads from 10-35 pf
4. Simultaneous acquisition and digitization/readout cycles
5. Selectable input bandwidth
6. Double correlated sampling
7. Large dynamic range on input integrator to minimize deadtime due to pre-amplifier resets
8. Programmable analog pipeline (47 cells, 42 cells maximum depth for pipeline, 4 cells for trigger buffer, 1 cell for write amplifer pedestal)
9. Digitization of analog signals up to 8 bits of resolution using a Wilkenson type ADC
10. Dynamic pedestal subtraction
11. Data sparsification (zero suppression)
12. Neighbor channel readout selection(cluster readout)

Characteristic	Value
process	Honeywell .8 micron
size	11916 X 6257 microns
minimum inter-chip gap	50 mils
channels	128
power consumption	3 mW/channel
integrator charge conversion gain	5mV/fC
Write amplifer voltage gain	3
total front end charge gain	15mV/fC
total chip charge gain	14 mV/fC
pipeline dynamic range	40 fC
linearity 0-40fC	INL $<$ LSB, DNL $<$ 1/5 LSB
equivalent noise charge	500 +60 e/pF rms
integrator dynamic range	300 pF
digitization ramp rate	53 Mhz maximum
maximum ADC dynamic range	8 bits
signal/noise for 4fC input	10:1 - 20:1 (35pF - 10pF)

Table 1.1: Specifications of the SVX3D chip

13. Low noise (S/N=10:1 to 20:1 for input capacitances from 35pf to 10pf for an input charge equivalent to 1 MIP = 4 fC)
14. Low power (approximately 3 mw/channel) to minimize the cooling requirements
15. Operation compatible with double-sided AC coupled detectors
16. Ability to inject charge for testing and calibration in each channel
17. Daisy chain operation capability
18. Parallel bus data readout
19. Integral Data Valid strobe signal in the data bus (OBDV)
20. Can be implemented in the Honeywell 0.8 micron radiation hard process

This document is arranged as follows. Chapter 2 gives a detailed description of the chip's operation, including timing diagrams. Chapter 3 defines the initialization bits in detail and how to use test pulse injection. Issues on measuring the performance of the chip are given in Chapter 4. The electrical specifications are given in Chapter 5 and Chapter 6 describes how to connect and mount the chip. Chapter 7 lists a number of miscellaneous considerations. The appendices compare settings and measurements of the chip on several different test stands with those from the prototype DAQ system.

Chapter 2

Functional Description

In this chapter the function of the SVX3D is described. Section 2.1 gives a brief overview, Section 2.2 describes the operation of the chip in detail, and Section 2.3 gives detailed timing diagrams. Items in the initialization bit stream are described as they relate to operation; a concise list is deferred to Chapter 3. Section 2.4 gives the physical layout of the chip, including tables of all the input and output pads.

Note: This document attempts to standardize the names used for the various input and output signals and initialization bits. These names appear as upper case in the text.

2.1 Overview

The SVX3D consists of 128 identical channels. Each channel has has two parts, a Front End and a Back End. The Front End contains the integrator and storage pipeline. The Back End contains the ADC for digitization and the readout logic and drivers. The major cycles of operation for these parts are Initialization (both), Acquisition (Front End), Digitization (Back End), and Readout (Back End). The initialization cycle usually is performed once, followed by repeated data acquisition, digitization, and readout cycles. The Acquisition cycle occurs simultaneously with the Digitize and Readout cycles. As required by these cycles, the front and back ends are in different states or modes. Three input signals, FEMODE, BEMODE, and CHMODE, are used to change the modes as summarized in Table 2.1. To change the state of the front or back end, the CHMODE pad is raised high, the mode bits are changed, and the CHMODE pad signal is lowered to complete the transition to the new state of operation. Timing specifications and the appropriate levels for FEMODE and BEMODE for each of the three modes(initialization, acquire and readout) are given in Section 2.3.

An illustration of the operation of the chip is:

Initialize	>> Acquire	>> Acquire	>> Acquire	>> Acquire	>> Acquire	>> etc.
	>> Digitize	>> Readout	>>>>>>>>>>>	>> Digitize	>> Readout	>> etc.

cycle	FEMODE	BEMODE
Initialization	0	1
Acquisition	1	1
Digitization	1	1
Readout	1	0

Table 2.1: Determining the mode of the SVX3D chip.

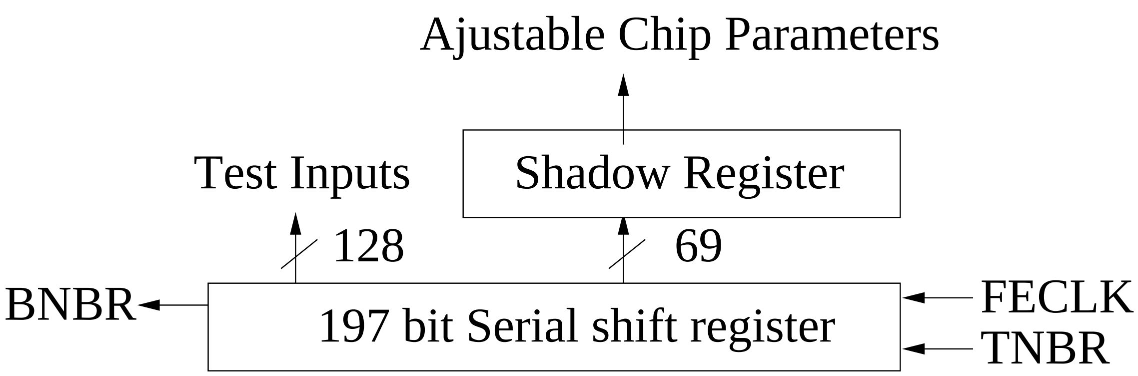


Figure 2.1: Serial shift register for downloading chip parameters.

2.1.1 Overview of Initialization Cycle

During the initialization cycle a serial bitstream of digital data is clocked into the chip to set various operational parameters of the devices and to provide a 128-bit mask that indicates which channels are to have charge injected when a calibration signal is sent. All the control bits, with the exception of the 128-bit channel mask, are transferred to a transparent latch via a strobe signal(CALSR). Bits are shifted in at the TNBR signal pin using the FECLK clock; the shifted out bits appear at the BNBR signal pin to allow for daisy-chaining of several device as shown in Figure 2.1. The pipeline cell pointer is reset as part of the initialization sequence. The meaning of the various initialization bits is introduced as required in this chapter and a systematic description is given in Chapter 3.

2.1.2 Overview of Acquisition Cycle

After the initialization cycle, the Front End should be placed in the acquisition mode until a new initialization is performed. **precisely how do you put the chip into acquistion mode?** Data acquistion occurs each cycle of the input signal FECLK. The integrator accepts charge from the detector and then transfers it to the current pipeline cell. Subsequent pipeline cells are filled in order on each clock cycle, and, if no trigger siganl is received before that cell is due to be used again, its data is lost and the pipeline cell reused. Thus, analog input values are continuously transferred to the pipeline independent of the digitization or readout states of the Back End. A signal from the trigger system(Level 1 Accept, L1A) will cause the appropriate cell in the pipeline to be marked for later readout and the pipeline address logic will skip this cell until it is released for reuse. The value of this cell is transferred to the Back End on the receipt of another input control signal, PRD1. There are four of these holding cells available, allowing multiple samples to queue up for the digitizer. The pipeline contains 47 cells so the pointer logic that controls the pipeline always has 42 cells available for data acquistion. Pipeline cell 47 is a fixed reference cell that is used to monitor and subtract off the pipeline cell pedestal. Once a reserved cell's value has been transferred to the Back End for digitization and readout, the input control signal PRD2 makes the cell available for the pipeline again. and reacquires the pedestal value stored on the reference cell of the pipeline.

The integrator can handle either positive or negative going signals. It has a dynamic range of about 300 fC. To prevent saturation, it is periodically reset during accelerator beam gaps.

2.1.3 Overview of Digitization and Readout Cycle

The digitization cycle is begun by the receipt of two PRD1 signals, which causes the difference of the charge stored on the cell to be digitized and cell 47, the reference cell, to be presented to a 8-bit Wilkinson-style ADC. Analog values are digitized using a single slope conversion technique. The ADC consists of a ramp generator and a counter (both common to all 128 chips) and a comparator and latch for each channel. Once the ramp and counter are started, the output of the ramp and the signal to be digitized are applied to the comparator. When the comparator fires, the output of the counter is latched as the digitized value of the charge. Bottom Neighbor (BNBR) and Top Neighbor (TNBR) lines are used as bi-directional semaphores to enable neighbor logic across several chips.

A unique feature of the SVX3D chip is its dynamic pedestal adjustment capability[12], [13]. This feature is enabled by setting the initialization bit DYNAMIC THRESHOLD ENABLE and is intended to give additional protection against environmental(common mode) noise in deadtimeless operation. The circuity uses all channels to calculate in real time a common pedestal and then subtracts it from each channel during digitization, before sparsification. This is equivalent to making the sparsification threshold a dynamic variable that tracks common mode pedestal fluctuations.

The actual data that is read out is selected by initialization bits THRESHOLD, READ ALL and READ NEIGHBORS. The analog comparator feeds a latch and neighbor hit logic. If both the READ NEIGHBORS and READ ALL bits are low, the channels to be read out are only those channels (i.e. hit channels) whose digitized outputs exceed the threshold set by the THRESHOLD bits. If the READ NEIGHBORS bit is set high, then hit channels *and* the channel immediately on each side of the hit channel are also read out. Readout of neighbor channel amplitudes allows interpolation to obtain higher hit location accuracy. Under some situations such as testing, all channels on a chip can be read out regardless of signal level by setting the READ ALL bit high.

The output of the neighbor logic circuit from all the channels form an ordered array of the channels to be read out. Before the chip is read out, the address and data for each channel to be read is stacked in a asynchronous FIFO for fast readout. A few hundred nanoseconds are required for the information to be stacked before readout can begin. The output information, together with a clock signal(OBDV for odd byte data valid), whose edges denote when the data are valid, are then made available in parallel form as differential signals at the BUS0–BUS7 and OBDV pads at a rate determined by the signal BECLK. Data transmission in a multichip system is based on a common data bus with tri-stated outputs and token passing between chips. Data from the active chip is output on each edge of the BECLK. Initially the chip presents its chip ID number, and then the address of the pipeline cell(time slice) being read out. Subsequently, the address and data for each pertinent channel is output. If there are no channels to read out, the token is passed to the next chip immediately after the chip ID and the pipeline cell have been readout. The Top Neighbor(TNBR)−Bottom Neighbor(BNBR) signal pair provide the token passing to allow readout of several chips in series.

The SVX3D chip has both current mode and resistor mode drivers for the differential data lines. The current mode driver is enabled (or not) when the chip is wired. The resistor mode driver is adjusted by the initialization bits DRIVER RESISTOR SELECT and DRIVER BIAS CMODE SELECT.

2.2 Detailed Operation

In this section, the operation of the SVX3D is described in more detail. Detailed timing information is given in Section 2.3.

2.2.1 Details of Acquisition - the Integrator and Pipeline

The SVX3D is comprised of 128 channels of identical electronics along with some digital circuits which are common to all channels. Figure 2.2 shows a simplified diagram of one of the identical channels of electronics and some of the common circuitry. Charge from the detector is fed directly to a free running integrator with feedback capacitor C_f and no feedback resistor. In addition to the detector input, a small separate programmable test input capacitor, C_t, is connected to each integrator. The capacitor allows each channel to be pulsed independently or simultaneously to (1) study channel operation, or (2) provide simulated events through the SVX3D to the data acquisition system. The use of this charge injection feature is described in Section 2.3.3 and also in Section 3.2.

In order to accommodate different interaction time intervals and input capacitances, the response or bandwidth of the integrator is adjusted by means of internal switches and capacitors to provide the optimal integrator output risetime and hence minimum noise. The BANDWIDTH initialization bits control the addition of binary weighted capacitors to the dominant node of the integrator. Optimum performance requires that the bandwidth be set correctly: If the risetime is greater than the effective integration time of the integrator, then some portion of a given signal is lost. If the risetime is less, the signal is noiser than necessary. The effective integration time of the integrator is the time when the Front End clock(FECLK) is low.

Each FECLK cycle the incremental change in the amount of charge stored on capacitor C_f is transferred to the pipeline as described in the next Section. As the reset takes ≥ 400 nanoseconds **This is Tom's number. I have heard 1 microsecond...** the charge is allowed to build until it can be reset by switch S_a in Figure 2.2 at a convenient time such as the major gaps in the collider beam structure.

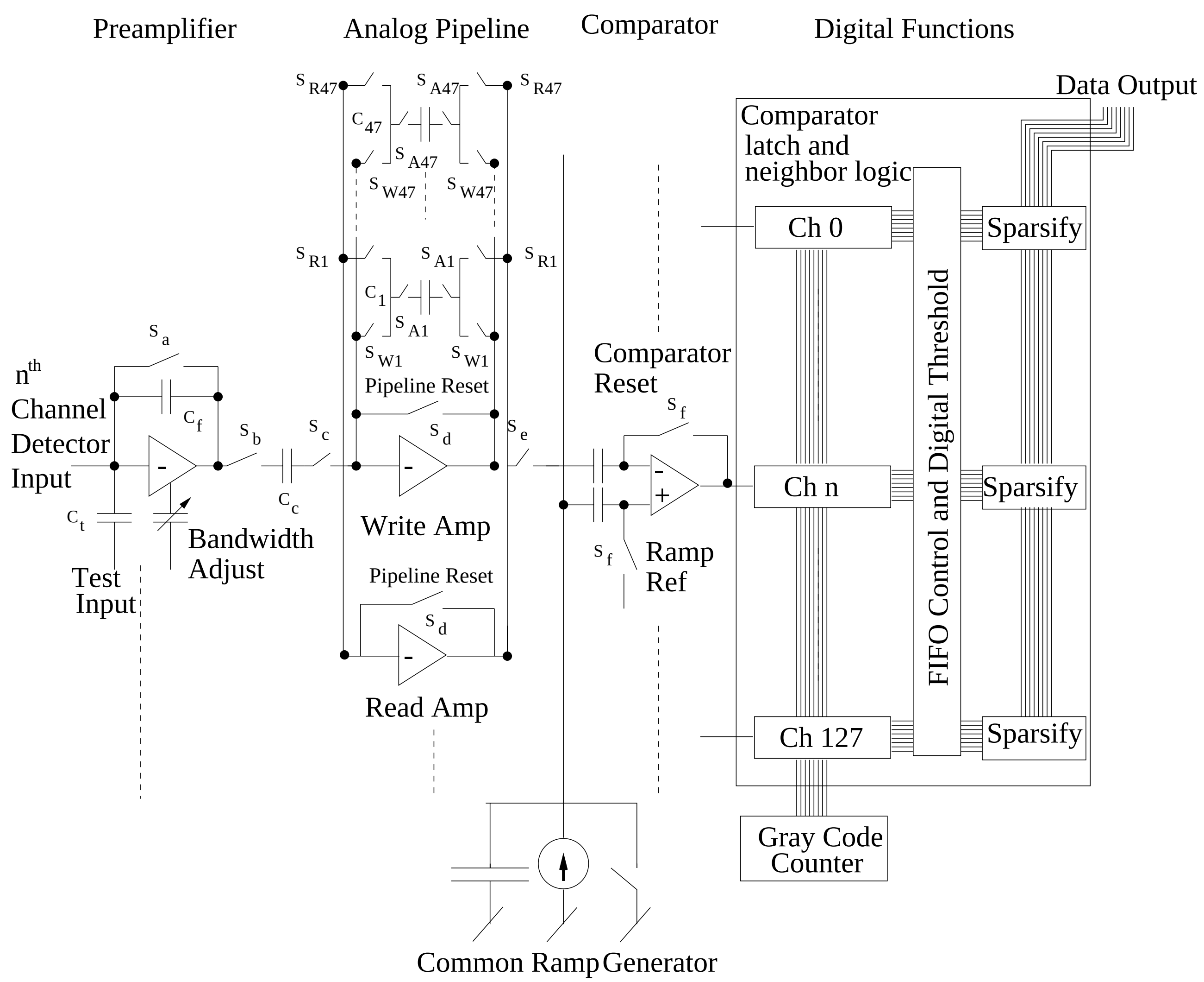


Figure 2.2: Simplified Single Channel Block Diagram. **New picture from Rick St. Denis. Need doubling checking against text. S_d on both read and write amplifers?**

The Pipeline

The output of the integrator feeds the analog storage pipeline as shown in Figure 2.2. The pipeline is dual ported for simultaneous read and write operation and consists of a write amplifer, a read amplifer and 47 identical storage cells. The method of double correlated sampling is used to transfer the amount of charge accumlated on C_f since the last acquistion. This method relies on the fact that the write amplifer op-amp always operates to keep the voltage across its input at 0 volts. Referring to Figure 2.2, the sequence is as follows: **This section needs work now we have with the final figure and the labeling of switches and capacitors.**

- During the time that the FECLK is low, switches S_b and S_c are closed. Charge from the silicon strip is integrated onto C_f.
- Close switches S_{Wn}, to route the nth storage cell capacitor into the write amplifier feedback loop, and S_d, to reset the cell. This happens on the rising edge of FECLK.
- Close switches S_b and S_c to transfer the signal from C_f onto capacitor C_c. The difference between the charge already on capacitor C_c from the previous cycle and on C_f is thus transferred to the pipeline cell (double correlated sampling) as illustrated in Figure 2.3.
- Once the signal has settled, the cell is switched out by openning S_{Wn}.

Section 2.3.2 describes the details of the timing of the various signals and clocks. Charge injection from opening S_d, S_{Wn}, and S_{An} is stored on the sample capacitor along with the desired signal. These charge injection effects are compensated during the pipeline readout where S_{An} is used again, together with S_{Rn}. **huh?** The next free pipeline cell should be reset just prior to a beam crossing. The reset occurs during the time that FECLK is high and a minimum reset time of 25 ns is required.

The write amplifier has a voltage gain of 3, which is set by the ratio of the input coupling capacitor and the total write amplifer feedback capacitance. The resultant front end gain is thus 15 mV/fC, which helps to minimize the effects of offsets in the back end ADC. The initialization bits ISEL allow for some adjustment of the internal biasing of the read and write amplifiers in the pipeline. This is explained in Chapter 3.

The operating point of the pipeline can be adjusted to give the maximum dynamic range for both positive and negative input signals. [1] When the initialization bit FE POLARITY = 0, the operating point is 0.8V, suitable for positive going signals from the n-side of a detector and for FE POLARITY = 1, it is 2.0V, for the negative going signals from the p-side. **Check these numbers - These are what Tom says.** Note that the integrator inverts the initial input signal.

Cell 47 of the pipeline is identical to all the others and is reserved for write amplifier pedestal acquistion. It is used in the analog to digital conversion process to reduce channel to channel offsets as described in Section 2.2.2. It is reset by PRD2. **more detail here?**

[1] This paper adopts the convention that the signal from the p-side of a silicon microstrip detector has charge flowing out of the integrator and corresponds to a negative going signal. This is illustrated in Figure 2.10 of Section 2.2.3.

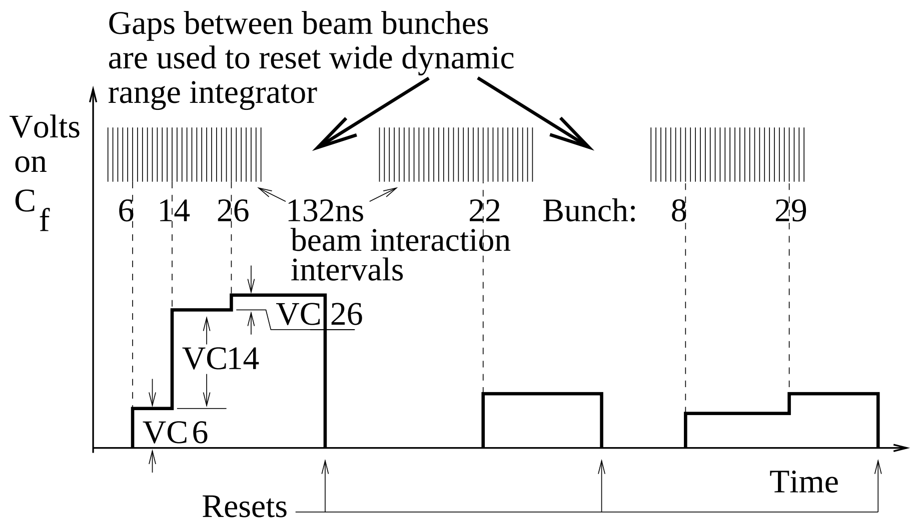


Figure 2.3: Resetting integrator during large beam gap. Schematic plot of the Voltage on the feedback capacitor of the front-end amplifier attached to a single channel versus time. The vertical lines indicate the times at which bunch crossings occur. Gaps between bunches should be used to reset the feedback capacitor, C_f. For illustration, it is assumed that the strip attached to this particular channel was hit at bunches 6, 14 and 26 in the first train, bunch 22 in the second train and bunches 8 and 29 in the third train. Only the voltage change indicated by VC6, VC14, and VC26 is passed to the pipeline cell.

Triggering and Setting a Cell Aside

As described above, the data from each beam crossing is stored sequentially in the pipeline. The pipeline must hold the data long enough for a L1A to arrive in order that the analog data for the desired beam crossing can be flagged for eventual digitization and readout. The pipeline depth is set from a minimum of 1 to a maximum of 42 FECLK clock cycles using the initialization bits PIPELINE DEPTH. This number of FECLKs thus sets the trigger latency. If a L1A does not arrive in this time, the cell is overwritten.

If a L1A does arrive, a pointer at the correct pipeline depth is set and that cell is by-passed in subsequent pipeline cell write operations until it is released after digitization by a sending a PRD2 signal. Up to four cells can be tagged. The by-passed cells are digitized and read out in the order in which they were tagged.

The system of pointers and shift registers used to tag the cells is shown in Figures 2.4 and 2.5. It is common to all 128 channels. and is used to control the simultaneous writing and reading of the pipeline. The write pointer shift register consists of a ring of 46 flip-flops Each flip-flop corresponds to a position in the pipelines of the 128 independent input channels. A token is passed from one flip-flop to the next in the ring in response to the FECLK signal. When the SVX3D is initialized the token is placed in location 1. The flip-flop which has the token selects the pipeline cell that will be used for the current acquistion cycle. In addition, the 6-bit address of the token's position is passed by the write address encoder to a 6-bit 42 cell delay register and is shifted along from cell to cell once each FECLK cycle. At the programmed(PIPELINE DEPTH) number of clocks, the write address is shifted back out of the write address delay register and is passed to both the read address FIFO and the skip address decoder. If this occurs in coincidence with a L1A, then the write address is saved by the read address FIFO and is immediately acted upon by the skip address decoder; otherwise, it is ignored. If it is ignored, then those pipeline storage cells referenced by the write address are available to be cleared and overwritten on subsequent beam crossings.

If the L1A did occur, the skip address decoder immediately sets a bypass condition on the appropriate flip-flop in the write pointer delay register. This means that the token will be passed over this flip-flop and the corresponding pipeline cells can't be used again until they are released.

The L1A increments a counter which in turn causes the next available cell in the four cell read address FIFO to be loaded. The oldest address in the read FIFO, if any, is always available to the read address decoder. When a PRD1 signal is issued, the read address decoder causes the read amplifier in each of the 128 channrls to pass the analog data from the appropriate pipeline cell to the ADC as described in Section 2.2.2. Once the data has been digitized, the pipeline cell is returned to the pipeline upon receipt of the PRD2. This signal is used in coincidence with the decoded address from the read address decoder to remove the bypass condition on the appropriate flip-flop in the write pointer shift register. The PRD2 also decrements the counter which effectively removes the oldest address in the read address FIFO.

Clearly, if more than four L1As are sent without PRD2s to clear old triggers, the chip will not operate properly. Similarly, a PRD1 when no pipeline cells are queued will also cause odd behavior. A PRD2 can be executed even when no cells are tagged in order to reset the reference cell. **The symptoms should be added here or in the timing section. Also, the considerations for then to reset the reference cell should be mentioned somewhere.**

2.2.2 Details of Digitization and Readout

An overview of the operation of the digitization and readout was given in Section 2.1.3. In this section, the process is divided up into the following steps and described in much more detail:

1. subtraction of pedestal,
2. ADC setup,
3. ADC operation,
4. threshold setting and readout,
5. dynamic pedestal adjustment.

Detailed timing information is given in Sectionsec:timing.

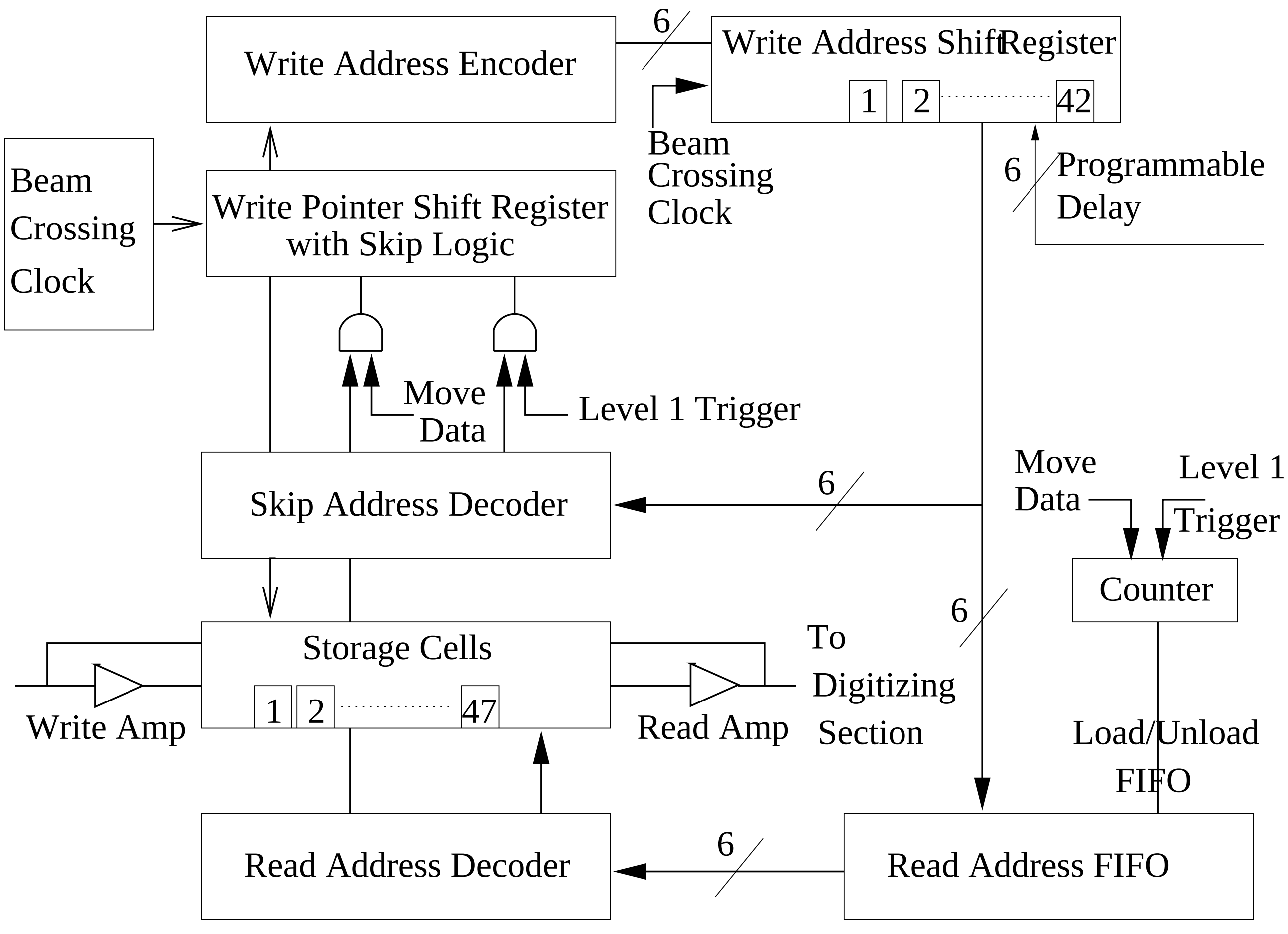


Figure 2.4: Simplified block diagram of the pipeline control logic showing the buffering and ship logic architecture required for deadtimeless readout. **Now we need to meld with other figures and the pinout! Also, the TDR has this figure but the NIM has "gate" instead of "counter" AND there is a line from Read address FIFO to the gate called FIFO Full. This could be the answer to the "what happens if we get too many triggers" question!**

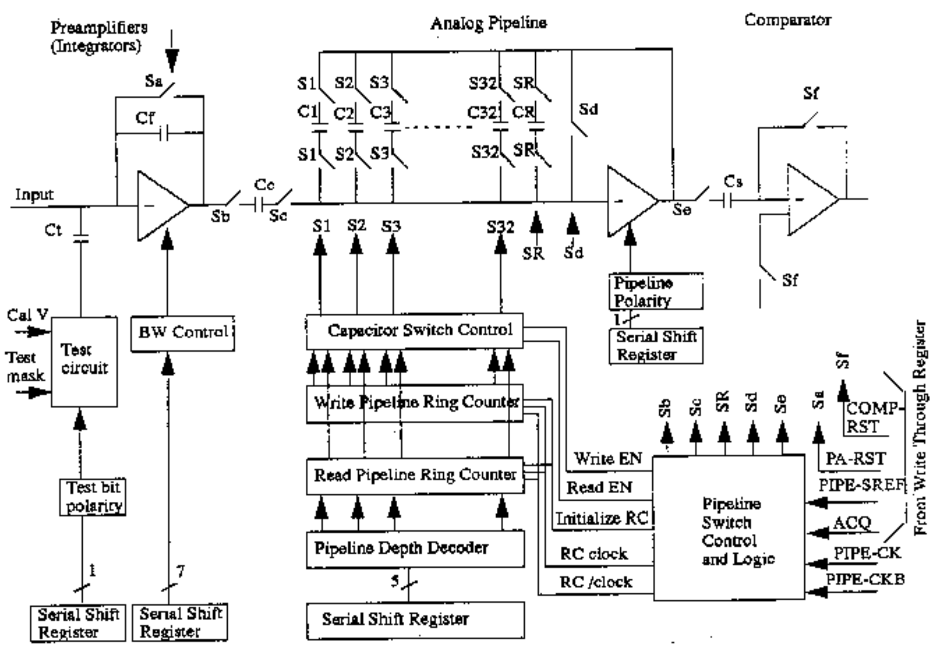


Figure 8 - Preamplifier and Pipeline Control

Figure 2.5: Illustration of the Preamp and Pipeline Control. **I think there is merit to include this stuff because we can put names to lines and signals on one end and switches and capacitors on the other end. But we need input as to which! We could also guess...**

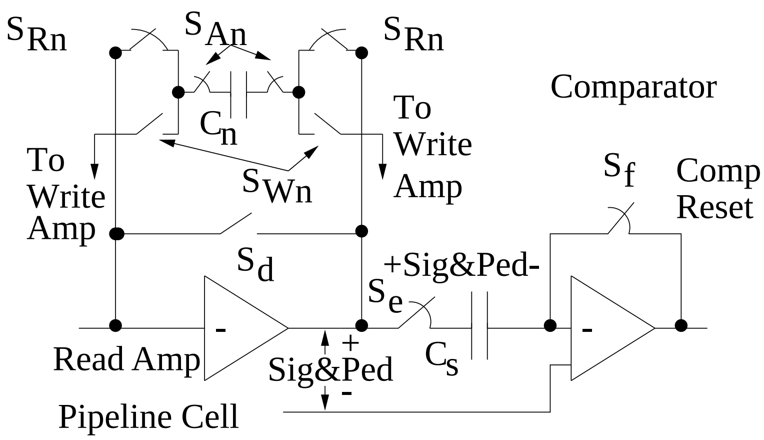
Subtraction of Pedestal

The SVX3D pipeline contains a 47th cell which is used to subtract off pedestals associated with pipeline operation. The digitization cycle is initiatied by the receipt of two PRD1 signals. If the initialization bit READOUT ORDER = 0, the first PRD1 causes the pipeline pedestal, cell 47, to be switched onto the read amplifier and the second PRD1 switches the charge stored on the pipeline cell(signal + pipeline pedestal) onto the read amplifier. If READOUT ORDER = 1, the signal cell is presented first and cell 47 second. There is an effective subtraction of the two signals presented to the ADC. Figure 2.6 demonstrates the case in which READOUT ORDER = 1, i.e. the signal is presented first. The S_{Rn} switches are closed to select the read amplifier. Then switches S_{An} are closed. **When is switch S_e used? Tom has a comment about Comp reset closed?** This causes the charge in the desired pipeline cell, which contains signal plus pedestal, to appear across C_s. (Positive signal and pedestal polarities are chosen for illustration purposes.) In (b) of Figure 2.6, the reference cell is placed on the read amplifier output. **Tom has a comment about comp reset openned. is this high or low?** The voltage stored on the coupling capacitor C_s subtracts from the pipeline output voltage to develop a voltage equal to the difference of the two signals at the input to the analog comparator. Depending on which signal is presented first, i.e. the value of READOUT ORDER, there may or may not be an effective signal inversion. Thus if READOUT ORDER is set differently for n-side and p-side signals, the same polarity signal can be presented to the ADC and the ADC can be operated in exactly the same way for both polarities.

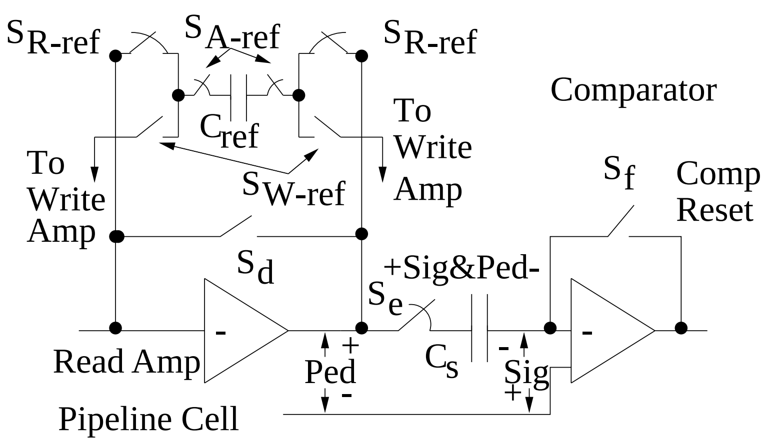
Setting up the ADC

The ADC itself consists of the ramp generator, the comparator and the Gray code counter. The process is dependent on a number of factors which are listed here and will be described more fully as the operation of the ADC is explained. The factors are:

1. Initialization bits that
   (a) set the direction(ADC RAMP DIRECTION), slope(RAMP SLOPE TRIM) and offset of the ramp generator(ADC RAMP PEDESTAL),
   (b) set the comparator direction(ADC COMPARATOR DIRECTION),
   (c) set the threshold for a valid signal(THRESHOLD),
   (d) set the maximum range of the Gray code counter(COUNTER MODULO).
   (e) adjust the bias current of the ADC comparators and the ramp op-amp, (IQUIESCENT BIAS RATIO SELECT-Not normally used and only discussed in Chapter 3.)
2. Signals whose timings are crucial to proper operation as they reset/enable the ramp, counter, and comparator of the ADC (COMP-RST, RAMP-RST, CNTR-RST, and RREF-SEL). They are input on the bi-directional Bus lines BUS0–BUS3. The timing details will be in Section 2.3.
3. External Components. The voltage ramp produced by the ramp generator is generated by a capacitor connected to a current source. The size of the current is fixed by the value of a resistor external to the chip. See Section 2.4 and Chapter 6.



a) Place Signal & Pedestal onC_s



b) Subtract Pedestal using Reference Cell

Figure 2.6: Pipeline Pedestal Subtraction is done by (a) placing the pedestal + signal on the storage capacitor from cell n and then (b) placing the pedestal on the storage capacitor from the reference cell.

Operation of the ADC

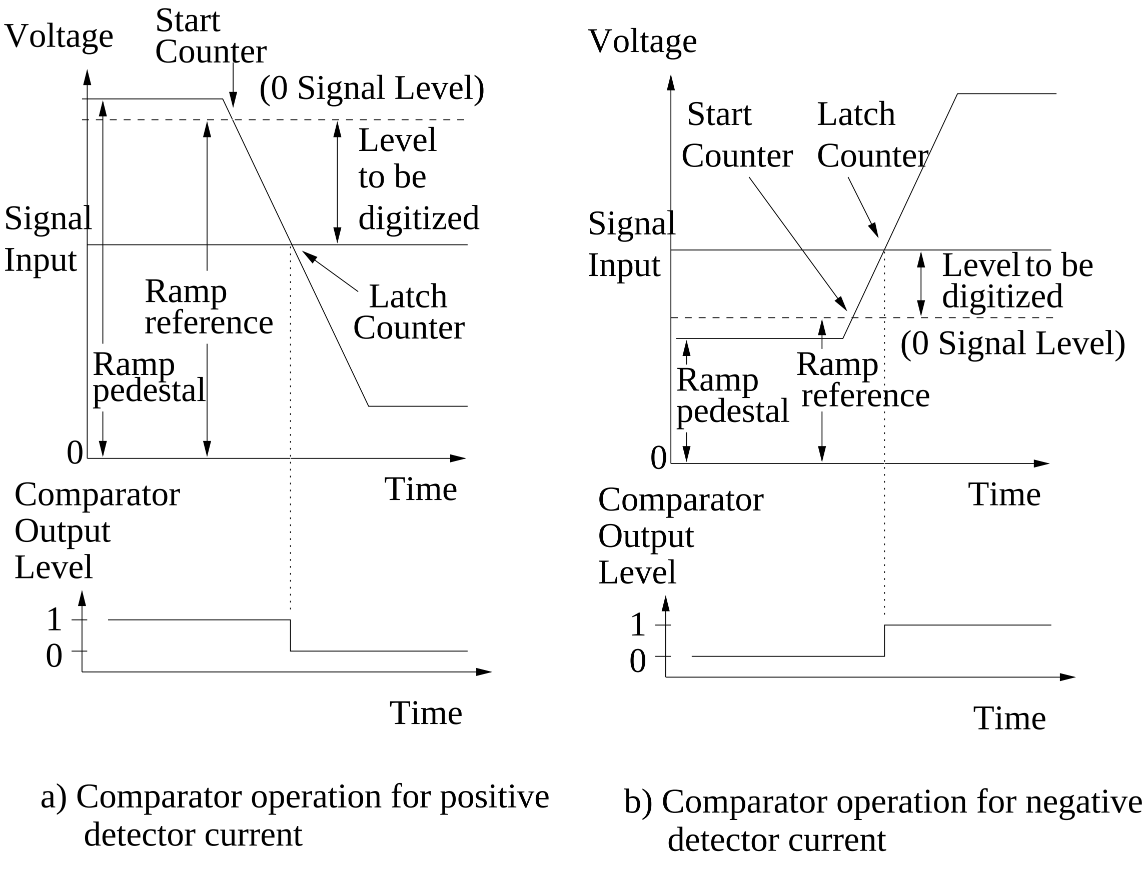


Figure 2.7: Analog Comparator Operation for positive (a) and negative (b) input current.

The sequence of operations for the ADC is illustrated in Figure 2.7 for both a rising and following ramp. The actual timing of these operations is controled by signals on the bi-directional bus lines as illustrated in Section 2.3.5. The sequence of operations is:

1. Reset the comparator and subtract cell 47 pedestal from pipeline signal, discussed in the previous paragraph. (signal COMP-RST),
2. Get the value of Ramp Pedestal, the actual starting level of the ramp (signal RREF-SEL),
3. begin the ramp (signal RAMP-RST),
4. start the Gray code counter (signal CNTR-RST),
5. the comparator fires when the ramp and input signal are equal

A rising or falling ramp is specified by the bit ADC RAMP DIRECTION; which one to use depends on the polarity of the signal at the input to the comparator. In the SVX3D chip, a positive(or negative) signal here could correspond to either polarity from the detector, depending on how bit READOUT ORDER is set, as described in Section 2.2.3. A falling ramp is appropriate for negative going signals at the ADC, while a rising ramp is correct for positive going signals.

The two levels Ramp Reference and Ramp Pedestal are very important. Ramp Reference corresponds to the level with 0 signal and is set to one of two values internally depending on the the choice of a rising or falling ramp as shown in Figure 2.7. Ramp Pedestal corresponds to the level at which the ramp actually starts. The initialization bits ADC RAMP PEDESTAL give an offset that is added to Ramp Reference to generate Ramp Pedestal. As shown in Table 3.2 this offset can be either positive or negative. Values of ADC RAMP PEDESTAL from 0-3 give negative offsets, 4 gives a 0 offset, and 5-15 give a positive offset. For a falling ramp Ramp Pedestal should be bigger than Ramp Reference, thus values from 5-15 should be used. The opposite is true for a rising ramp. **Tom had a question about this.**

Having established the starting level and slope of the ramp, the next step is to decide The ramp offset established by ADC RAMP PEDESTAL serves two important purposes. First, the nonlinearity at the start of the ramp generator is passed before any comparator can flip. Second, the value of ADC RAMP PEDESTAL provides a fine control for adjusting the pedestal. **Is this true? used to say noise hits at any given threshold.** A 1 mv change in Ramp Pedestal corresponds to a 400 e shift in the threshold level which has been set. **??? what is the range? Tom says it depends on BE clock frequency, ramp slope,**

The offset between Ramp Reference and Ramp Pedestal can cause a count offset at the output if the counter clock is started with the ramp. However, this offset can be largely corrected by delaying the start of the digitizing counter clock until the ramp input to the comparator is nearly equal to the zero signal input level. Ramp Reference may be forced to a specific values by applying voltage to the RAMPPED pad.

The slope of the ramp is determined by the value of an external resistor. This sets the sensitivity of the ADC, i.e. number of ADC counts per electron. However, the RAMP SLOPE TRIM bits 167-174 can be used to trim the value of the charging capacitor in the ramp generator to correct for changes due to process variations. However, the feedback capacitor in the integrator stage and the ramp capacitor in the ADC are fabricated in the same manner. Therefore to a first approximation, gain errors caused by integrator capacitor variations are compensated by similar changes in the A/D converter capacitor. Thus, the ability to adjust the ramp capacitor with high precision may not be needed.

Threshold and data sparsification

The hit threshold level for an SVX3D chip is set digitally (bits THRESHOLD) and is the same for all channels on that chip. The maximum count number that the A/D converter can reach during digitization is set by a Gray code number using the COUNTER MODULO bits 183–190. To achieve the largest count (255) on the SVX3D, the downloaded number is 10000000. For a count of 127, the downloaded number is 01000000; for 63 counts the number is 00100000, etc., as indicated in the Gray Code conversion Tables C.1 and C.2 in Appendix C. The threshold level for a hit channel is set digitally by a Gray Code number using the THRESHOLD bits 175-182. Normally the threshold level is set well below the maximum A/D converter count setting. If the threshold is set above the

Action	READ NEIGHBORS	READ ALL
Sparsify: read channels over threshold plus the two nearest neighbors	1	0
Sparsify: read only channels over threshold	0	0
Read all data	1	1
Read all data	0	1

Table 2.2: Data readout according to setting of READ NEIGHBORS and READ ALL bits.

maximum A/D converter count setting, no channels on that chip should indicate a hit. In this manner, a chip in a daisy chain is quickly skipped over (except for chip ID and status).

Readout

As shown in Figure 2.2, the analog comparator feeds a latch and neighbor hit logic. The SVX3D data readout can take one of three different forms depending on the status of two control bits called READ NEIGHBORS and READ ALL in the neighbor hit logic. If both of these bits are low, the channels to be read out are only those channels (i.e. hit channels) whose digitized outputs exceed the threshold level which was set during initialization via the THRESHOLD bits. f the READ NEIGHBORS bit is set high, then hit channels *and* the channel immediately on each side of the hit channel are also read out. Readout of neighbor channel amplitudes allows interpolation to obtain higher hit location accuracy. Under some situations such as testing, all channels on a chip can be read out regardless of signal level by setting the READ ALL bit high. If by accident both READ NEIGHBORS and READ ALL are set high, all channels are read out. This is summarized in Table 2.2. When chips are daisy chained together, neighbor information is passed from one chip to another using the top/bottom neighbor logic (TNBR, BNBR) so that if an end channel is hit, a neighbor channel on the adjacent chip is read out.

The output of the neighbor logic circuit from all the channels form an ordered array of the channels to be read out. Before the chip is read out, the address and data for each channel to be read is stacked in a asynchronous FIFO for fast readout. Time must be allowed between digitization and readout for the FIFO to settle as described in Section 2.3.6. When readout does begin, channels are read out sequentially beginning with the lowest address channel. Channel 0 is at the top for a chip which is viewed with its detector inputs on the left hand side.

The digitized data is read out on a tri-stated eight-bit parallel bus. The information that is on the bus changes with each half cycle of the BECLK clock. When readout of a chip begins, the chip ID number appears first on the high part of the clock cycle and then an 8 bit pipeline cell number appears on the following low half of the clock cycle. Only the lowest 6 bits are used to encode the cell number. After the first complete clock cycle, address and the data appear on alternate halves of the clock cycle until the chip is completely read out. The channel numbers are binary encoded and the channel contents Gray number encoded.

Unlike previous versions of the SVX family of chips, the SVX3D has two output driver schemes for the differential data bus and OBDV, a current mode driver and a resistor or voltage mode driver. A simplified diagram is given in Figure 2.8. They are not really separate circuits. It is expected that the differntial data lines will be terminated in the receiver with a resistor across the differential outputs as is done on the port card by CDF.**Is there a reference for the portcard?**

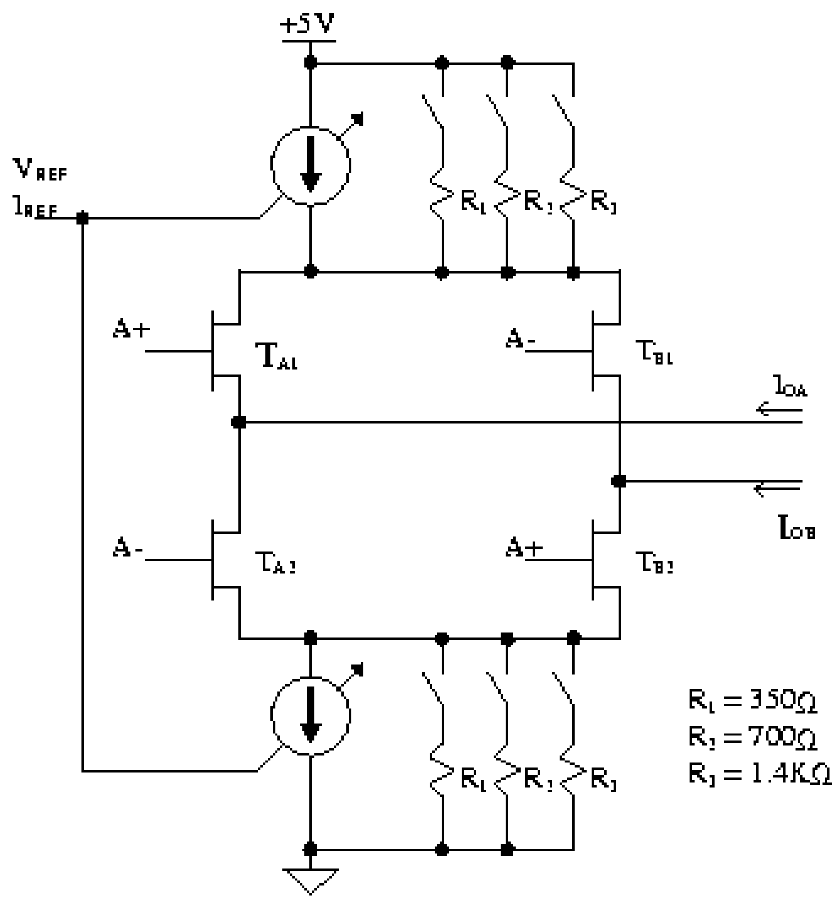


Figure 2.8: Diagram of the differential drivers/receivers. **This figure probably needs to be tweaked. It comes from the lcds document by Sergio Zimmerman.**

The current driver is enabled by tying the I_{drivers} pin to ground though a resistor whose value adjusts the current, and disabled by tying the I_{drivers} pin to +5V. **- what is the algorithm?** The common mode voltage of the current mode driver can be adjusted with the initialization bit DRIVER BIAS CMODE SELECT. If this bit = 0, the common mode voltage should be +2.5 V, if the bit = 1, +1.7 V. It has no effect if the current driver is not enabled. Tests show that common mode voltage with the simple resistor termination can vary significantly during a single read out and that the expected common mode voltage may not be what is actually seen.

The resister mode output driver is controled using DRIVER RESISTOR SELECT bits. Each of the three select bits switches in a set of driver resistors. Any or all can be switched in. Setting the MSB to 1 results in a driving current of about 6.3mA, the middle bit adds about 3.3mA and the LSB about 1.7mA. The common mode voltage of gthe resistor driver is 2.5 V. **What are the considerations here for chosing the proper resistors settings?** Of course, if the the current mode driver has been enabled, the values seen will be different. Conversely, the settings of these bits will affect operation when the current mode driver is enabled.

Dynamic Pedestal Adjustment

This feature[12], [13] is enabled by setting the initialization bit DYNAMIC THRESHOLD ENABLEand is intended to give additional protection against environmental(common mode) noise in deadtimeless operation. Its proper operation relies on two conditions:

1. Low hit occupancy
2. Uniform pick-up of environmental noise in all of the 128 channels.

The circuity uses all channels to calculate in real time a common pedestal and then subtracts it from each channel during digitization, before sparsification. The implementation simply changes the time of the start of the ADC counter from its normal location when the ramp passes Ramp Reference to a later time t_p at which a channel at pedestal would fire. The time t_p is determined by a "demoncratic election" in which every channel casts one vote. The comparator output from each channel is capacitively coupled to a common capacitor in parallel with the input of a discriminator, the output of which is used to start the counter. After a certain number of comparators have fired, the voltage across the common capacitor will reach the discriminator threshold, at which point the counter will start(t=t_p). Because channels at pedestal fire very close in time, t_p is sharply defined. The discriminator threshold is adjustable. **How is it adjusted? Do we need/have a drawing for this circuit? what about the external resistor and what is the calibration?**

2.2.3 Input Signal Polarity and the Polarity bits

The SVX3D is designed to work with double sided detectors and thus is able to accept both positive and negative current input signals. For proper operation, externally programmed polarity signals are used to choose either positive or negative input operation for the chip. Four bits (FE POLARITY, READOUT ORDER, ADC RAMP DIRECTION, and ADC COMPARATOR DIRECTION) are provided for maximum flexibility to set levels inside the chip and establish the proper operation. A fifth bit (CAL DIRECTION) sets the direction current flows for the test pulse.

The polarity signals perform three different functions inside the SVX3D chip. First FE POLARITY sets the reset point in the pipeline amplifier to one of two different values so that the output range of

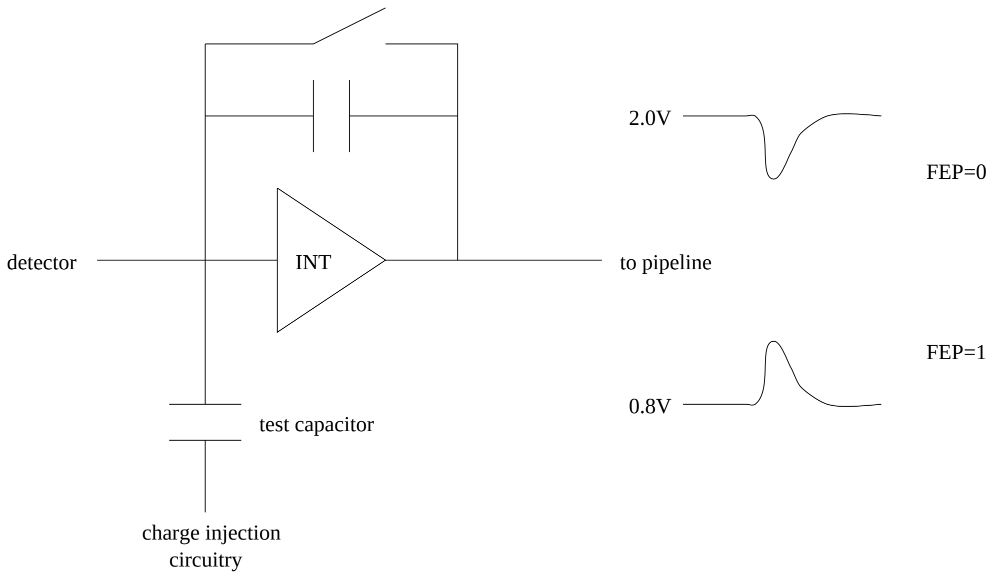


Figure 2.9: Function of the FE POLARITY bit.

the pipeline can be maximized for a given polarity, as shown in Figure 2.9. Knowing which side of the detector a given chip is bonded to therefore determines the value of this bit. Figure 2.10 shows the proper polarity setting for both cases.

In the case where the SVX3D chip is not bonded to a detector, or the chip is to be tested independently of the sensor, the test charge injection circuit may be used. In this circuit, a voltage difference is placed across a small test capacitor connected to the integrator input. A switch, with position controlled by the CALSR line, selects either the externally provided voltage VCAL or an internally generated level of 2.5V. The value of CAL DIRECTION bit determines the order in which the two voltages are presented. Figure 2.11 summarizes the possible scenarios when the rising edge of CALSR is used to inject charge. Using the falling edge of CALSR effectively reverses the meaning of the CAL DIRECTION bit.

The READOUT ORDER bit controls the order in which the pipeline cell and the reference cell are subtracted as they are transferred to the ADC. The details of the signal subtraction are shown in figure 2.6. This can be used to allow signals of either polarity to look the same to the ADC. As shown in figure 2.12, the pipeline inverts the output of the integrator, which is itself inverted with respect to the input. Setting READOUT ORDER to 0 keeps the same signal polarity that comes out of the pipeline, and setting it to 1 corresponds to a third signal inversion.

The ADC RAMP DIRECTION bit controls the direction (rising or falling) of the ramp generator. ADC COMPARATOR DIRECTIONsets the direction in which the comparators are active. In practice these bits are always set equal to one another and are collectively referred to as the Back End Polarity (BEP). Figure 2.13 demonstrates the operation of the ramp for both polarities.

There are many possible combinations of the polarity bits. By making the following conventions, the possibilities can be reduced to two, one for each polarity of input signal.

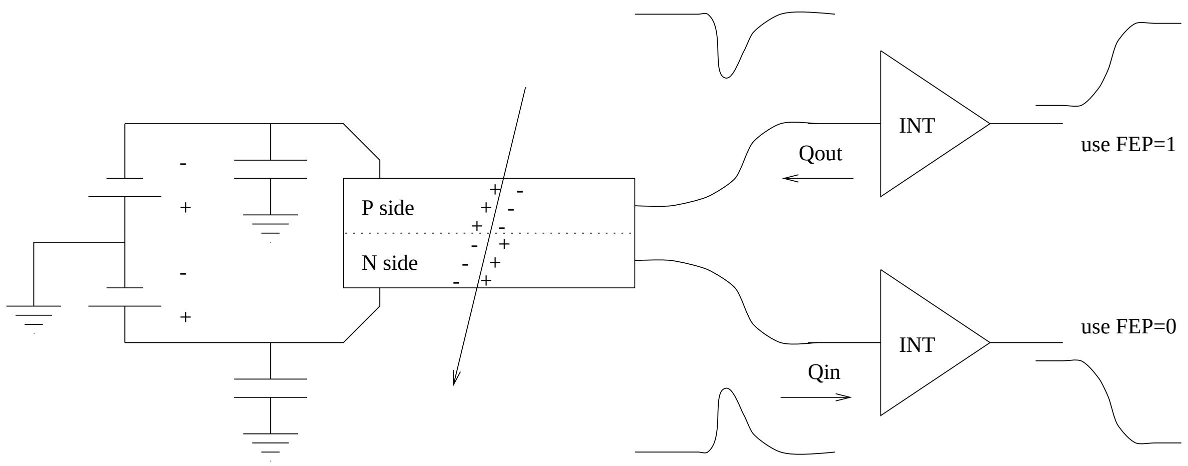


Figure 2.10: Response of the integrator to signals from a detector.

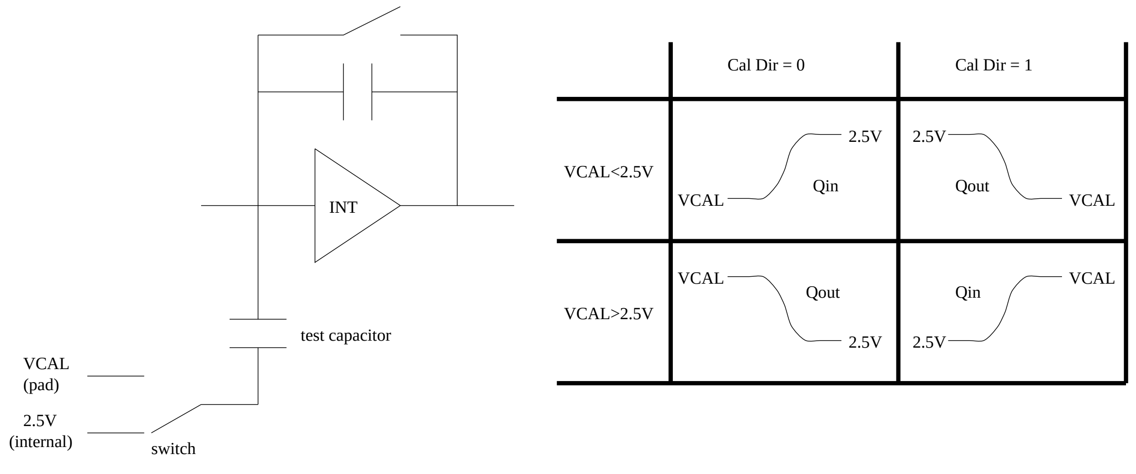


Figure 2.11: Operation of the test charge injection circuit.

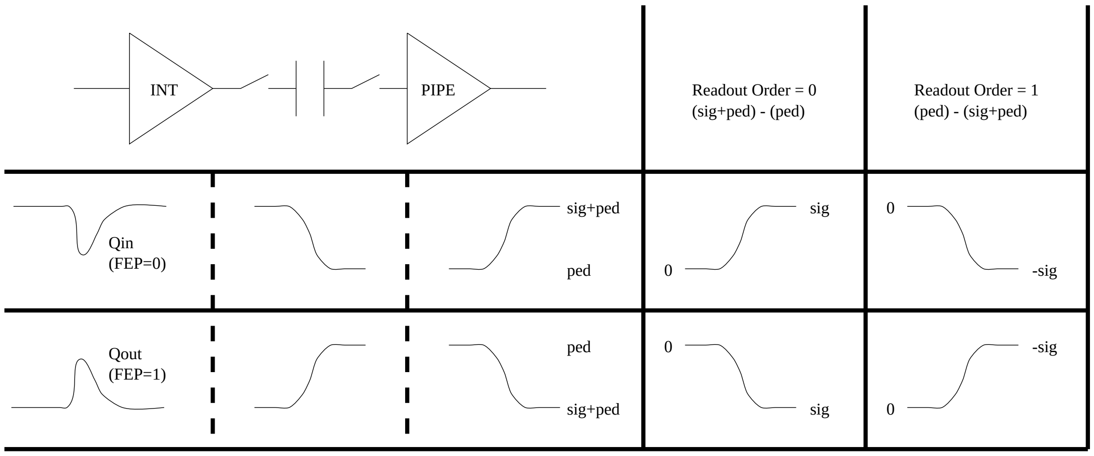


Figure 2.12: Function of the READOUT ORDER bit, and the pipeline pedestal subtraction.

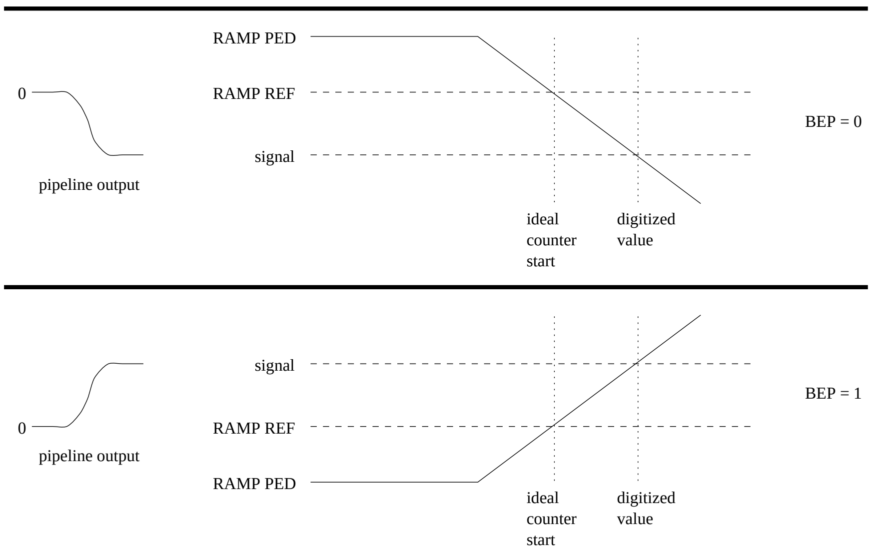


Figure 2.13: Operation of the ADC.

bit	n-side	p-side
FE POLARITY	0	1
READOUT ORDER	1	0
ADC RAMP DIRECTION	0	0
ADC COMPARATOR DIRECTION	0	0
CAL DIRECTION	1	0

Table 2.3: Recommended settings for the polarity bits

1. Use rising edge of CALSR to inject charge
2. Use VCAL $> 2.5V$
3. Use falling ramp

The two sets of polarity settings are summarized in table 2.3.

2.3 Detailed Operation with Timing Diagrams

This section gives detailed timing diagrams and considerations for all the cycles.

2.3.1 Timing of Chip Initialization

The initialization sequence for the SVX3D is shown in Figure 2.14 where the I/O control pads for the SVX3D are shown on the left side. The chip is placed in the Initialization state by raising CHMODE pad high, setting FEMODE low and BEMODE high, and then lowering the CHMODE pad signal to complete the transition. Chip parameter information is then placed on TNBR to be shifted into the 197-bit serial shift register. Once CHMODE has fallen, the FECLK clock signal to the chip is started as the serial shift register clock at the same time as the initialization bits are loaded onto BNBR. Data may be downloaded with a 50% duty cycle clock at speeds up to 53 Mhz.

An entire initialization sequence is shown in Figure 2.14. (The proper order of presentation of the bits is given in Chapter 3.) The waveform for BNBR shows three of the bits. Bits 1 to 3 show the first three bits of the test mask for a calibration charge injection test pulse on channels 127, 126, and 125. Channel 126 is masked out. Bit 197 is shown set high to set the MSB of the ramp pedestal. When the clock for bit 197 goes low, the first bit that was loaded into the shift register appears on BNBR and is available for TNBR of the adjacent chip to load parameters into that chip. In other words, the shift registers of all chips that have been daisy chained together should be considered as one large shift register and a total of 197 times the number of chips must be downloaded in total. When all of the bits have been loaded into all the shift registers of the daisy-chained chips, CALSR is raised to load some of the shift register bits into the shadow registers as shown in Figure 2.1. The 128 bits for the test mask do not have a shadow register. When CALSR is lowered, the initialization parameters are

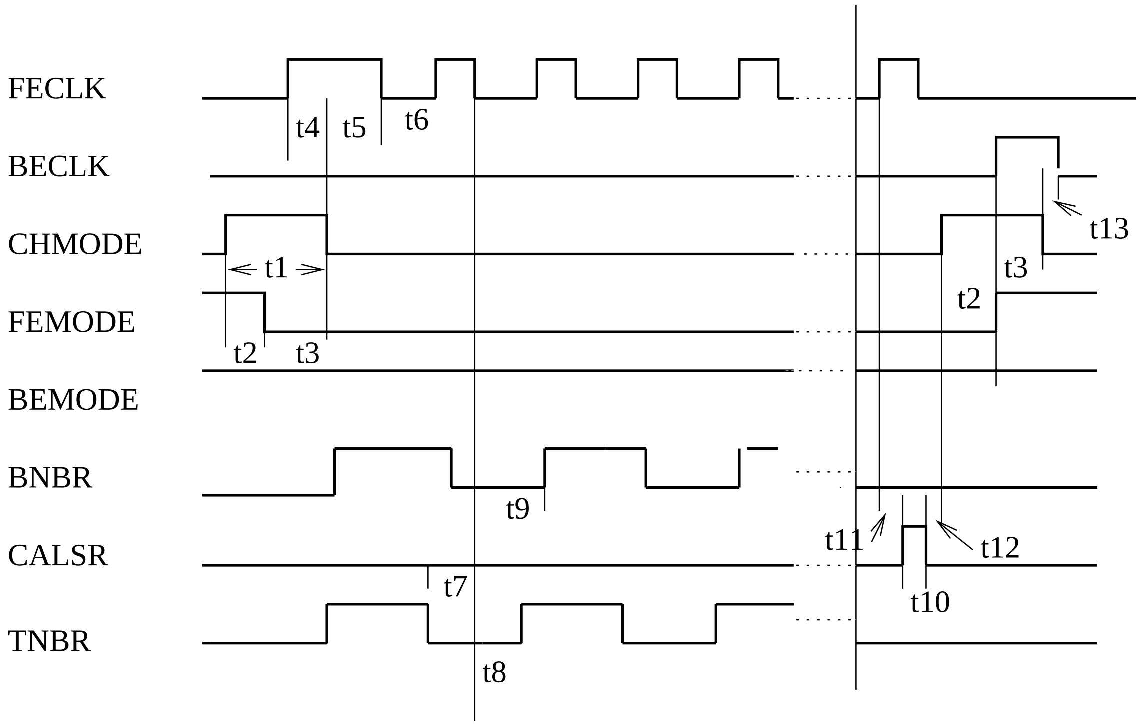


Figure 2.14: Initialization cycle.

Parameters	No.	Minimum	Maximum
CHMODE ↑ width	t1	100 ns	—
CHMODE ↑ to FEMODE ↑ or ↓	t2	25 ns	—
FEMODE ↑ or ↓ to CHMODE ↓	t3	25 ns	—
FECLK ↑ to CHMODE ↓	t4	10 ns	—
CHMODE ↓ to FECLK ↓	t5	t4+30ns	—
FECLK cycle time	t6	50ns	—
TNBR data setup to FECLK ↓	t7	20 ns	—
TNBR data hold after FECLK ↓	t8	20 ns	—
BNBR data ready after FECLK ↓	t9	20 ns	—
CALSR pulse width	t10	???	—
last FECLK ↓ to CALSR ↑	t11	???	—
CALSR ↓ to CHMODE ↑	t12	???	—

Table 2.4: Timing specifications during initialization. **Fix the figure- it doesn't show the implied break.**

Figure 2.15: Illustration of the transition from the initialization state to acquire state.

latched in the shadow registers. (In wiring up a set of daisy-chained chips, it is assumed that CALSR signal will be simultaneously applied to all the chips so that they are all loaded in parallel.) Raising CALSR also initializes the pointers in the pipeline shift registers. Initialization of the chip is complete and operation can be the CHMODE pad is raised high, transferred to the next state.

It is not possible to read out the shadow register. The best way to check the initialization procedure is to send the bit stream twice and compare the output on BNBR to what was sent.

The following signals should be set to a steady state level at least 25 ns before the falling edge of CHMODE and held at that level throughout the Initialization cycle:

- HIGH - BEMODE, L1A, and BUS0 – BUS7.
- LOW - FEMODE, PRD1, and PRD2.
- TRISTATED - BNBR.

2.3.2 Timing of Data Acquisition

The integrator and pipeline sections of the SVX3D in Figure 2.2 are active in the Data Acquisition mode. There are numerous switches which need to be opened and closed in the proper sequence. Many of the switches and critical timing issues are controlled internally. Critical external timing issues for data acquisition are addressed in this section.

The Acquire mode is entered by controlling the CHMODE and FEMODE lines as shown in the timing diagram of Figure 2.15. BEMODE is irrelevent to data acquisition. CHMODE is raised high, during which FEMODE is set to 1. When the CHMODE line is lowered, the SVX3D is in Acquire mode.

Before operating in the Data Acquisition mode, the proper parameters for the integrator and pipeline must have been downloaded into the serial shift register during initialization.

Prior to raising the CHMODE line, the integrator reset switch S_a controlled by PARST must have been closed for more than 200 nsec to insure adequate reset of the front end integrator. This is accomplished by having PARST set to a high condition at the end of Initialize. After the reset switch is opened (when CHMODE goes low), the integrator must absorb the charge injection from S_a. Data acquisition should not begin until the integrator response stabilizes which takes a time at least equal to the 0-99% risetime programmed into the integrator. If data sampling begins immediately after CHMODE goes low as shown in Figure 2.15, the first data sample after CHMODE goes low will have a large signal due to charge injection from opening the integrator reset switch.

The rising edge of FECLK is used to advance the write and read pointers in the pipeline and initiates reset of the next capacitor in the pipeline. While the clock is high, the pipeline reset switch S_d is closed. The FECLK should be phased so that the clock goes low (and the reset switch opens) at the instant a beam crossing takes place. To insure a complete reset, the clock should be high for a least 25 nsec. When operating with 132 nsec interaction times, the reset should not exceed 30 nsec in order to allow for maximum integration time and minimum noise. **Is this paragraph out of place?**

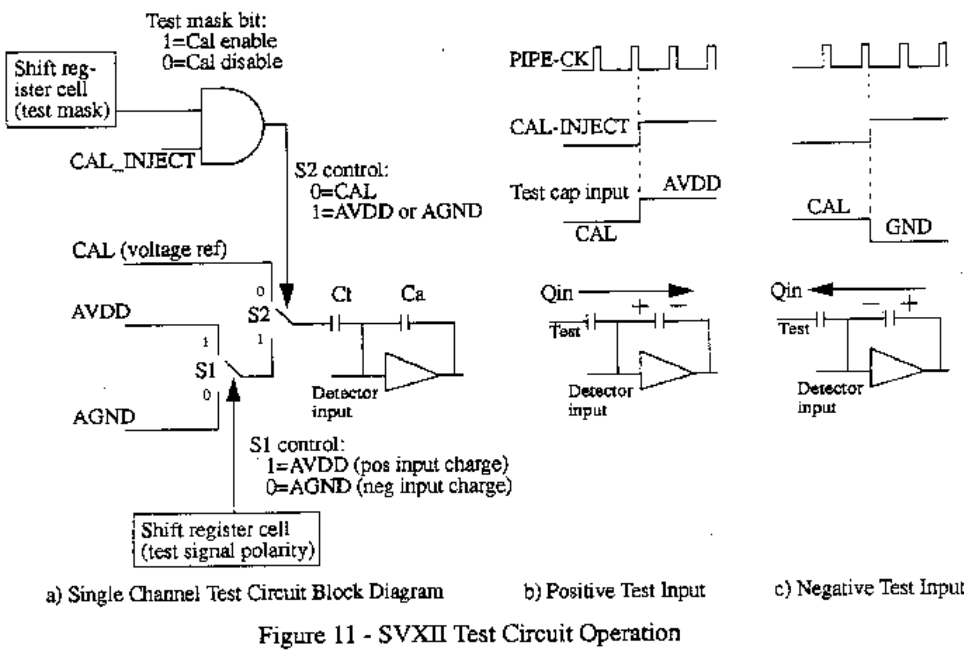


Figure 2.16: SVXII Test Circuit Operation.**This diagram needs to be changed ala George's sketch.**

2.3.3 Timing of Charge Injection

Each channel of the SVX3D has a test charge circuit which is programmed by two bits in the serial shift register. The test charge can be activated during the data sampling period and read out after the delay set by the downloaded pipeline depth. Test input charges are generated by switching a voltage through a small capacitor into the integrator input as shown in Figure 2.11. Polarity of the charge input is controlled both by the magnitude of VCAL and by the value of the CAL DIRECTION polariy bit.

The test pulse is generated by using an external voltage on the VCAL pin, and switching the test input voltage from an internally generated 2.5V to VCAL on the rising edge of CALSR and from VCAL to 2.5V on the falling edge of CALSR. Depending on the magnitude of VCAL with respect to 2.5V, this will provide either a positive or a negative charge injection at the rising edge of CALSR, and the opposite sign charge injection on the falling edge. This is illustrated in Figure 2.11.

Parameters		Minimum	Maximum
FECLK ↓ to L1A ↓	t1	5 ns	tc - 5 ns
L1A pulse width	t2	???	
L1A ↑ to FECLK ↑	t3	5	tc - 5 ns
L1A recovery time	t4	15	

Table 2.5: Timing Specifications for the Level 1 Accept

For each channel of the SVX3D the test pulse is gated with a test mask bit. Only channels for which the mask bit has been set to 1 will have the test charge injected. For proper operation, the rising edge of the CALSR should coincide with the falling edge of the clock (opening the pipeline reset switch). CALSR should stay high for at least one interaction interval.

More detail on charge injection, specifically setting the proper polarity bits, can be found in Section 3.2

2.3.4 Timing of Front End Level 1 Accept

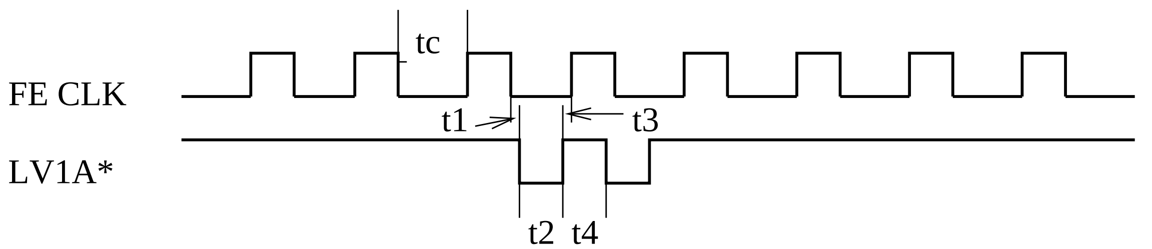


Figure 2.17: Level 1 accept. **fix to show real duty cycle and to give example of which cell is tagged.**

Asserting L1A marks a cell for digitization and readout. The cell is skipped until it is put back with a PRD2 signal. Successive cells marked by L1A are processed in the order in which they received L1A's.

As shown in Figure 2.17 and Table 2.5, assertion of a L1A (active low) must occur between FE-clocks during low cycle of FECLK (high of $\overline{\text{FECLK}}$). L1A must go low and return to high within a single integration period.

The cell number marked by the L1A is determined by the delay set by the initialization bits PIPELINE DEPTH. When in Initialize, the pipeline is set to cell 0 upon a CALSR signal. It will stay on cell zero until the first FE clock where it will advance the pipeline to cell 1, 2, 3 .....m etc. on the rising edge of the FE clocks. FECLK is normally set to go low at the instant that a beam crossing takes place. If the crossing of interest occurs for FECLK number m and PIPELINE DEPTHis set to n, then L1A should go low on clock m+n. **is this correct?** The number of clocks set by the initialization bits PIPELINE DEPTH must be reached before L1A's can be received by the SVX3D. This means for example, if the depth is set to 3 then 3 FE clocks are required to get the first cell ID into the skip logic pipeline.

At some point after digitization, PRD2 must be asserted (active high) to put the recently processed cell back into the pipeline. This MUST be done prior to processing the next event **Otherwise you reprocess the same event over again?**. It is preferable to do this during a beam gap because PRD2 also resets the pipeline reference capacitor. **somewhere put note from Tom of the effect if a L1A coincides with PRD2. Also widely varying times between PRD2's will cause a problem?**

It is illuminating to consider the special case where cell m has just been digitized and returned for use by a PRD2, but the pipeline pointer is pointing to m-1. More precisely, the pointer is on cell m-1 for the raising edge of PRD2 (and the falling edge is in the next bucket.). The pointer will count m-2, m-1, m+1, m+2, etc. Cell m will not get back into the pipeline until the next time around. This is only if the place to put the cell back is being passed by the token at the same time that the cell is being put back. /bf /large check this!

2.3.5 Timing of Digitization

Setting up of the various parameters that control operation of the ADC was covered in Section 2.2.2.

The critical timing conditions for the pipeline readout section are shown in Figure 2.18. After the trigger signal arrives, the pipeline requires at least 560 nsec to read out the desired signal before digitization can begin. **Does trigger mean L1A or PRD1? What is the minimum time between l1A and the PRD1s**?

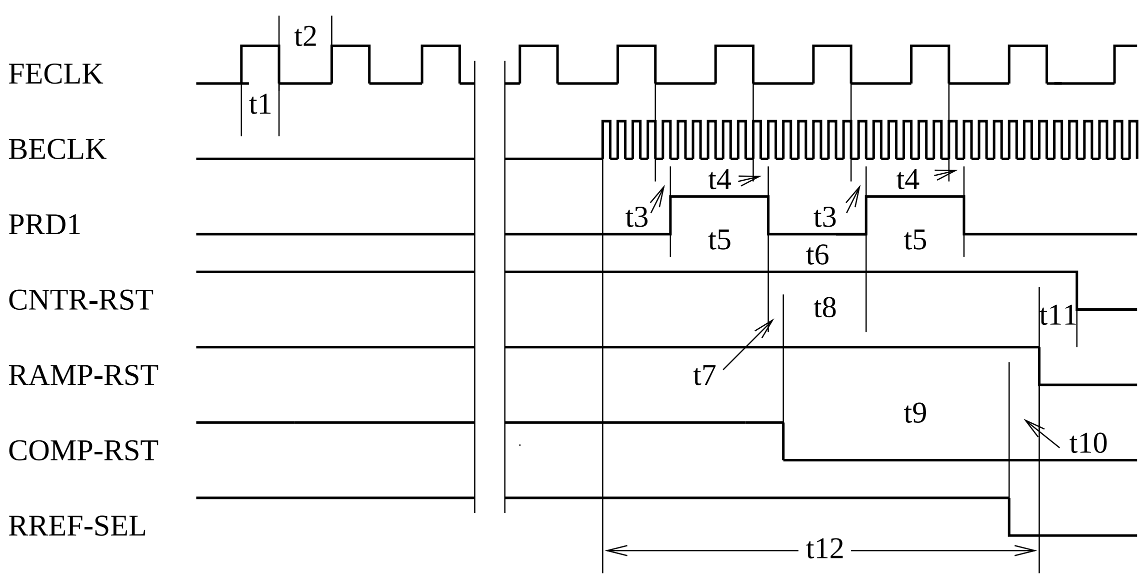


Figure 2.18: Start of Digitization **Does not match XTL; check bus0-3**.

Digitization is begun by starting the back-end clock and sending two PRD1 pulses while in Acquire mode. Acquization will continue while the digitization sequence takes place as long as there is room for a trigger in the pipeline pointer logic.

The signals for starting digitization and the setup of the ADC are shown in the timing diagram of Figure 2.18).

The A/D setup period is near the left hand side of the figure. Immediately after the Digitize Mode is entered, RREF-SEL is lowered to add the offset voltage to the ramp output. Then RAMP-RST is lowered to begin the A/D ramp. After a short period of time **what is it?**, CNTR-RST is lowered to start the Gray Code counter.

In Figure 2.18 the delay between RAMP-RST low and CNTR-RST low (t11) is provided to allow the ramp generator output to reach its linear operating region before starting the counter. When the Gray Code counter reset is released, the Gray Code counter begins to count starting from zero. The counter increments on both the positive and negative edges of the counter clock. Thus a 53 MHz clock increments the counter at 106 MHz.

The end of digitization and start of readout is shown in Figure 2.19. Here the maximum programmed value for the counter is set arbitrarily at 60. After a few counts, BNBR is shown going low which indicates that channel 127 on the chip being examined is over threshold (has a hit) and is tagged for readout. Whenever a hit is detected, the internal logic of the chip determines whether adjacent channels should also be read out. If the READ NEIGHBORS bit was set high, the channel on either side of the hit channel is also tagged for readout. If the READ NEIGHBORS and READ ALL bits are set low then only the hit channels are tagged for readout. If the READ ALL bit is high, all channels are tagged for readout as soon as the counter reaches its programmed maximum value. Two counts after BNBR went low, TNBR is shown going low which indicates that channel 127 on the top neighbor chip is over threshold. TNBR going low means that if the READ NEIGHBORS bit is active on the chip being studied, then channel 0 of that chip is tagged for read out.

After 60 counts on the Gray Code counter, any digital latch which has not been previously been set is set to the maximum programmed value of 60. If the threshold for the chip is set to less than 60 counts, then the channels which were set to 60 are over threshold and they are also tagged for readout. The counter clock may continue to run but it has no further effect on the chip. Information (address and digital data) for all of the tagged channels is held on latches in the readout FIFO for further processing.

The time when the counter maximum value has been reached is known in SVX3D only from the clock speed and the maximum count programmed into the clock . After it is known that the counter has reached maximum, Readout Mode can be entered. This starts the compression of the tagged data (sparsifyng the address and digital data) stored on the latches in the FIFO. In a daisy chain configuration, information in all chips will collapse simultaneously. The time for the information to completely collapse is about 600 nsec in the SVX3D. The back-end clock is no longer needed while information is being compressed. However, the clock may continue to run as shown in Figure 2.19. While the information is collapsing, RREF-SEL is raised to reconnect RAMP-REF to the ramp generator input.

Considerations:

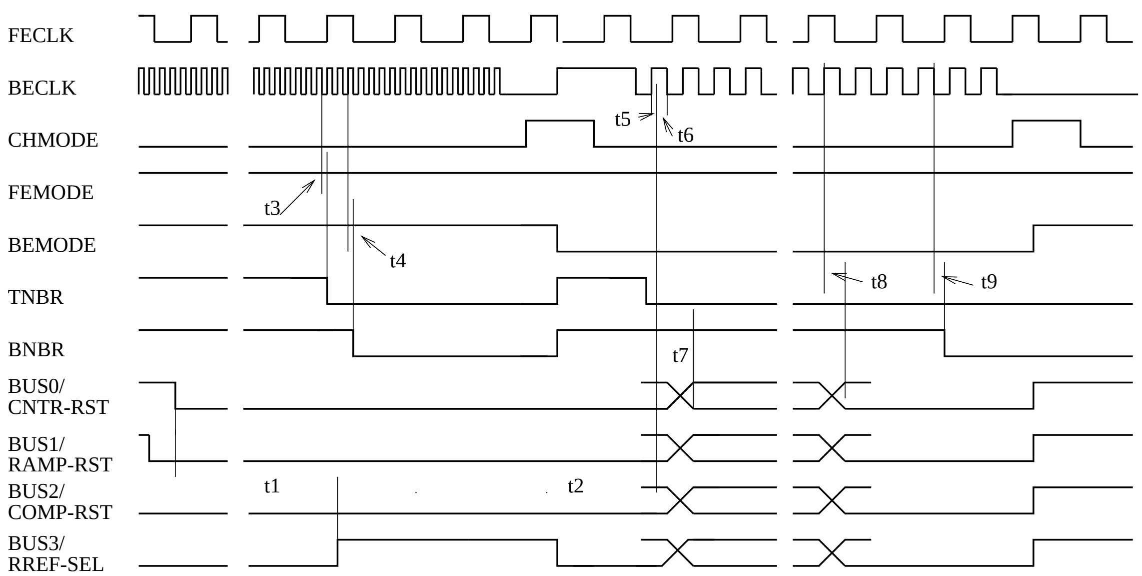


Figure 2.19: End of Digitization and start of readout. **Check Bus0-BUS3 behaviour.**

Parameters		Minimum	Maximum
FECLK width high	t1	25 ns	—
FECLK width low	t2	15 ns [2]	—
FECLK ↓ to PRD1 ↑	t3	???	—
FECLK ↓ to PRD1 ↓	t4	???	—
PRD1 pulse width	t5	???	—
PRD1 ↓ to PRD1 ↑	t6	???	—
PRD1 ↓ to COMP-RST ↓	t7	???	—
COMP-RST ↓ to PRD1 ↑	t8	???	—
PRD1 ↓ to RREF-SEL ↓	t9	???	—
RREF-SEL ↓ to RAMP-RST ↓	t10	300 ns[3]	—
RAMP-RST ↓ to CNTR-RST ↓	t11	0	—
Start of BECLK to RAMP-RST ↓	t12	1 BECLK	—

Table 2.6: Timing specifications for the start of digitization. **Are the footnotes there?**

- During the digitization cycle both TNBR and BNBR can act as inputs and outputs, therefore they should not be driven by external signals.
- Bus lines BUS0 – BUS3 are used as inputs to control the ADC.
- Bus lines BUS4 – BUS7 are tri-stated throughout the digitization cycle.
- The FEMODE and BEMODE lines are high.
- PRD1 and PRD2 have to be in phase with the FECLK.

this next paragraph may be out of place.

If the Counter CK and Counter CKB in the Digitize Mode are ever high at the same time, the counter clock oscillates creating noise on the chip. Under normal operating conditions Counter CK and Counter CKB should never be high at the same time. However upon power up, the internal latches for these clock signals are set in random states and even initialization does not clear them. Only after going through the digitization mode for the first time and leaving the digitize mode with the clock lines in the correct states can the latched Counter CK and the Counter CKB states be guaranteed to be correct. Thus any data from the first digitization cycle should be suspect.

2.3.6 Timing of Data Sparsification and Readout

After waiting for the digitization counter to max out, operation of the chip can be changed to the Readout Mode. The mode control lines are used to switch the SVX3D into a data readout mode. First, CHMODE is raised and while it is high, BEMODE is set equal to 1. At the same time, the data acquisition system connected to BUS0–BUS7 should be changed from a data transmit to a data receive condition in preparation for receiving digitized data from the SVX3D. When CHMODE is lowered, the internal SVX3D data lines are connected to the bus lines provided the chip has received a Priority Input signal. The TNBR line low indicates that the chip has received a priority input for control of the bus, and that data may be read out on alternate half cycles of a 50% duty cycle clock.

In Readout Mode, the TNBR pad is pulled low internally by a 15k resistor and the BNBR pad is pulled high internally before readout of the chip occurs. After readout, BNBR goes low.

Rick has changes relating to multiple chips in a chain...

Summary of actions:

1. The BEMODE line goes low to initiate readout. FEMODE is always high except during initialization.
2. Bus lines BUS0 – BUS7 present chip ID and channel numbers after the rising edge and status and data after the falling edge of BECLK.

When a high BNBR is connected to a low TNBR as occurs with daisy chained chips, the TNBR pad is pulled high (wire-or). Figure 2.20 shows how the priority bit is passed in a three chip daisy chain readout. Passing the priority between chips requires 1-2 nsec.

Parameters		Minimum	Maximum
CNTR-RST ↓ to RREF-SEL ↑	t1	maxcnt+3 beclk	—
RREF-SEL ↑ to TN↓	t2	550 ns[4]	—
BECLK edge to TN ↓	t3	3 ns[5]	—
BECLK edge to BN ↓	t4	3 ns[6]	—
BECLK ↑ to TN ↓	t5	5 ns[7]	—
TN↓ to BECLK ↓	t6	5 ns	—
TN↓ to Data	t7	5 ns	—
BECLK edge to Data	t8	15 ns	—
BECLK ↓ to BN↓	t9[8]	15 ns	—

Table 2.7: Timing specifications for the end of digitization and readout.

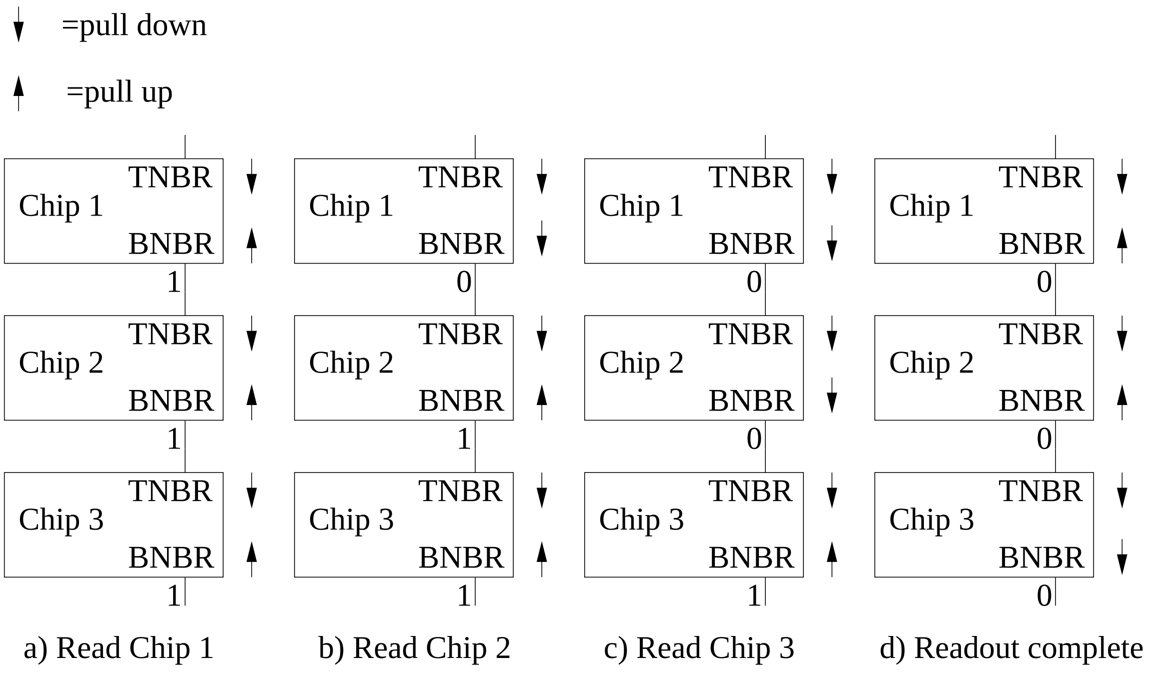


Figure 2.20: Passage of priority bit during readout.

Value	comment
Chip ID	high order bit always set also
Status = pipeline cell number	only lowest six bits ever set
Channel number	binary
Data	Gray code
Channel number	binary
Data	Gray code
... repeat channel number/data	as needed...
Channel number	binary
Data	Gray code

Table 2.8: Data readout according to setting of READ NEIGHBORS and READ ALL bits.

Figure 2.19 shows a timing diagram for readout of a single chip. Since TNBR is pulled low internally, readout of a single chip could begin as soon as TNBR falls (T_C =15kΩ $\times C_{ext}$) after entering the Readout Mode. However in Figure 2.19, TNBR is externally held high to inhibit readout for a few clock cycles. (TNBR high holds the data bus in a tri-state condition.)

2.3.7 Output Data Format and OBDV

The data format is shown in Table 2.8 and Figure 2.21. Accompanying the data is the synchronous strobing of the OBDV output signal for every other byte of data: the odd byte data valid signal. The first rising edge of OBDV can be used to latch the Chip ID, the first falling edge can be used to latch the cell number. Subsequent rising and falling edges can then be used to latch the channel IDs and data bytes respectively. The channel numbers are normal binary code and the data are Gray Code. When all of the desired information is readout from the chip, the Priority Out signal on BNBR goes low. If the clock continues to run after all data is read out, the output data bus once again enters a tri-state condition. If a chip receives a priority input and there is no digital data in that chip for readout, the 16 bits for chip ID and status are read out in one low/high cycle of the clock and then priority is passed to the following chip. For clarification, a typical output bus data pattern for daisy chained chips is shown in Figure 2.21.

2.3.8 Timing of FE integrator reset

The integrator needs to be regularly reset to prevent it from saturating. The best time to reset the integrator is during a major beam gap. During a beam gap, the pipeline clock (FECLK) must keep running to permit possible data readout from earlier interactions. To reset the integrator completely, PARST must be raised for at least 400 nsec. **Is this correct time?** When PARST is lowered, charge is injected into the integrator. The integrator should be allowed to settle for **how long?** before valid data is taken.

PARST minimum pulse width is about 400ns, depending on ISEL bits, to reset the integrator com-

BUS0	1	X	X	X	X	X	X	X	0	X	1	X	X	X	X	X	0	X	X	X	1	X	1	X
BUS1	0	X	X	X	X	X	X	X	1	X	1	X	X	X	X	X	0	X	X	X	0	X	1	X
BUS2	0	X	X	X	X	X	X	X	0	X	0	X	X	X	X	X	1	X	X	X	1	X	1	X
BUS3	0	X	X	X	X	X	X	X	0	X	0	X	X	X	X	X	0	X	X	X	0	X	0	X
BUS4	0	X	X	X	X	X	X	X	0	X	0	X	X	X	X	X	0	X	X	X	0	X	0	X
BUS5	0	X	X	X	X	X	X	X	0	X	0	X	X	X	X	X	0	X	X	X	0	X	0	X
BUS6	0	0	X	X	X	X	X	X	0	0	0	0	X	X	X	X	0	0	X	X	0	0	0	0
BUS7	1	0	0	X	0	X	0	X	1	0	1	0	0	X	0	X	1	0	0	X	1	0	1	0
BECLK	0	1	0	1	0	1	0		0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	Chip ID	Cell No.	Address	Data	Address	Data	Address	Data	Chip ID	Cell No.	Chip ID	Cell No.	Address	Data	Address	Data	Chip ID	Cell No.	Address	Data	Chip ID	Cell No.	Chip ID	Cell No.

Figure 2.21: Typical output bus data for several chips. In this example threshold suppression is assumed to be active and the nearest neighbors are to be read out. The first chip has therefore three strips read. The second has no strips about threshold and so only the Chip ID and Cell number are returned. The next chip has two strips at the end of the chip where the last is above threshold. Hence one strip is read out on the following chip due to the neighbor logic action. The last two chips have no data.

pletely. Data taken during reset and within 1 μs after reset is not valid. **- how long?**

2.3.9 Timing of Reference Pipeline Reset PRD2

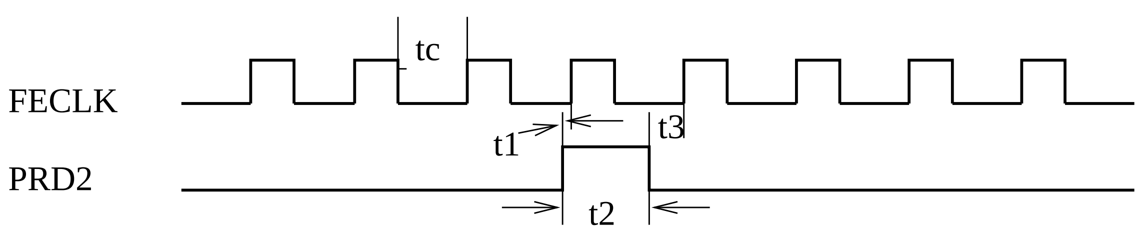


Figure 2.22: Reference Pipeline Reset.

- The reference pipeline reset must occur each time after the digitization is completed. Also, if the time between digitizations is large **quantifiy!** additonal resets are required.
- While PRD2 is high, the write amplifier is connected to the reference cell so no data can be acquired but the pipeline cell pointer is still advanced.

Parameters		Minimum	Maximum
PRD2 $\uparrow$ to FECLK $\uparrow$	t1	5 ns	tc - 5 ns
PRD2 pulse width	t2	???	
PRD2 $\downarrow$ to FECLK $\downarrow$	t3	5	tc - 5 ns

Table 2.9: Timing specifications for the reference pipeline reset.

- Because of this, the PRD2 should occur at a time when no data is present at the chip input. Also, the PRD2 should not occuring during PARST.
- The pipeline cell, which has been digitized, is put back into the cell at the first clock after the falling edge of PRD2.

2.3.10 Timing of Re-synchronization of pipeline cell

Re-synchronization of pipelines means resetting the cell counters so all the pipelines point at the first cell number. A full initialization cycle will resynchronize the pipelines. In addition, dropping the FEMODE line and toggling the CALSR line without toggling the FECLK also resets the pipeline cell pointer.

2.3.11 Timing of Abort readout cycle

If necessary the readout cycle can be aborted before all devices in a daisy-chain are read out by switching out of Readout Mode. **- what exactly do you do?**

2.4 Floorplan and Pinout

Figure 2.23 shows a simplified floorplan of the SVX3D chip. Starting from the left, the integrator section is followed by the analog pipeline section and the A/D section. Following the A/D is the Neighbor and Latch section which feeds the asynchronous FIFO section. Address and data information is passed from the FIFO to the bidirectional I/O pads for readout from the chip.

The SVX3D chip measures 6.3×11.9 mm. This is more than twice the size of the SVXI radiation hard device. There are approximately 100,000 transistors on the SVX3D.

Figure 2.24 shows the location of most of the pads on the SVX3D chip. The inputs from the 128 silicon strip channels are at the top of the figure. They are placed in a double row with an effective pitch of 48 microns. (Table 2.10

The pads on the other sides of Figure 2.24 have a variety of functions as described in Table 2.12 and Table 2.11. The BNBR (bottom neighbor) pad on the left side and the TNBR (top neighbor) pad on the right hand side are used to communicate between adjacent chips and to download the initialization

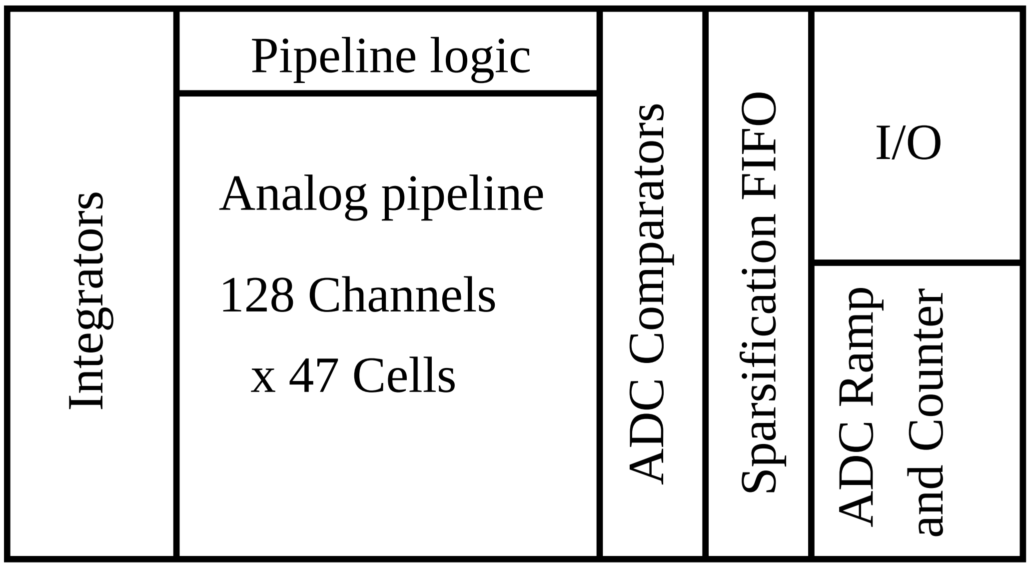


Figure 2.23: Physical layout of SVX3D chip.

bitstream as described elsewhere in this chapter and in Chapter 3. The pads PARST, PRD1, PRD2, L1A, and CALSR are located on the right hand side along the bottom edge in the figure. They control aspects of the Front End. The next three pads on this side, FEMODE, BEMODE, and CHMODE, are used to determine the states of the front and back ends. The next four pads in this area are the differential clocks, FECLK and BECLK. Continuing along this side, eight sets of differential signal pads, BUS0–BUS7, are used to output address and data information from the SVX3D during the Readout Mode. Pads BUS0–BUS3 are also used for real time control of internal switches during digitize mode. The pads with multiple functions are described in more detail in Section 2.4.1.

The remaining pads on the chip carry DC voltages, set bias levels within the chip or provide test points. For some of the biasing, an autobias circuit is used to set current levels for the internal components, but the internal values can be overridden using the pads, which are normally left unconnected.

What was the following supposed to communicate? The pads on the I/O side of the chip are in a single row with a 200 micron pitch. What is the I/O side? What does numbering starting in the lower right hand corner and moving counterclockwise really mean?

How are the pins really numbered. could someone really find the pins given the information in this section?

2.4.1 Pads with Multiple Functions

The SVX3D has 8 pads which change function depending on the cycle. Table 2.4.1 summarizes the signals on the multifunctional and clock pads in the different operating states.

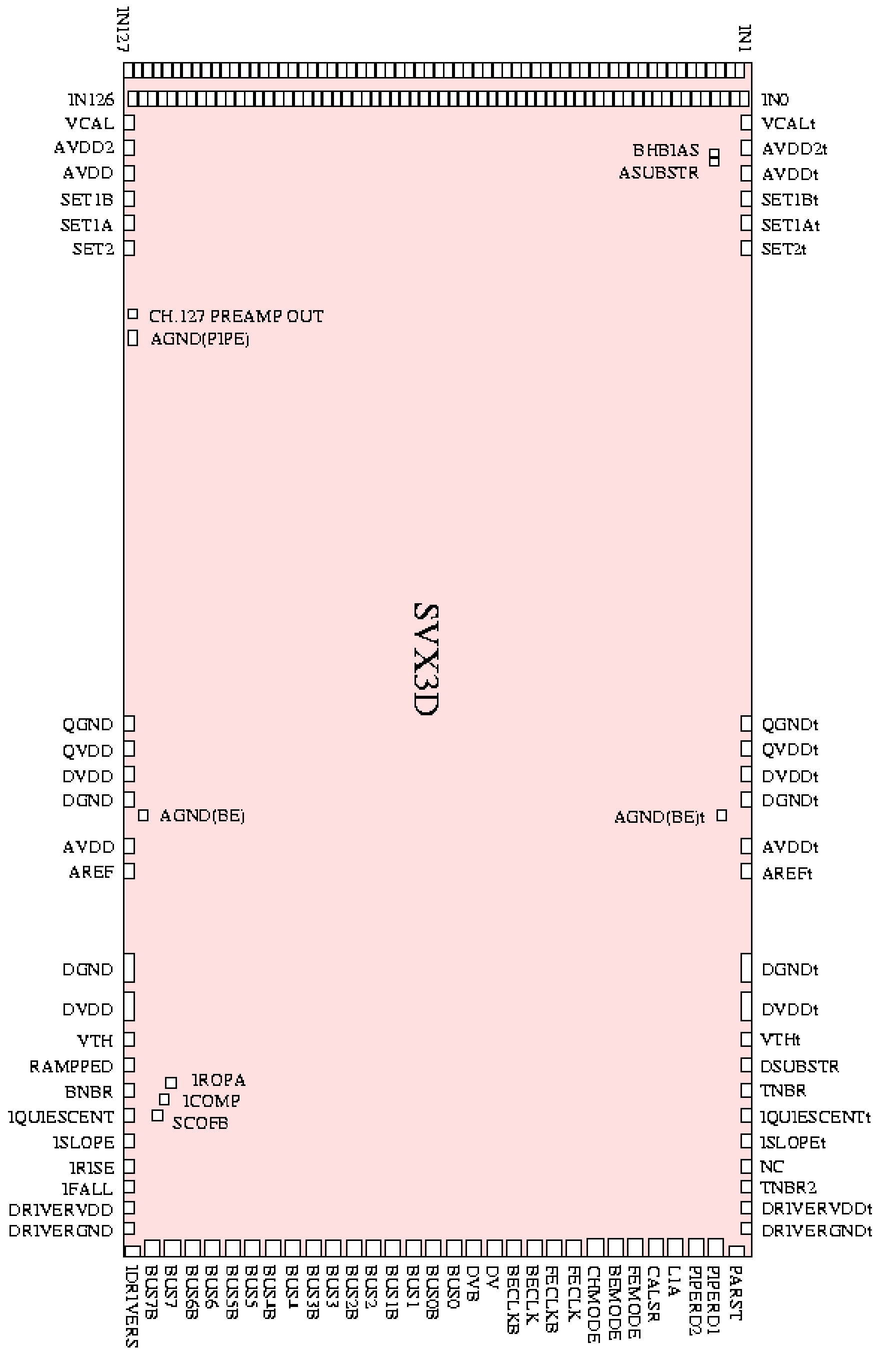


Figure 2.24: SVX3D footprint. Doesn't show all the signals that are listed in Table 2.11

Pin Name	Pin No.	Pin Function
ANALOG127	A127	Analog input channel #127
....	....	channel #126–channel #1
ANALOG0	A0	Analog input channel #0

Table 2.10: Description of signals going into the SVX3D chip at the top of Figure 2.24.

The clock signals on pads FECLK and BECLK are different for the four states. Thus, an intelligent clock (one that changes frequency and duty cycle) is required to control the SVX3D. The differential input clock uses PECL logic levels (1=+3.0V, 0=+2.2V). In the Initialize state, the FECLK runs with a 50% duty cycle and is used to clock chip parameters and test hit patterns into the SVX3D serial shift register. During the Acquire state, the FECLK is directed internally to the analog pipeline. The FECLK line must have an accurately controlled non-50% duty cycle since the time the clock is high corresponds to the pipeline capacitor reset and the time the clock is low corresponds to the integration time of the signal. **Is this correct?** In the Digitize state, the BECLK line is run with a 50% duty cycle and is used to increment the Gray Code counter in the A/D converter. In the Readout state, the BECLK is also run at a 50% duty cycle and is used to read data out from the SVX3D chip onto the data bus. In principle, the BECLK could be run at the same frequency for all the operating states. However, for optimal performance, the clock frequency is different for the various states.

Four of the pads, BUS0–BUS3, are used together with BUS4–BUS7 for parallel data readout and also for independent real time control of internal switches during digitization. Table 2.4.1 details the meaning or level of BUS0–BUS3 for the various states.

The other two pads TNBR (top neighbor) and BNBR (bottom neighbor) are used for communicating between adjacent chips or the control system and provide three very different functions.

During the Initialize state, the TNBR acts as an input for serial data (parameters) to be loaded into the SVX3D. BNBR acts as an output for serial data passing through the chip to the next adjacent chip or acts as a monitor for checking data which was previously loaded into the chip(s). The TNBR and BNBR pads have no function for acquisition.

During the Digitization cycle, the BNBR pad passes neighbor hit information back and forth between the bottom neighbor chip and the TNBR pad performs the same function with the top neighbor chip. When the last channel on the chip exceeds the digitally set threshold, BNBR undergoes a high to low transition, signalling the next chip that its first strip should be read out. Similarly, when the first strip on a chip exceeds the digital threshold, the TNBR undergoes a high to low transition indicating to the preceeding chip that its last channel should be read out. The transition occurs as soon as the channel's Gray code counter exceeds threshold; therefore, lower thresholds cause the high to low transition sooner than high thresholds.

In the Readout cycle, several chips share the same data bus and priority bit is passed between chips to acknowledge which chip has access to the bus. In the Readout cycle, the TNBR pad acts as a priority input pad from a previous chip or the control system and BNBR acts as a priority out signal to feed an adjacent chip. When TNBR falls, the readout starts and when the last channel is read out, BNBR falls. Since BNBR is TNBR for the next chip, readout begins for that chip.

Pin Name	Pin No.	In/Out	Signal Type	Pin Function
VCAL	B1		ANALOG	Calibration voltage
AVDD2	B2		ANALOG	Integrator supply voltage
AVDD	B3		ANALOG	Analog supply voltage
SET1A	B4		ANALOG	
SET1B	B5		ANALOG	
SET2	B6		ANALOG	
QGND	B7		ANALOG	Pipeline analog ground
QVDD	B8		ANALOG	Pipeline analog voltage
DVDD	B9		ANALOG	Pipeline digital voltage
DGND	B10		ANALOG	Pipeline digital ground
AVDD	F1		ANALOG	Quiet Digital Supply Voltage
AREF	F2		ANALOG	Analog reference voltage (AVDD)
DGND	F3		ANALOG	Digital Ground
DVDD	F4		ANALOG	Digital Supply Voltage
VCMTH	F5		ANALOG	Common mode threshold voltage
DSUBSTR	F6T		ANALOG	Digital substrate(connect to digital ground)
RAMPPED	F6B		ANALOG	External ramp pedestal override
TNBR	F7T	I/O	CMOS	INIT mode: shift register in;
				DIGI mode: ch. 0 neighbor logic;
				READOUT mode: priority in
BNBR	F7B	I/O	CMOS	INIT mode: shift register out;
				DIGI: ch. 127 neighbor logic;
				READOUT: priority out
$I_{quiescent}$	F8		ANALOG	Bias for comparator via Resistor to GND
I_{slope}	F9		ANALOG	Comparator ramp rate adjust - A/D gain adjust
NC	F10T		none	not connected
IRISE	F10B		ANALOG	Test point for current mode of output bus drivers
TNBR	F11T		CMOS	Redundant pad to TNBR above
IFALL	F11B		ANALOG	Test point for current mode of output bus drivers
SVDD	F12		ANALOG	Driver digital supply voltage
SGND	F13		ANALOG	Driver digital ground
SCOFB	TP1			
ICOMP	TP2			
IROPA	TP3			
CRSTI	TP4			
CRSTO	TP5			
THBUS	TP6			
THCO	TP7			
VLATCH	TP8			
VRAMP	TP9			Ramp voltage
NIP	TP10			
VCOMP	TP11			Comparator voltage

Table 2.11: Description of signals going into and out of SVX3D chip on the sides of Figure 2.24. Analog ground, AGND is supplied through the substrate only, not via pads. Pads TP1-TP11 are testpoints. **with tom's changes. Where are TP1-11? How can these be the pin numbers? Only a few are shown in the interior of the figure.**

Pin Name	Pin No.	In/Out	Signal Type	Pin Function
PARST	1	IN	CMOS	Integrator reset - active high
PRD1	2	IN	CMOS	Causes analog voltage transfer from pipeline
PRD2	3	IN	CMOS	Restore cell and Reset pipeline reference cell
L1A	4	IN	CMOS	Level 1 Accept trigger - select pipeline cell for read
CALSR	5	IN	CMOS	INIT: strobe serial data; ACQ: calibration pulse
FEMODE	6	IN	CMOS	Front End Mode control line (0=INIT)
BEMODE	7	IN	CMOS	Back End Mode control line (0=READOUT)
CHMODE	8	IN	CMOS	Change Mode - latch mode control signals
FECLK	9	IN	CDIF	INIT: serial register shift clock; ACQ: pipeline advance clock
$\overline{\text{FECLK}}$	10	IN	CDIF	"
BECLK	11	IN	CDIF	DIGI: ADC counter advance clock; READOUT: data clock
$\overline{\text{BECLK}}$	12	IN	CDIF	"
OBDV	13	OUT	CDIF	Odd byte data valid
$\overline{\text{OBDV}}$	14	OUT	CDIF	"
BUS0	15	I/O	CDIF	DIGI: Comparator Reset; READOUT: Data Bus D0
$\overline{\text{BUS0}}$	16	I/O	CDIF	"
BUS1	17	I/O	CDIF	DIGI: Ramp Reset; READOUT: Data Bus D1
$\overline{\text{BUS1}}$	18	I/O	CDIF	"
BUS2	19	I/O	CDIF	DIGI: Counter Reset; READOUT: Data Bus D2
$\overline{\text{BUS2}}$	20	I/O	CDIF	"
BUS3	21	I/O	CDIF	DIGI: Ramp Reference Select; READOUT: Data Bus D3
$\overline{\text{BUS3}}$	22	I/O	CDIF	"
BUS4	23	OUT	CDIF	Data Bus D4 (Readout)
$\overline{\text{BUS4}}$	24	OUT	CDIF	"
BUS5	25	OUT	CDIF	Data Bus D5
$\overline{\text{BUS5}}$	26	OUT	CDIF	"
BUS6	27	OUT	CDIF	Data Bus D6
$\overline{\text{BUS6}}$	28	OUT	CDIF	"
BUS7	29	OUT	CDIF	Data Bus D7
$\overline{\text{BUS7}}$	30	OUT	CDIF	"
$I_{drivers}$	???		ANALOG	Output current adjust for current mode drivers via via Resistor to GND. Connect to +5V to disable.

Table 2.12: Description of signals going into/out of SVX3D chip at the bottom of Figure 2.24.

Pad Name	Initialize	Acquire	Digitize	Readout
FECLK	Shift register clock	clock pipeline	clock pipeline	clock pipeline
BECLK	not used	not used	ramp clock	readout clock
BUS0	not used	not used	COMP-RST	DOUT0
BUS1	not used	not used	RAMP-RST	DOUT1
BUS2	not used	not used	CNTR-RST	DOUT2
BUS3	not used	not used	RREF-SEL	DOUT3
TNBR	Serial data in	not used	TOP HIT	PRIORITY IN
BNBR	Serial data out	not used	BOTTOM HIT	PRIORITY OUT

Table 2.13: SVX3D pad functions versus state. The acquire state affects only the front end. The digitize and readout states only affect the backend. Initialization affects both front and back ends.

Pad name	Signal name	Signal function
BUS0	COMP-RST	A/D analog comparator reset (1=reset)
		Also does pedestal subtraction
BUS1	RAMP-RST	A/D ramp reset (1=reset)
BUS2	CNTR-RST	A/D Gray code counter reset (1=reset)
BUS3	RREF-SEL	Selects RAMP-REF(1) or RAMP-PED(0) for double-sampling
		lowering RREF-SEL adds offset to the ramp output

Table 2.14: Description of the BUS lines that are used for digitization control.

Chapter 3

Initialization Bit Stream

The bits for initialzation are summarized in Table 3.1 and described in this section. Bits are to be loaded in the following order: 128 bits of CHANNEL MASK (channel #127 first), followed by 22 bits of control for the Front End, followed by 46 bits of control for the Back End (bit #152 shifted in first); control bits are latched into registers by the CALSR signal. The values used currently in a variety of test stands can be found in Chapter A. Be careful with the signal polarity bits - the software for most teststnds and the CDF DAQ do not allow individual control, but has pre-set combinations of these bits. (Note that Appendix C is a Gray code decoding table.)

3.1 Shift Register Bit functions and descriptions

3.1.1 Bit Descriptions

1. **CHANNEL MASK (**1– 128**):** There is one bit per channel. If the bit is set, the charge injection circuity is enabled for that channel. Note that these load in reverse order, i.e. channel 127 loads first and channel 0 last.

2. **CAL DIRECTION(**129**):** The charge injection pulse is generated by switching between two voltage levels: the external VCAL level(Table 2.11), and 2.5V, which is generated internally. This voltage difference is applied to the test input capacitor. (Figure 2.2). The order of the switching is determined by this bit, which in turn determines the polarity of the injected charge. If CAL DIRECTION = 0, the voltage switches from VCAL to 2.5V when the CALSR control signal goes from low to high. If CAL DIRECTION = 1, the voltage switches from 2.5V to VCAL. By using this bit, the polarity of the injected signal can be changed without having to change the VCAL voltage level. See additional information in Section 3.2 below.

3. **FE POLARITY (**130**):** This bit affects the DC reset points of the input integrator and the pipeline, in order to maximize their dynamic range for a given polarity. Use 0 for positive input signal and 1 for a negative signal.

Front-End Bits		
BITS	0=switch from VCAL to 2.5V	
130	FE POLARITY	0=pos. input current, 1=neg.
131-133	BANDWIDTH [0 : 2]	LSB: 131
134-139	PIPELINE DEPTH [0 : 5]	LSB: 134
140-150	ISEL [1 : 11]	Bias adjust bits
151	READOUT ORDER	0=pedestal first, 1=signal first
Back-End Bits		
152-158	CHIP ID [0 : 6]	LSB: 152
159	DYNAMIC THRESHOLD ENABLE	0=disable, 1=enable
160	IQUIESCENT BIAS RATIO SELECT	0=low, 1-high
161	DRIVER BIAS CMODE SELECT	0=2.5V, 1=1.7V
162	LAST CHIP	1=last chip
163	READ NEIGHBORS	1=read neighbors
164	READ ALL	0=sparse readout, 1=read all
165	ADC RAMP DIRECTION	0=ramp down, 1=ramp up
166	ADC COMPARATOR DIRECTION	0=ramp down, 1=ramp up
167-174	RAMP SLOPE TRIM [7 : 0]	MSB:167
175-182	THRESHOLD [0 : 7]	MSB:175(Gray Coded)
183-190	COUNTER MODULO [7 : 0]	MSB:183(Gray Coded)
191-193	DRIVER RESISTOR SELECT	0=disable (LSB: 193)
194-197	ADC RAMP PEDESTAL	LSB:194

Table 3.1: Summary table of front and back end initialization bits

4. **BANDWIDTH (**131–133**):** These three bits provide a binary code to set the integrator bandwidth. The actual bandwidth or rise time is affected by integrator bias, input capacitance, and the setting of the these bits. These bits can be used to set the rise time to a value appropriate for 132ns or 396ns crossing time for an input capacitance range of 10-30pF. See Chapter 4.

5. **PIPELINE DEPTH (**134–139**):** This six bit binary word sets the delay in number of buckets (actually number of FECLKś) from signal arrival at a pipeline cell to L1A removing that cell from the normal pipeline process. Valid settings are 1-42. A setting of zero has no meaning.

6. **ISEL 1-11(**140–150**):** These bits control the bias current levels for the input integrator (ISEL1-ISEL4), integrator reset (ISEL5-ISEL6), pipeline read amplifer(ISEL7-ISEL9) and pipeline write amplifier (ISEL10-ISEL11). The following bias levels assume that SET1A, SET1B, and SET2 bias current pads are connected in parallel to a 13K resistor to ground, thus applying 280 μA.

   ISEL1, ISEL2 and ISEL3 supply bias current to the NMOS input transistor only, whereas ISEL4 bias current flows through the cascode section also. Ignore, i.e. don't set, ISEL4. It really shouldn't be there but was too much trouble to take out.

   The recommended ISEL 1-11 settings for normal operation are (ISEL1)10101010010(ISEL11). (See Section A.)

   (a) **Integrator NMOS bias current,**
   $=35\ \mu\text{A} + \text{ISEL1} \times 35\mu\text{A} + \text{ISEL2}\times 70\mu\text{A} + \text{ISEL3} \times 140\mu\text{A} + \text{ISEL4}\times 70\mu\text{A}$
   This affects noise and bandwidth. ISEL(4) = 0

   (b) **Integrator cascode current**
   $=35\ \mu\text{A} + \text{ISEL4} \times 70\ \mu\text{A}$
   Determines the time required to reset the integrator. A fast time is desireable, but can cause things to oscillate. ISEL4=0

   (c) **Integrator reset bias**
   $=0.65\ \mu\text{A} + \text{ISEL5} \times 0.65\ \mu\text{A} + \text{ISEL6} \times 1.6\ \mu\text{A}$
   For nominal reset bias, ISEL5=1, ISEL6=0.

   (d) **Pipeline write amplifier bias**
   $=70\ \mu\text{A} + \text{ISEL7} \times 17\ \mu\text{A} + \text{ISEL8} \times 35\ \mu\text{A} + \text{ISEL9} \times 70\ \mu\text{A}$
   Affects the amplifer rise time. To minimize power disipation, set to minimum value that gives the required speed.

   (e) **Pipeline read amp bias**
   $=17\ \mu\text{A} + \text{ISEL10} \times 17\ \mu\text{A} + \text{ISEL11} \times 35\ \mu\text{A}$
   Affects the amplifer rise time. To minimize power disipation, set to minimum value that gives the required speed.

7. **READOUT ORDER (**151**):** When digitizing, the pipeline sequentially reads out two levels, signal and pedestal (cell number 47 of the pipeline). The ADC digitizes the difference between them. Reversing the order of readout effectively reverses the signal polarity seen by the ADC. Thus, if desired, the ADC can be run in one polarity only, and polarity reversals are handled by the Readout order bit.

8. **CHIP ID (152-158):** Each chip in a daisy chain can be given a unique chip id.

9. **DYNAMIC THRESHOLD ENABLE (159):** If this bit is set, an automatic pedestal subraction is made to the digitized data. See Chapter 2.

10. **IQUIESCENT BIAS RATIO SELECT (160):** This affects the bias current of the ADC comparators, and the ramp op-amp. The high bias option increases the bias current to these sections by about a factor of three. Based on test results, low bias seems to be adequate.

11. **DRIVER BIAS CMODE SELECT (161):** The chip has two output drivers for the differential data lines, a resistor driver and a current mode driver. The current mode driver is disabled by tying the $I_{drivers}$ pin to +5V and enabled by tying the $I_{drivers}$ pin to ground though a resistor whose value determines the current. **algoritm - - we were us9ing 35k** See Table 2.12. The bit is intended to set common mode voltage for the current driver terminated with a resistor across the differential output as is done on SVX3 port card for CDF. If this bit = 0, the common mode voltage should be +2.5 V, if it = 0, +1.7 V. Tests show that common mode voltage with the simple resistor termination can vary significantly during a single read out and that the expected common mode voltage may not be what is actually seen.

    The resister mode output driver is controlled using bits 191–193 as described below.

12. **LAST CHIP (162):** Set to indicate this is the last chip in the daisy chain.

13. **READ NEIGHBORS (163):** When this bit is enabled, the nearest neighbor on either side is read if a channel is above digital threshold. If the channel is the last on the chip, then the BNBR line makes a high-low transition indicating that the next chip's first channel should be read. This BNBR transition occurs as soon as the digitized channel value crosses the digital threshold. Similarly, if the channel is the first on the chip, TNBR undergoes a high–low transition as soon as the digitized value exceeds the digital threshold. This tells the preceeding chip to include the last channel in readout.

14. **READ ALL (164):** When set, causes all channels to be read independent of the threshold. However, the TNBR and BNBR lines behave as though the threshold were set.

15. **ADC RAMP DIRECTION and ADC COMPARATOR DIRECTION (165& 166)** Refer to Chapter 2 on the operation of the ADC. The ADC consists of comparator, a counter and a ramp generator whose output is determined by its initial value and the sign and magnitude of its slope, The ramp and the counter are started and, as the ramp signal ramps up, it is compared to the signal being digitized with a comparator. When the two agree, the value of the counter is saved as the digitized value. ADC RAMP DIRECTION determines the direction, up or down, of the ramp. 0 gives a falling ramp, i.e. from higher voltage to a lower one. ADC COMPARATOR DIRECTION determines which direction the comparator fires in, i.e. as the ramp signal approaches from above or below. 0 means ramp approaches signal from above. These two bits should always be set to the same value, and are used to change the ADC polarity. If the Readout order bit is set to 0(see above), then a positive input current (FE polarity = 0) will produce a signal which is positive with respect to the pedestal at the pipeline output. Under

these conditions, the Ramp direction and Comparator direction bits should be set to 1. If the Readout order bit is set to 1, the Ramp and Comp bits should be set to 0.

The initial value of the ramp is set by ADC RAMP DIRECTION and ADC RAMP PEDESTAL as described below and in Section 2.2.2,

The slope is determined by the value of RAMP SLOPE TRIM and the external ramp rate resistor that is attached to VRAMP. **- wrong name?**

Note that there are external pads which can be used to modify or bypass ADC RAMP PEDESTAL and the internal ramp reference voltage. (these pads are only used in the B version since internal biasing was incorrect in that version of the chip.)

16. **RAMP SLOPE TRIM (**167–174**):** This is an 8-bit word that can be used to tweak the value of the ramp rate capacitor, i.e. the value of the slope of the ADC ramp. This is intended as a fine tune to equalize the ADC gain between chips if needed. The tweak range is about 20% of the total capacitance. All 1's gives the maximum ramp capacitance, or slowest ramp rate.

17. **THRESHOLD (**175–182**):** Gray coded digital threshold for sparsification.

18. **COUNTER MODULO (**183–190**):** Gray coded maximum value for digitization, i.e. how high the ADC counter is allowed to count. This can be used to limit the effective dynamic range of the ADC.

19. **DRIVER RESISTOR SELECT (**191–193**):** These bits set the output driver resistors. Each of the three select bits switches in a set of driver resistors. Any or all can be switched in. Setting the MSB to 1 results in a driving current of about 6.3mA, the middle bit adds about 3.3mA and the LSB about 1.7mA. The proper value of the driver resistance depends on the value of the line termination and differential voltage required. Of course, if the the current mode driver has been enabled, the values seen will be different. Conversely, the settings of these bits will affect operation when the current mode driver is enabled.

20. **ADC RAMP PEDESTAL (**194–197**):** This is a four bit binary code, which gives 16 different values for the offset of the ramp starting point from the ramp reference voltage. See Figure 2.7 and accompanying description in Section 2.2.2. The ramp reference voltage is an internally generated voltage. Table 3.2 contains a list of pedestal offset voltages corresponding to the ADC RAMP PEDESTAL settings. Normally, pedestal values of 5-15 would be selected with a falling ramp, since these produce a ramp offset in the opposite direction of the signal, defined as a "positive" pedestal offset, since the apparent pedestal of the signal is increased. Values of 0-3 give a ramp offset in the same direction as the signal: "negative" pedestal offset. ADC RAMP PEDESTAL affects the pedestal value of the signal which is read out. **is this consistent with discussion in chapter 2?**

Ramp Pedestal Setting	Pedestal Offset Voltage (mV)
0	-225
1	-169
2	-112
3	-56
4	0
5	$+56$
6	$+60$
7	$+65$
8	$+69$
9	$+73$
10	$+77$
11	$+82$
12	$+86$
13	$+142$
14	$+199$
15	$+255$

Table 3.2: Pedestal offset voltages set by bits 194-197.

3.2 Using Charge Injection for Testing and Calibration - Polarity bits and Cal Inject

As shown in Figure 2.11, charge can be injected into the SVX3D pre-amplifer for testing and calibration. This section describes how the amount and direction of this charge is determined by means of the polarity bits and the calibration voltage. Note that not all combinations of bits are commonly used. For example, the falling edge of CALSR is not used for calibration ramps in any of the usual test systems and we do not consider that case here.

The first bit to consider is the CAL DIRECTION [1]. This bit determines the presentation order of two voltages on the test capacitor during a CALSR signal. These voltages are an internally generated 2.5V, and the externally provided VCAL voltage. Since an external voltage that is greater than or less than 2.5V can be provided, there are four scenarios as indicated in Figure 2.11.

The choice of VCAL voltage and CAL DIRECTION determines whether voltage will be flowing into or out of the preamp, and will determine the proper setting for some of the other bits when charge injection is being used. If the CAL DIRECTION bit is set incorrectly, the best to hope for is an inverted output, i.e. a slowly increasing signal will yield a slowly decreasing output. Using the falling edge of the CALSR signal effectively reverses the meaning of this bit. This mode of operation is not recommended: it is prefereable to use the rising edge of cal strobe and let it fall a microsecond or so later.

[1] This bit has changed meaning since the SVXII chip, so the original Beginner's Guide is misleading

scenario	CALSR	CAL DIRECTION	current direction
A	< 2.5V	0 (VCAL first)	into preamp
B	< 2.5V	1 (2.5V first)	out of preamp
C	> 2.5V	0 (VCAL first)	out of preamp
D	> 2.5V	1 (2.5V first)	into preamp

Table 3.3: Direction of current for various scenarios.

The correct behavior of the chip now depends on the setting of the FE POLARITY, READOUT ORDER, ADC RAMP DIRECTION and ADC COMPARATOR DIRECTION bits. First the FE POLARITYbit must be set. This adjusts the operating point of the integrator and the pipeline in order to maximize dynamic range for the input signal. If there is current flowing into the integrator, it should be set to 0. In this case the integrator gives a negative signal (it goes from high to low). If the current is flowing out of the integrator, the FE POLARITYshould be set to 1 and the integrator output is positive. If the FE POLARITY bit is set incorrectly, this can result in insufficient dynamic range. This may or may not be an easy thing to diagnose. (Note that The operating point of the pipeline has been measured to be about 0.9V for FE POLARITY=0 and 1.8V for FE POLARITY=1 on an SVX3B chip. This may seems reversed because the output of the integrator is inverted with respect to the input signal.)

Next there is freedom to choose a desired read order out of the front end chip. This is determined by the the READOUT ORDER(also known as pipe polarity or pipe read order bit, aka PB.) If it is set to 0, the pedestal is presented first; conversely, if it is set to 1, the signal is presented first. The presentation order makes a difference because the first is always subtracted from the second. For the next paragraph, “signal” will now be used to mean the result of this subtraction.

Based on the previous two bits, there are four scenarios giving either a positive or a negative signal to digitize. The ADC RAMP DIRECTIONand ADC COMPARATOR DIRECTIONpolarity bits are set based on that signal. They are always equal, so it is only necessary to discuss the ADC RAMP DIRECTIONbit. Setting the ADC RAMP DIRECTION bit to 0 gives a ramp that starts at about 3V and falls. This ramp would be used for a negative signal. Setting the ADC RAMP DIRECTION to 1 gives a ramp that starts at about 2V and rises. This ramp is for positive signals. The ramp has a maximum range of about 1.5V if everything is set correctly. If the chip is run with a slow ramp using a 90kohm ramp rate resistor (typically what is used on SVX3D testcards), the ramp will only move about 0.5V during a standard 8-bit digitize sequence. If the ADC RAMP DIRECTION and ADC COMPARATOR DIRECTION bits are set incorrectly, at best one obtains an inverted signal that quickly runs out of range; it is possible that no signal is obtained because the comparators do not fire.

A summary of the valid combinations of the five polarity bits are given in Table 3.4.

Note that if the conventions specified in section 2.2.3 are followed, then the eight valid combinations collapse to just two, one for each detector side. These are given in table 2.3.

Combination	Scenario	CAL DIRECTION	FE POLARITY	READOUT ORDER	Ramp Dir	Comp Dir	comments
		bit 129	bit 130	bit 151	bit 165	bit 166	
1	A	0	0	0	1	1	sig>ped, + diff
2	A	0	0	1	0	0	sig>ped, − diff
3	C	0	1	0	0	0	sig<ped, − diff
4	C	0	1	1	1	1	sig<ped, + diff
5	D	1	0	0	1	1	sig>ped, + diff
6	D	1	0	1	0	0	sig>ped, − diff
7	B	1	1	0	0	0	sig<ped, − diff
8	B	1	1	1	1	1	sig<ped, + diff

Table 3.4: Valid bit combinations for calibration, polarity, ramps and read order.

Chapter 4

Considerations in Measuring the Performance of the SVX3

This chapter explores the subtleties of determining the bandwidth and choosing the best setting. It begins with a discussion of expectations of bandwidths, integration time, and setting the bandwidth. Effects of external capacitive load are examined and use of the calibration voltage and gain measurements to obtain a standard for presenting performance results follows. After this discussion there are warnings about testing with unloaded channels, a likely event when one is just looking at a chip on a hybrid, as well as robustness of the measurement including a word on common mode and control using differential noise measurements. A final word of warning on comparing the results to simulation concludes the section.

4.1 Expectations

It is common to present results on the performance of the readout electronics by presenting a plot of ENC (equivalent noise charge) versus capacitive load. Usuall this is a linear relationship; however, this is not guaranteed. In order to accomplish this, one must have an amplifier whose bandwidth is insensitive to the capacitive load. Usually, amplifiers are followed by shapers with a long shaping time compared to the amplifier rise time. Thus, the effect of capacitive load on rise time is negligible.

The SVX3D does not have a shaper and the load affects the bandwidth strongly. Therefore, a bandwidth setting has been provided: the rise time can be artificially slowed down for low capacitive load to allow for a constant bandwidth for all loads, and hence a linear result for ENC versus capacitance.

An example of direct measurements of the bandwidth of the amplifier in the SVX3C chip for 107ns integration time is give in Table 4.1. The result is linear because the bandwidth (inverse of rise time) remains constant as the load capacitance is changed. For this measurement the load capacitance is the external capacitance plus internal and stray capacitances. These latter two are about 3 pf. There is no measurement for the 0pF case. One would expect about 400e ENC, but the amplifier cannot be slowed sufficiently without external capacitance to observe this low noise.

Ext. Capacitance	BW Setting	0-90% Rise-time	ENC (e)
10 pF	4	70 ns	1070
20 pf	2	70 ns	1730
30 pf	1	65 ns	2460

Table 4.1: Equivalent noise charge for various capacitances and BW settings.

This measurement is only possible in test structures whereas most chip performance measurements need be done using the back end ADC. This ADC can add additional noise that will increase the low ENC values.

4.2 Integration Time

The integration time will be imposed by the accelerator; however, it is interesting to look at the gain as a function of integration time for all other parameters held constant. The integration time is the amount of time that the FE-CLK is low. In quoting chip performance, a standard of 100ns and 360ns integration times will be used, corresponding to the 132ns and 396ns bunch crossing settings.

4.3 Bandwidth Setting

The bandwidth is not just the "preamp bandwidth" set in the initialziation sequence. The "preamp bandwidth" setting selects among the discrete capacitors to be added to the dominant pole of the preamp circuit. The physical preamp bandwidth is a function of

1. preamp bandwidth capacitor settings chosen;
2. load capacitance;
3. preamp reset point as determined by the preamp and pipeline polarity initialization bit;
4. input transistor current, determined by AVDD2 and adjustable via the ISET1 resistor and **be specific** some shift register bits.
5. operating voltages AVDD2 and AVDD

The recommended setting for SVX3D is to use a single resistor for all the ISET pins in parallel with a value of 14kΩ to ground. For the SR bits, the input transistor bias current= 000 is recomnned. The operating volteages AVDD and AVDD2 should be set to 5V. For each measurement a bandwidth setting must be chose *after* the integration time and all other variables have been fixed.

In order to establish the optimimum setting, a criterion must be chosen. Two possibilities include:

- maximize signal to noise ratio;

- optimize the product of the sparse noise occupancy multiplied by the sparse signal inefficiency.

These suffer from the need to define a signal whereas benchmarking requires an easily reproducible and unambiguous perscription. This leads to the following suggestion. For each bandwidth setting (BW=0-7) the gain should be measured using the internal charge injection calibration for the loaded channel of interest. The gain should be constant for low BW values and start to fall of at higher values. The BW setting is chosen from that value that is on the plateau of the curve to within 5%. If there is any question as to the precise location of the plateau, the next lowest BW value should be chosen.

4.4 External Load Capacitance

The input transistor to the SVX3D chip is NMOS and no special care need be taken in connecting load capacitors to ground. The simplest method is to wirebond the chp pad to a trance and the put the capacitor to ground at the other end of this trace.

This is in contrast to a situation where PMOS input transistors are used leading to large sensitivity to power supply noise.

4.5 Calibration Voltage

Use of the internal calibration voltage circuit allows measurements to be compared among a variety of test stations. It is recommended that a 10KΩ resistor be placed in series with VCAL before the chip, and a 0.01 – 0.1 μF capacitor to ground be placed near the chip. This will filter out common mode noise and the capacitor will also keep the voltage constant during injections, thus giving the desired sharp charge pulse.

When noise measurements are peformed, it is essential to turn off the charge injection for the channel in question.

4.6 Presentation of Results

In order to compare different noise mesurements it is necessary to specify the conditions under which they were obtained. It is desirable to have a minimum number of parameters which must be kept under control and yet be flexible enough to compensate for differences between individual setups. Initialization bit settings fail this latter requirement. The ideal measurement is the direct value of the risetime which can then be adjusted to assure a constant value for the ENC versus C measurements. All other parameters are superfluous compared to this, including integration time provided that it is longer than the rise time.

An additional parameter that needs to be under control is the current in the input resisitor. This affects the bandwidth and the intrinsic noise itself; however, this only enters in the noise as a square

Ext. Capacitance	ADC rms	Gain (ADC/Volt)	ENC (e)
C_1	R_1	G_1	N_1
C_2	R_2	G_2	N_2
...	...	...	...
C_n	R_n	G_n	N_n

Table 4.2: Equivalent noise charge for various capacitances using noise and Gain as a control of the bandwidth setting.

root. Provided the values of the resistor and current described in Section 4.3 are used, the variation from one test station to another should be small.

Unfortunately it is not practical to make an accurate measurement of rise time. However, from the procedure outlined in Section 4.3, the same rise time should result for every external load. This can be verified by quoting the measured gain for each load value. It is expected that this gain remain constant. When using the ADC, quoting the noise as an RMS in ADC counts will give indication of binning systematics and, together with the gain, makes it clear what value was assumed for the internal capacitor. An example of a result is given in Table 4.2. In addition, an integration time of 100ns or 360ns should be used.

4.7 Unloaded Channels

It is often important to study the performance of unloaded channels. For example, testing of hybrids before they are mounted and bonded on ladders is done with unloaded channels. In this case care must be taken because the preamp will be very fast and at low BW settings the "rise time curve" is likely to have significant overshoot. This leads to an increase in the ADC rms noise and strange behaviour of the gain at low BW settings. Simply choosing the maximum value of BW leads to noise that is so low that binning systematics or noise sources other than the preamp input transistor may become important or dominant in the measurement.

for this special case of unloaded channels, the lowest BW setting that is still on a flat part of the gain vs. BW curve is the best choice. This curve will probably rise quickly at BW=0. At that point the noise is significantly larger than the 400e obtained from extrapolation of the data for unloaded channels and slightly less than the 800e obtained in the simulation of unloaded channels when BW=0. In the simulation the preamp is perfect and has no overshoot.

4.8 Robustness

In order to obtain consistent and correct results, the chip and teststand must be working together properly. It is desirable to study the systematic effects of varying the power supply voltage and repeating the measurements a number of times over several days. There should be a low common mode noise that must be kept significantly lower than the noise to be measured. Differential noise is useful in evaluating the level of common mode noise.

4.9 Differential Noise

This is the rms/$\sqrt{2}$ of the ADC value for channel i minus the ADC value for channel $i+1$. The important quantity to obtain is of course the total noise which the signal must exceed. It is possible for adjacent channels to have some correlation to their noise via shared power supplies, ground, and ADC ramp. Unloaded channels that overshoot may have extra coupling as well. This leads to larger noise but lower differential noise near BW=0. Nonetheless, while differential noise may be a useful diagnostic to gauge the amount of system noise present, it is not appropriate as a measure of performance.

4.10 Simulations

The principle simulations should predict the noise; however, these simulations are notoriously bad at accurately predicting bandwidths. Therefore tuning of these simulations to data will have to be performed in any case. Furthermore, the noise seen in the SVX3D is dominated by the input transistor and it is the dependency of its noise on length, width, current, oxide thickness, capacitive load and amplifier rise time, not just BW, which must be considered.

Chapter 5

Electrical Specifications

Absolute Maximum Ratings			
Parameter	Minimum	Maximum	Unit
Supply Voltage - DVVD	-0.5	6.5	V
Supply Voltage - AVVD	-0.5	6.5	V
Supply Voltage - AVVD2	-0.5	6.5	V
Input Signals	-0.5	DVDD + 0.5	V
Calibration Voltage	-10??	+10??	V
Ramp Reference Voltage	-0.5	DVVD+0.5??	V
Ramp Pedestal Voltage	-0.5	DVVD+0.5??	V
Operating Temperature	0	+70	C
AVVD2	2.50	5.00	V

Table 5.1: A table

Recommended Operating Conditions				
Parameter	Minimum	Nominal	Maximum	Unit
Supply Voltage -DVVD	4.75	5.0	5.25	V
Supply Voltage - AVVD	4.75	5.0	5.25	V
Supply VoltageAVVD2	2.5	3.5	5	V
Time delay DVVD to AVVD on	???			ms
Time delay AVVD to AVVD2 on	???			ms
Low Level Input CMOS	0		0.8	V
High Level Input CMOS	2.2		DVDD	V
Differential Input CDIF$_{DIFF}$	.80	1.0	DVVD	V
Differential Input Offset CDIF$_{OFF}$	CDIF$_{DIFF}$/2	2.5	DVVD-CDIF$_{DIFF}$/2	V
Ramp Pedestal Voltage	1.5		3.5	V
Ramp Reference Voltage	1.5		3.5	V
FE-CLK (Initialize)^2			25	MHz
FE-CLK (Acquire)			25	MHz
BE-CLK (Digitize)^2			75	MHz
BE-CLK (Readout)			30	MHz

Table 5.2: A table

DC Characteristics				
Signal Type	Minimum	Nominal	Maximum	Unit
Digital High level - $CMOS_{HIGH}$	2			V
Digital Low level -$CMOS_{LOW}$			0.8	V
Digital Source current -$CMOS_{Iout}$				mA
Digital Sink current - $CMOS_{Iin}$				mA
Input capacitance - $CMOS_{Cin}$				pF
Output capacitance $CMOS_{Cout}$				pF
Differential level CDI_{FDIFF}	20	100	200	mV
Offset level $CDIF_{OFF}$	$CDIF_{DIFF/2}$	2.5	DVVD-$CDIF_{DIFF/2}$	V
$CDIF_{Iout}$				mA
$CDIF_{Iin}$				mA
Input capacitance $CDIF_{Cin}$				pF
Output capacitance $CDIF_{Cout}$				pF
Supply Current AVVD	???	???	???	mA
Supply Current AVVD2	30	40	50	mA
Supply Current DVVD	3	10	20	mA
DVVD during Readout	30	50	50	mA

Table 5.3: A table

Chapter 6

Connecting the Chip

this section needs to have standard signals, pad names, etc. and to refer to 2.4 In fact, maybe that section should be combined with this section.

The SVX3D chip is a monlithic chip incorporating a "front end" section and a "back-end"section. In earlier versions these were on separate chips, and it is still common practics to refer to the "front end" and "back end" areas. Thus, the following nomenclature is used:

- BE $\longrightarrow$ "BE" is for "back-end". This area has the digitization, FIFO and readout logic.
- FE $\longrightarrow$ "FE" is for "front-end". This area has the analog amplifier, pipeline, and deadtimeless skip-logic.
- Hybrid $\longrightarrow$ the ceramic circuit layout that holds 2 to 7 SVX3D chips and services either the r-ϕ side or the z side of the silicon sensors. One hybrid pair forms the complete readout for a sensor.

6.1 Connecting the Chip for Single or Daisy Chained Operation

1. Ideally there should be one very large bypass capacitor (greater than 1 μF) per hybrid pair for AVDD and DVDD. The hybrid set for layer 0 has space for only one capacitor of this size, which should be conected to DVDD.
2. DVDD of the FE should NOT be connected to DVDD of the BE. All of the following FE power pads should go to the same 0.1μF bypass per chip (for layer 0 this means four capacitors): AVDD, AVDD2, QVDD and DVDD
3. AVDD and AREF on the BE should connect to the same point as all of the pads mentioned in the previous rule. DVDD of the BE should be connected to the same point as SVDD, and should have one 0.1μF bypass per chip.
4. Table 6.1 below summarizes which pads should be connected to which power feeds.

Pad Name	Analog Power	Digital Power
(FE) AVDD2	X	
(FE) AVDD	X	
(FE) QVDD	X	
(FE) DVDD	X	
(FE) AVDD	X	
(FE) AREF	X	
(BE) DVDD		X
(BE) SVDD		X

Table 6.1: Power for the SVX3D

5. There should be one common ground plane for the chip sets on the hybrid. An exposed section of this ground plane is where the back face of the SVX3 chip rests. The digital power feed should have its own return line, connected to the ground plane at one point per hybrid.

6. Table 6.2 summarizes which pads should be connected to which grounds.

7. ISET1A, ISET1B, and ISET2 should all be tied together and connected to a 14k resistor to ground. They should have a 0.01μF bypass (one per chip) to the same analog power mentioned in the previous rules.

8. **What about VCMTH?**

9. IQUIESCENT should be biased with a 6.8k resistor to the same analog power mentioned in the previous rules. ISLOPE should be biased with a 100k resistor to ground. IDRIVERS should be connected directly to the analog power feed.

10. FE-CLK and FE-CLK*, BE-CLK and BE-CLK*, should be differentially terminated once per hybrid pair to the characteristic impedance of the control cable. This impendance is expected to be 80-100 ohms differential.

11. PRD2 should be terminated once per hybrid pair with a 300 ohm resistor.

12. Hybrids that are not for layer 0 will require bonding in the gap between chips. Therefore a minimum 54 mil gapis required between the chips.

6.2 Guide for Daisy Chain Operation

The SVX3D is designed for daisy chained operation to minimize the number of bus and control lines required to operate the device. (Fewer control lines means less space on the high density interconnect and less mass in the system.) A group of daisy chained chips is shown in Figure 6.1. All of the chips share a common communication bus (BUS0-7) and a common differential clock (FE-CLK, BE-CLK).

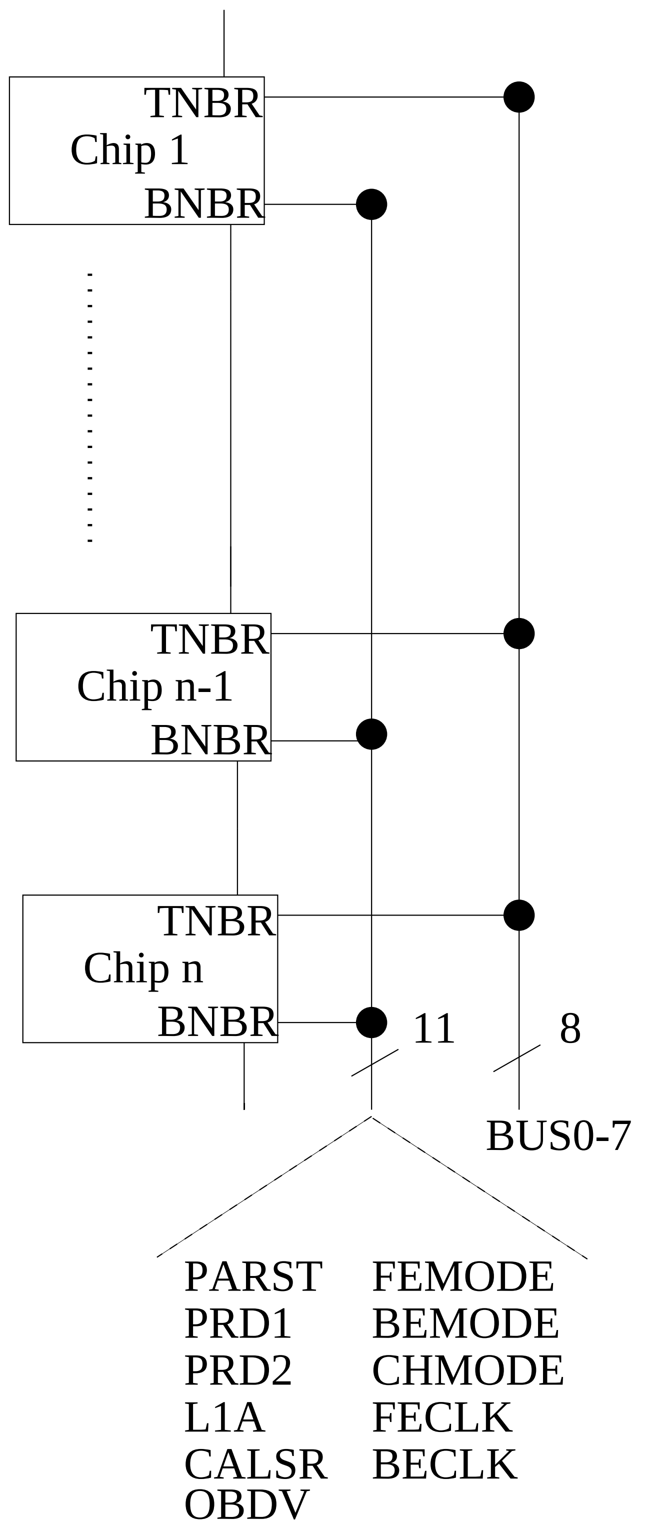


Figure 6.1: Daisy chained readout chips.

Pad Name	Ground Plane	Digital Return
(FE) QGND	X	
(FE) DGND	X	
(BE) DGND		X
(BE) DSUBS	X	
(BE) SVDD		X

Table 6.2: Grounding of the SVX3D

In addition, each chip has two pins called TN and BN which are used for communication between adjoining chips.

After power up of the SVX3D's, the chip parameters listed in Chapter 3 must be downloaded before useful operation of the readout chips can begin. For each SVX3D chip, 197 bits must be downloaded into internal registers. In the Initialize Mode, the TN and BN pads are used as a serial data link to form a very long shift register for downloading parameters to the string of daisy chained SVX3D's. Parameters for each of the chips are loaded in sequential order with data for chip #1 loaded first via the BN pad on the last chip in the daisy chain. Data is clocked between cells in the shift register using the common differential clock pads. If there were 10 chips in the chain, exactly 1970 bits would have to be downloaded in the Initialize Mode. Downloaded parameters may be checked by shifting the bits out through TN of the first chip while reloading the chips with the same data. To identify each chip in the daisy chain, a separate chip ID number (bits 137 - 143) is downloaded into each chip during the Initialize Mode. The seven bit chip ID number allows chips to be tagged with numbers from 0 to 127.

Still true? In the Acquire Mode, the BUS0-7 and clock pads provide simultaneous real time control of all of the chips in the daisy chain. These pads perform critical timing functions within the chip. The TN and BN pads have no function in the Acquire Mode.

In the Digitize Mode, the BUS-7 and differential clock pads provide simultaneous real time control of all the chips in the daisy chain. Again, these pads perform critical timing functions within the chip. The TN and BN pads are used to pass neighbor information between adjacent chips for neighbor readout in the Digitize Mode.

In the Readout Mode, the BUS-7 lines are changed from input lines to output lines. During readout, data from each SVX3D chip is placed on the common bus beginning with the top chip in the daisy chain and proceeding sequentially through the remaining chips. Information is placed on the bus in 8 bit bytes. First the chip ID and status of the first chip is read out. Then the address and data information for that chip is read out beginning with the channel nearest the top of the chip, channel 1, and proceeding downward. Priority for the output is passed from pad BN of the first chip to pad TN of the next chip after the first chip has been completely readout. (The top chip in the daisy chain will have a priority first since the TN pad is internally pulled weakly low to initiate readout). Information is read out using both the high *and* low transitions of the differential clock. Thus, the channel readout rate is approximately equal to the BE-CLK clock frequency.

Chapter 7

Miscellaneous Considerations

Chip initialization is expected to occur infrequently. The parameters for the chip setup are held in static latches which are not expected to change until the next initialization. One of the parameters set in the latches is analog time delay which is an offset between the read and write pointers in the analog storage section. Once the chip leaves initialization, these two shift registers on all of the chips in a system could de clocked at a 7.6 MHz rate for an indefinite period of time. The amounts to 1xE13 to 1xE14 clocks per hour in a relatively large system. If a glitch (ringing, infrequent coincident noise sources) occurs on a clock line somewhere in the system, the electrical delay for one or more of the chips could be incorrect leading to scrambled data. Although this should be unlikely, the results could be messy. One way to check the integrity of the data is to use the test input feature and readout all chips. The input test mask should be loaded for one hit channel per chip and pulsed during an acquisition mode beam gap. After the appropriate delay time, all the chips should be read out. If channel 1 was pulsed and the Neighbor Enable is active, three channels per chip (1,2,128) would be read out and the neighbor hit feature would also be checked. If any chip does not read out hit information, the time delay may be incorrectly set, and previous data from that chip should be suspect. A test of this nature may be warranted either once an hour or once a minute depending on experimental results in the actual installation to provide confidence in the data integrity.

It is recommended that the power supplies for the SVX3D be turned on in the following sequence: AVDD then DVDD. In benchtop testing, latchup has not been observed using this sequence.

Appendix A

Typical Initialization Settings in Use

Different groups are using different initialization sequence patterns. To compare these patterns, it is necessary to know the translation of what the bits and values are called in the code, input file, GUI etc employed by the groups. This is given in Tables A.1 and A.2. Using this translation, the initialization bits in use by various groups are given in Table A.3.

The settings for the five bits that determine the calibration charge injection are more complicated and those are found in Table A.4. They turn out to all come from valid combinations listed in Table 3.4 but nobody uses the same settings: All options are used. The gain scan settings for the XTL stand are obtained by choosing either "neg. polarity" or "pos. polarity" from the GUI. Control over the bits is always available from the chip parameter setting GUI although Ramp Dir and Comp Dir are forced to be equal. For the STAR test stand, the initialization file has the "Polarity" option that takes on values "Negative" or "Positive" and the "pipePolarity" option that takes on values "Normal" or "Inverted". The bit patterns generated for the program are then detailed in Table 3.4.

In addition to the specific settings in the tables, som comments on the ISEL settings are in order. First, there are George's settings for ISEL:

ISEL 1-11 int. input bias	5	(4 bits)	0101
int. reset bias	0	(2 bits)	00
pipe write bias	3	(3 bits)	011
pipe read bias	3	(2 bits)	11

Then Tom's settings for ISEL 1, 3, 7, 8, 10, and 11 high agree: 11011000101.

The meaning of these bits is:

- **ISEL 1-4:** Adjust integrator bias. Affects noise and BW. Ignore ISEL4, it really shouldn't be there but it was too much work to take it out.
- **ISEL 5-6:** Reset bias. Determines time required to reset integrator. Fast reset is desireable, but can also make things oscillate.
- **ISEL 7-11:** Pipeline bias bits. Affects pipe ramp risetime. To minimize power dissipation, set

Front-End Bits				
BITS	PARAMETER	XTL	DAQ	Star
1-128	channel mask $[0:127]$	Channel Calibration Mask	Mask	mask15,etc.
129	Cal Direction	Calibration polarity bit	Polarity	
130	FE Polarity	Pipeline select (Preamp. Pol)	Pipe Polarity	
131-133	Preamp Bandwidth $[0:2]$	Preamp Bandwith (0-7)	Bandwidth	bandwidth
134-139	Pipeline Delay $[0:5]$	Pipeline delay	Pipe Depth	pipedepth
140-150	ISEL $[1:11]$	Bias bits:	ISEL 1-10	
		type bianry numbers		
	int. input bias	Integrator input transistor bias current (3 bits)		nIBias?
	int. cascode current	Integrator cascode current (1 bit)		nIBias?
	int. reset bias	Integrator reset bias (2 bits)		nIBias2
	int. write bias	Pipeline writeamp bias (3 bits)		nIBias3
	int. read bias	Pipeline readamp bias (2 bits)		nIBias4
151	Readout Order	Readout order (PB)		

Table A.1: Translation table for Front-End bit initialization values used in various test setups.

to minimum value that gives required speed (for write and read pieplines).

Back-End Bits				
BITS	PARAMETER	XTL	DAQ	Star
152-158	Chip ID [0 : 6]		Chip ID	chipid
159	Dynamic Threshold EN		Dynamic Threshold Select	
160	Iquiescent Bias Ratio Select	Bias Ratio Select	Bias Ratio Select	BiasRatio
161	Driver Bias Cmode Sel	Common Mode Select	Driver Common Mode Select	ComMode
162	Last Chip		Last Chip	last chip
163	Read Neighbors	Read neighbor	Read Neighbors	
164	Read All	Read all	Read All	
165	Ramp Direction	ADC/comparator ramp*		
166	Comparator Direction	ADC/comparator ramp*		
167-174	Ramp Cap Adjust [7 : 0]	Ramp cap. adjust	Ramp Trim	ramp trim
175-182	Threshold [0 : 7]	Spars. threshold	Threshold	threshold
183-190	Counter Modulo [7 : 0]	Counter modulo	Counter Modulo	counter
191-193	Output Driver Resistor Sel.	Output driver resistor select 3 bit binary, SVX3D only	Driver resistor, 3 bits as integer r to l	outdrv
194-197	Ramp Pedestal	Ramp pedestal(0-15)	Pedestal	rampped

Table A.2: Translation table for Back-End Bit initialization values used in various test setups. Notes: * These two bits must be the same so they are only one bit in the XTL GUI.

Front-End Bits					
BITS	PARAMETER	XTL	DAQ	Stimulus	Star
1-128	channel mask [0 : 127]	0	mod 8	alternating	1000...
129	Cal Direction	1		0 or 1 *	
130	FE Polarity	0	1	0 or 1 *	
131-133	Preamp Bandwidth [0 : 2]	5	3	2	7
134-139	Pipeline Delay [0 : 5]	2	4	40†	9
140-150	ISEL [1 : 11]		11011000101		
	int. input bias	100		5**	5**
	int. cascode current	0			
	int. reset bias	10		0	0
	int. write bias	100		3	3
	int. read bias	10		3	3
151	Readout Order	1		0 or 1 *	
Back-End Bits					
152-158	Chip ID [0 : 6]	128+n ***		?	6
159	Dynamic Threshold EN		0	?	
160	Iquiescent Bias Ratio Select	1	0	?	0
161	Driver Bias Cmode Sel	0	0	0	0
162	Last Chip	††	1	1	1
163	Read Neighbors	0	0	0	
164	Read All	1	1	1	
165	Ramp Direction	0		0 or 1 *	
166	Comparator Direction	0		0 or 1 *	
167-174	Ramp Cap Adjust [7 : 0]	0	5	120	0
175-182	Threshold [0 : 7]	10	254	0	254
183-190	Counter Modulo [7 : 0]	250	250	250	250
191-193	Output Driver Resistor Sel.	101 †††	5	?	5
194-197	Ramp Pedestal	10	6	7	6

Table A.3: Initialization values used in various test setups. Notes: * described in the appendix on the polarity bits and cal inject; †For 132ns operation; ** combined with cascode current; *** n=1 for first chip, 2 for second, etc. automatically set in software, depending on number of chips chosen; †† Last chip is automatically set **What is it now? 0?**; †††Binary

Name	Bit	XTL	
		pos	neg
Cal Direction	129	1	0
FE Polarity	130	0	1
Readout Order	151	1	1
Ramp Direction	165	0	1
Comparator Direction	166	0	1
Combination		6	4

Name	Bit	Stimulus			
		pos		neg	
Cal Direction	129	1	1	0	0
FE Polarity	130	1	1	0	0
Readout Order	151	0	1	0	1
Ramp Direction	165	0	1	1	0
Comparator Direction	166	0	1	1	0
Combination		7	8	1	2

Name	Bit	Star			
Polarity		"Negative"		"Positive"	
pipePolarity		"Inverted"	"Normal"	"Inverted"	"Normal"
Cal Direction	129	0	0	1	1
FE Polarity	130	1	1	0	0
Readout Order	151	0	1	1	0
Ramp Direction	165	0	1	0	1
Comparator Direction	166	0	1	0	1
Combination		3	4	6	5

Table A.4: Settings of the bits used to control charge injection. The "Combination" refers to the previous table bit patterns.

.

Appendix B

Measurements of Timing on Various Test stands

In this chapter, the specifications and descriptions of the previous chapters are confronted with measurements in the systems which are in use. The measured patterns are compared to the specifications and to each other.

B.1 Systems in use

The SVX3D is currently being studied using a variety of systems covering a range of complexity, expense, and data transfer bandwidth. The systems are:

- **The XTL test stand** This is also referred to as the "burn-in" system because it's intention is that it can be used to take data for several days and trace the operation of the SVX3D for such a time period. This test stand is based tests an SVX3D by:

  1. Sending the timing sequence from a PC to a FIFO;
  2. clocking the FIFO signals to a bus that drives the chip signals;
  3. reading the data back into a FIFO;
  4. reading the data in the FIFO back into a PC for analysis.

  This system has the advantage that the components for interfacing to the SVX3D are cheap and that it can be run on a PC using the LYNUX operating system. The signals to be sent to the chip are specified in ascii files indicating that the line should be high or low for each clock pulse. This is easily modified. It has the disadvantage that the clock pulses are not delivered continuously, but in bursts. It also is limited by the depth of the FIFO and multiple triggers are not allowed. It is custom made and hence available in limited quantities. It has not been made triggerable although it should be possible.

- **The Stimulus system** This system works in a manner similar to the XTL system. However it is based on a general pattern generator that is quite expensive and rather delicate to program. It is however an off-the-shelf item. It has not been set up in any triggerable manner.
- **The DAQ** The DAQ system is the CDF system for taking data for a large number of SVX3D chips – the entire silicon detector system. This system is extremely complicated, having requirements of special light weight boards, high speed and large data transfer volume. It run continuously and is triggerable.
- **STAR** The STAR system is similar to the DAQ system in complexity and expense and is triggerable. It can be used in connection with a laser to scan modules. It runs patterns in bursts, in a manner similar to the XTL and Stimulus systems.

B.2 Measurements of the Basic Sequence

Analysis of the basic sequence of signals going to and coming from the SVX3D involves studying the Digitization and Readout Modes while Acquisition is occurring. Items of interest to observe are the changes that occur at each of the mode boundaries, the acceptance of a trigger and its handling, and the return of a pipeline cell after readout. For the systems that do not run continuous sequences, it is useful to examine the start and end of the sequence chain and to compare the state of the various lines before the start and after the end of a sequence burst.

This suggests the following measurements be made:

1. **Basic Clock Rate** A measurement of the clock speed used to drive the sequence of signals going to/coming from the chip is useful in each of the systems. Systems may be able to only change states at a one-half their basic clock rates. This has consequence for the rate at which the FECLK or BECLK may be run in comparison to the basic clock rate.
2. **Full Sequence** A snapshot of the full sequence starting with the beginning of the burst of signals going to the SVX3D and ending with the end of the burst gives an overview of which lines make transitions at which points. Detailed timing relationships cannot be easily observed.
3. **Preamp Reset** The reset of the Preamp should, in CDF operation, occur between bunches. This is handled differently on various systems and may affect the results they produce. Measurements of where these transitions occur have been made.
4. **Start of Sequence** The disposition of the various signal lines at the start of the sequence is relevant for systems that do not run continuously.
5. **Level 1 Accept** The level 1 accept causes the pipeline cell to be put aside. In the DAQ system this should be followed by **What happens** that causes digitization to occur and by **what happens?** so that readout is triggers. In the systems used, most of this is ignored and level 1 accept is immediately followed by digitization and readout. Hence it is useful to measure the state of the various lines around receipt of level 1 accept to see how the systems behave.

6. **Digitization** Resetting of the Wilkinson ramp, the counter, the threshold comparators and the interaction with the PRD1 signals which place the pedestal and then the signal capacitor in place for measurement are critical portions of SVX3D operation and are hence interesting to measure.

7. **End of Digitization** The signalling of the end of the digitization and the observation of the operation of the top and bottom neighbour logic in action are interesting to document.

8. **End of Digitization/ Beginning of Readout** The transition from the end of the digitization to the readout, noting the modification of the BEMODE line over this boundary is of interest to document.

9. **Beginning of Readout** Examination of the data lines and correlation of the data with that which are eventually seen in computer memory of the device used to store the data are interesting to study.

10. **End of Readout** The final data words, together with observation of how the data stream to the computer is terminated, are correlated with the data as they appear on the computer.

11. **End of Sequence** The end of the commands sent to the chip for systems which send only bursts of sequences are useful measurements so that the quiescent state of the lines between bursts can be studied.

B.3 Measurements on XTL

The measurements described above have been performed on the XTL stand. The frequency of the clock was 25MHz, about half the speed that the FECLK should run in the final system. As mentioned in the introduction to this chapter, there is a detailed discussion of the XTL signals. In the following sections on the other systems, differences with this system are noted and similarities no longer discussed. Hence, the discussion begins with a description of the XTL stand and signals special to this stand. From there the basic clock is studied and an overview of the entire cycle of Acquisition, Digitization and Readout is given. This is followed by some detailed discussion of specific portions of that cycle.

The measurements were made using the MM6 chip card containing a **MIN MAX or SVX3D!!!!!** chip. The TTL signals going to the chip card were measured at the pins on the connector to the chip card and are indicated in the figures with the prefix "CH_". The differential signals were measured on the scrambler board and are indicated by the prefix "SC_" in the figures. In addition to the basic clock signals common to all systems, there are special signals peculiar to the XTL system. These are:

- **SC_RCK** The "raw clock" is the clock used to drive the FIFO's that contain the sequence of signals for the chip. This clock is also used as the BECLK under certain conditions. This is determined by the use of the SC_CSL bit described next.

- **SC_CSL** The "clock select" level is used to determine if the BECLK is derived from the sequence in the FIFO (or "patterns") or directly from the raw clock.

B.3.1 The XTL clock and a Full Cycle Overview

Figure B.1 shows the raw clock at some point during digitization. The markers have been placed such that they are 4 cycles apart and the measured value is 160.6ns, corresponding well with the expected 25 MHz frequency of the oscillator.

In Figure B.1 it is possible to look in detail at the relationship of the various clocks in some detail. The clock select line (SC_CSL) is low. This means that the XTL system is deriving the BECLK from the sequence in the FIFO. The BECLK is running at half the frequency of the raw clock (SC_RCK) and in constant phase. The FECLK is running at one quarter the raw clock speed and in constant phase. The FECLK and BECLK make transitions at the same time. It is noteworthy that a transition in the FECLK at the BECLK boundary is visible for a short time between two FECLKś in this picture. This is probably not intentional. The data lines, SC_0 through SC_7, make transitions in phase with the BECLK.

The full sequence of data is shown in Figure B.2. The cycle begins with a PRD2. Usually this signal is used to put a pipeline cell back into the pipeline; however, as described in §2.1.2 PRD2 also causes the reference capacitor pedestal to be reacquired and it is for this reason that it is issued at the start of the sequence. If this is not done, the first event is corrupted by having a random charge on the reference capacitor. A PRD2 is performed and the FECLK begins to run in a rather complicated pattern until the preamp reset (PRS) is dropped. In fact this is quite different from the mode in which the chip would usually be operated. As indicated in §2.3.8 a preamp reset is normally a short pulse of duration **200 or 400ns** . In this case, the preamp has been cleanly reset at the start of sequence. The intention is to ensure that transients due to operation in a burst mode do not influence the measurement of the chip performance. After his preamp reset, the FECLK cycles for some time, simulating a continuous stream of cycles. Charge is injected into the preamps by the CALSR line low-high transition (CH_CST) and a level 1 accept is generated. The level 1 accept is to narrow to be visible on this scale but occurs at the first dotted line.

The level 1 accept puts the pipeline cell aside for digitization and readout. Indeed, the pipeline read 1 signals (CH_PD1) are issued together with the various digitizer reset signals on BUS0–BUS3 (SC_0 to SC_3). The exact timing of this can be see in Figure B.3 and is discussed in some detail below.

It is also noteworthy that the clock select line changes, indicating that the BECLK is operating at the speed of the raw clock. The BECLK cannot be seen but for the time that the clock select is low, it is running at the raw clock rate.

At the end of digitization, BNBR had undergone a low/high transition indicating that the last channel on the chip is above threshold. The TNBR high-low transition is not visible because TNBR is instructed by the sequence to be held low.

At end of the digitization, the BUS0–BUS3 lines are set back to high as are all the bus lines. A transition of change mode from low to high and back is then made. At the same time TNBR is set high and the BEM is changed to low. It is noteworthy that the change mode remains high until the BEM level is modified and then change mode is modified. This prepare the back end for readout, but the channel readout begins only when TNBR goes down. The FECLK ffrequency goes up just as the change mode occurs. The behaviour around this change mode is complex and hence examined in detail in Figure B.7 and the corresponding discussion below.

As the TNBR transition from high to low is made, the readout begins. The data lines are active. The channel mask has been set up such that every eighth channel had charge injected. The amount of charge injected was adjusted such that BUS7 of the Gray-coded binary signal was 1. The first and last channels also had charge injection. Hence, between those two channels, there are 15 high signals on BUS7 marking the 128 channels that are read. At the end of readout, BNBR goes low as it would be TNBR for the next chip. The FECLK is stopped, a Change mode occurs strobing in the change in BEM.

Shortly after this the burst of signals from the FIFO ends and the lines go to a quiescent state. There are some uncontrolled transitions of some of the lines, most notably the change mode and data lines. The preamp reset is held high and remains there until the next burst.

B.3.2 Preamp Reset

The preamp reset high-low transition is shown in Figure B.3. It is interesting to note the slightly irregular behaviour of the FECLK around this transition. The raw clock is running at three times the rate of the FECLK.

B.3.3 Start of Sequence

The sequence begins with the raw clock running, a change mode is issued, ensuring that the BEM and FEM states are properly registered high, and the FECLK begins to cycle. A PRD2 refreshes the reference pipeline cell and the FECLK is gradually brought up to one third the raw clock speed. Then as described in §B.3.2, a preamp reset is done.

B.3.4 Level 1 Accept

The relationship between the injection of charge by the CALSR transition and the level 1 accept is shown in Figure B.5. **Is there a SPEC on this!?!?!**. Also, that there are two pulses because **WHY** can be seen. The relation of these pulses to the FECLK can be compared to the specification indicated in Figure 2.17 and Table 2.5. It can be seen that the full level 1 accept cycle occurs while FECLK is low. **Why 2, what is t4?**

B.3.5 Start Digitization

This is under dispute! The start of digitization measured in Figure B.6 and is compared to the specification in Figure 2.18 and Table 2.6. The data lines are used as CNTR-RST RAMP-RST COMP-RST and RREF-SELÅs described in §2.2.2, after the first PRD1, the comparator reset should go low. After the second PRD1 which switches the charge stored on the pipeline cell on to the read amplifier, Figure 2.18 indicates that the RREF-SEL is followed by the ramp and counter resets. However, the measurement shown in Figure B.6 shows thatRREF-SEL has gone low before the second

PRD1. **Is this allowed?** RAMP-RST and COMP-RST undergo a high-low transition in the proper sequence after the second PRD1.

B.3.6 End Digitization and Start of Readout

The end of digitization and the start of readout is measured in Figure B.7. The specifications may be found in Figure 2.19 and Table 2.7. The measurement of the control lines, BUS0–BUS3 shows they are set high at the same time, except for BUS2. They should all be set high at the same time according to Figure 2.19; however, this seems not to have an impact and there is no specification for this in numbers. Change mode is set high. Before it goes low, BEMODE is set low and both TNBR and BNBR are set high. These are shown in the specification as coming at the same time as one another as as the transition in BEMODE but there is some deviation from that measured here. The forgotten BUS2 is also set high. Change mode falls and the FEMODE and BEMODE are strobed in, particularly the changed BEMODE. The BECLK is under the control of the sequence coming from the FIFO because the clock select has been set high. There are some irregularly spaced BECLK's **Is this important?** and the FECLK has an extra wide pulse. The fall of TNBR signals the start of readout. There are six BECLK after the fall of TNBR and in this time all data lines are high. The data file on the PC starts with six values of 255. **We clock on both edges so we want 12, not 6 values of 255???**. The dumped event from XTL is given here:

```
raw data dump at 11:41:05, machine cdfbu2.fnal.gov : 1 chips
   0:  255  255  255  255  255  255    0  129   20    0
  10:  227    1  117    2  114    3  117    4  117    5
  20:  118    6  117    7  119    8  231    9  117   10
  30:  116   11  116   12  119   13  117   14  118   15
  40:  119   16  230   17  117   18  119   19  117   20
  50:  117   21  119   22  117   23  116   24  229   25
  60:  124   26  118   27  117   28  119   29  119   30
  70:  118   31  116   32  231   33  119   34  117   35
  80:  119   36  115   37  118   38  118   39  116   40
  90:  231   41  119   42  124   43  117   44  117   45
 100:  117   46  117   47  116   48  225   49  119   50
 110:  116   51  116   52  119   53  117   54  116   55
 120:  116   56  231   57  117   58  125   59  116   60
 130:  116   61  117   62  117   63   91   64  198   65
 140:   75   66   80   67  116   68  116   69  119   70
 150:  117   71  119   72  230   73  117   74  116   75
 160:  116   76  116   77  117   78  117   79  117   80
 170:  230   81  119   82  117   83  116   84  117   85
 180:  119   86  117   87  116   88  228   89  116   90
 190:  117   91  124   92  117   93  114   94  114   95
 200:   90   96  203   97  116   98  116   99  124  100
 210:  124  101  116  102  116  103  117  104  228  105
```

Bit Pattern	Binary to Decimal	Gray Decoded
1 1 1 0 0 1 1 0	230	187
0 1 1 1 1 1 1 1	127	
0 1 1 1 0 1 0 1	117	89
0 1 1 1 1 1 1 0	126	
0 1 1 1 0 1 1 1	119	90
0 1 1 1 1 1 0 1	125	

Table B.1: Bit patterns seen at end of data readout.

```
220:  117  106  117  107  117  108  117  109  124  110
230:  117  111  124  112  231  113  116  114  116  115
240:  124  116  119  117   95  118   81  119   74  120
250:  220  121  117  122  124  123  117  124  116  125
260:  119  126  117  127  230  230  247  255  255  255
```

Since the data are transferred on both edges of BECLK the next clock shows 0 on the data line and that is what is found on the PC. The first dashed line corresponds to the fall of the eighth clock of BECLK after TNBR fell. The value on the line appears to be 129 and this is indeed the chip id read as the eighth value. After this comes the pipeline cell, where BUS4 and BUS2 are set high, indicating cell 20 was read. This is confirmed in the data. This is followed by channel id 0, the first data channel data, channel id 1, the second data channel data and so on. The bit pattern for the first channel is 11100011 or 227 if the bits are interpreted as binary values. Note that this is what appears in the data dump. Thus, the data dump gives the decimal value of the Gray code interpreted as a binary code. The Gray Code translation in Table C.2 indicates that this pattern actually corresponds to 189. The first channel had charge injection enabled and hence a rather large value is observed. Channel 1 has a bit pattern 01110101, or 117 if interpreted as binary bits and converted to decimal. Table C.1 can be used to translate this to the correct decimal value of 89. **something sets this!?**.

After eight more BECLK cycles, channel eight is read and this had charge injection. Indeed, BUS7 is high and this continues for every eight channel. This is shown for more channels in Figure B.8. It is notable that there are a number of short pulses in various lines. These do not seem to affect the data.

B.3.7 End of Readout

The measured end of the readout cycle is shown in Figure B.9. It is interesting to see where the data really end. This can be seen by comparing the data in §B.3.6 to the pattern in Figure B.9. The distinct pattern on BUS7 makes the analysis easier. There is a high transition followed by a final high transition and a small, fast, low transition before the signal goes high for some number of clocks. This last high transition is the last channel. Reading *backwards* from the figure, the bit patterns are given in Table B.1. The first column in the table is the pattern, the second is the pattern interpreted as a binary code and converted to decimal, and the final column is the Gray code interpretation for the case that the value was Gray coded.

This clearly establishes where the readout ends. Indeed, at the end of the sequence BNBR falls. It is TNBR for the next chip and starts readout on that chip. PRD2 puts the cell back into the pipeline. This is followed by a "mini-digitize" sequence where change mode and back end mode are cycled twice. Also, the preamp reset is put high again; BNBR is set high since this is the only chip being read. CALSR is lowered and the BECLK undergoes a rather irregular set of pulses during the mini-digitize. The last part of the mini digitize has the data lines all set low and then they go high. The lines undergo some rapid transitions and finally reach the quiescent high state. The purpose of all this is **WHAT?**.

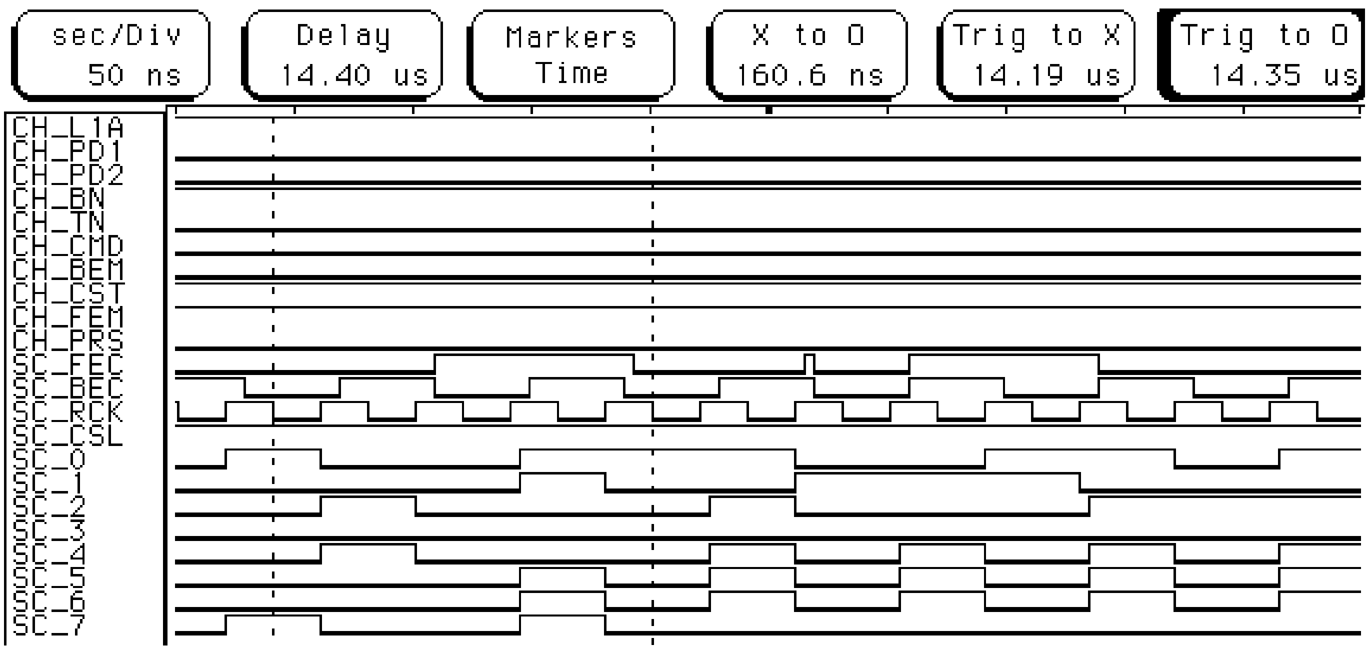


Figure B.1: XTL: Clock cycles.

B.4 Measurements on Stimulus

In this section, the Stimulus system clock patterns are compared to the specification and to the XTL system. The measurements were done in two sets because of a limited number of probe channels. The FECLK and BECLK were measured using only one side of the differential signal and therefore do not look very good. The only signal specific to this system is the FIFO clock (FF_CLK) which runs with a period of 140ns, corresponding to 7.14 MHz. Chip MM1 was used for these measurements.

The clock cycles are compared in Figure B.10. The FECLK is running four times slower than the BECLK which has a period of 140 ns, the same as the FIFO clock.

The full sequence is shown in Figure B.11. Comparison of this to Figure B.2 reveals a number of differences. First, at the start of the burst, FEMODE and TNBR are lowered at the same time.

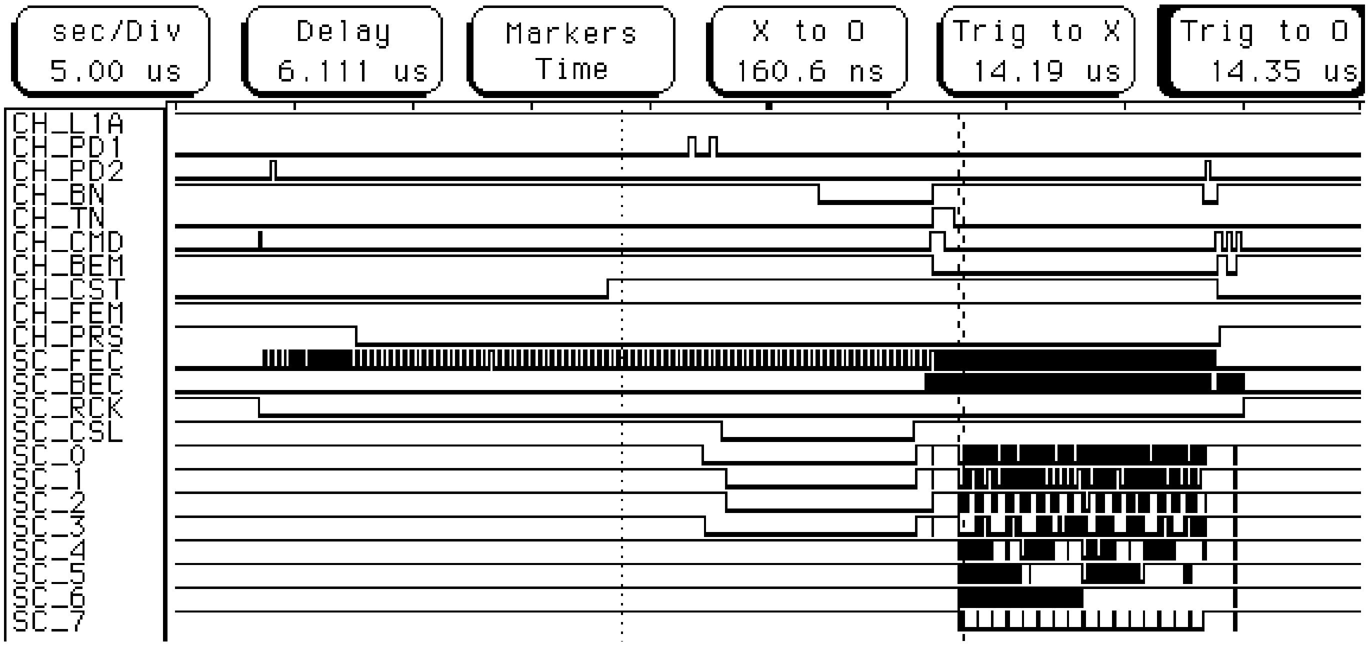


Figure B.2: XTL: Full Sequence.

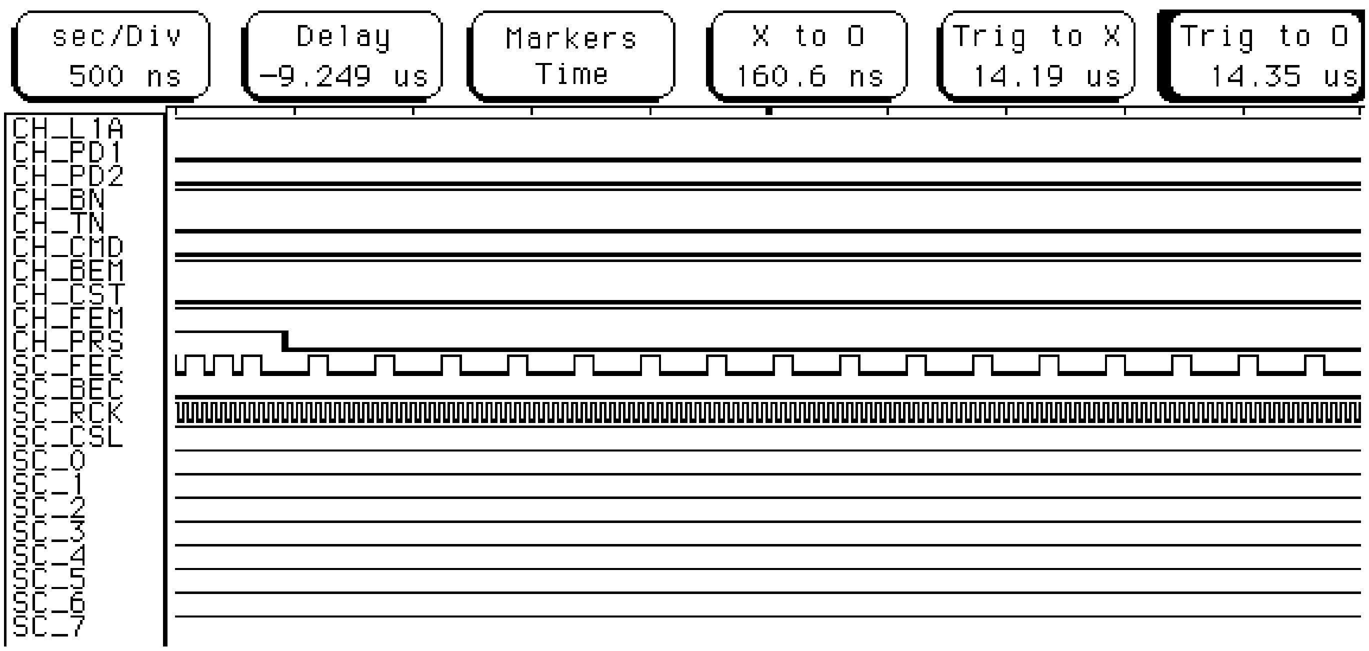


Figure B.3: XTL: Detail of Preamp Reset.

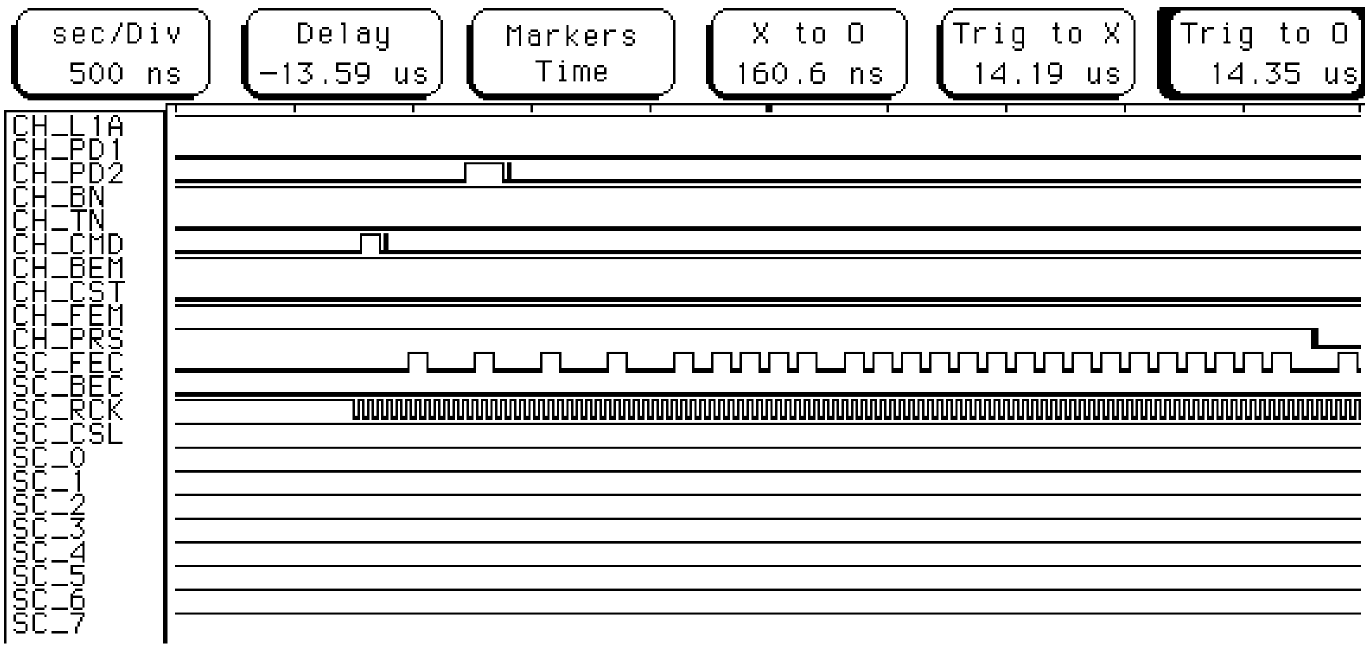


Figure B.4: XTL: Start of Sequence.

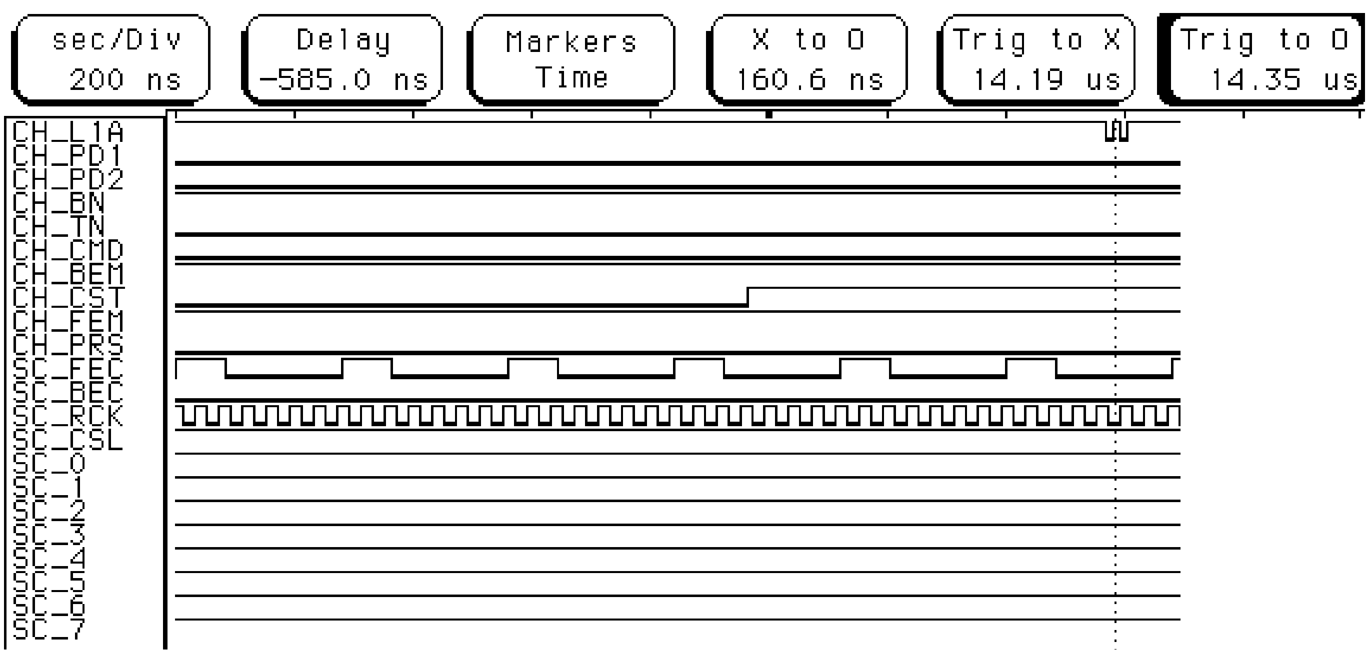


Figure B.5: XTL: Level 1 Accept.

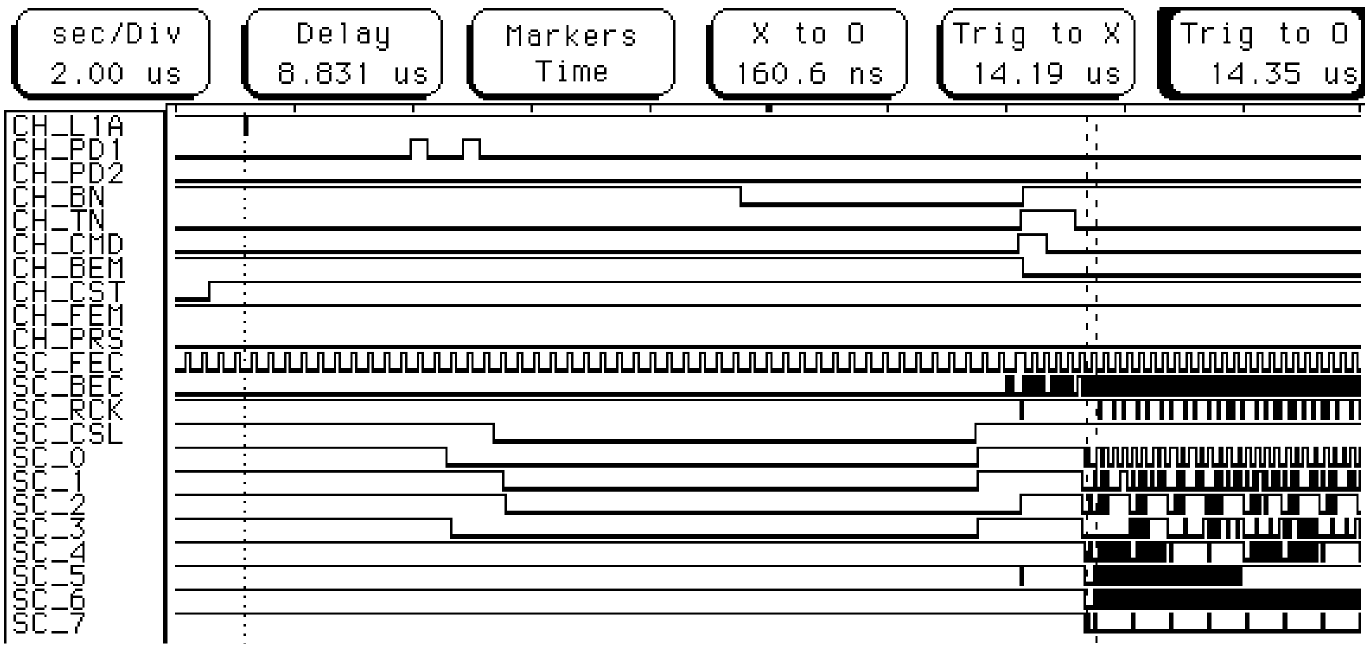


Figure B.6: XTL: Digitization.

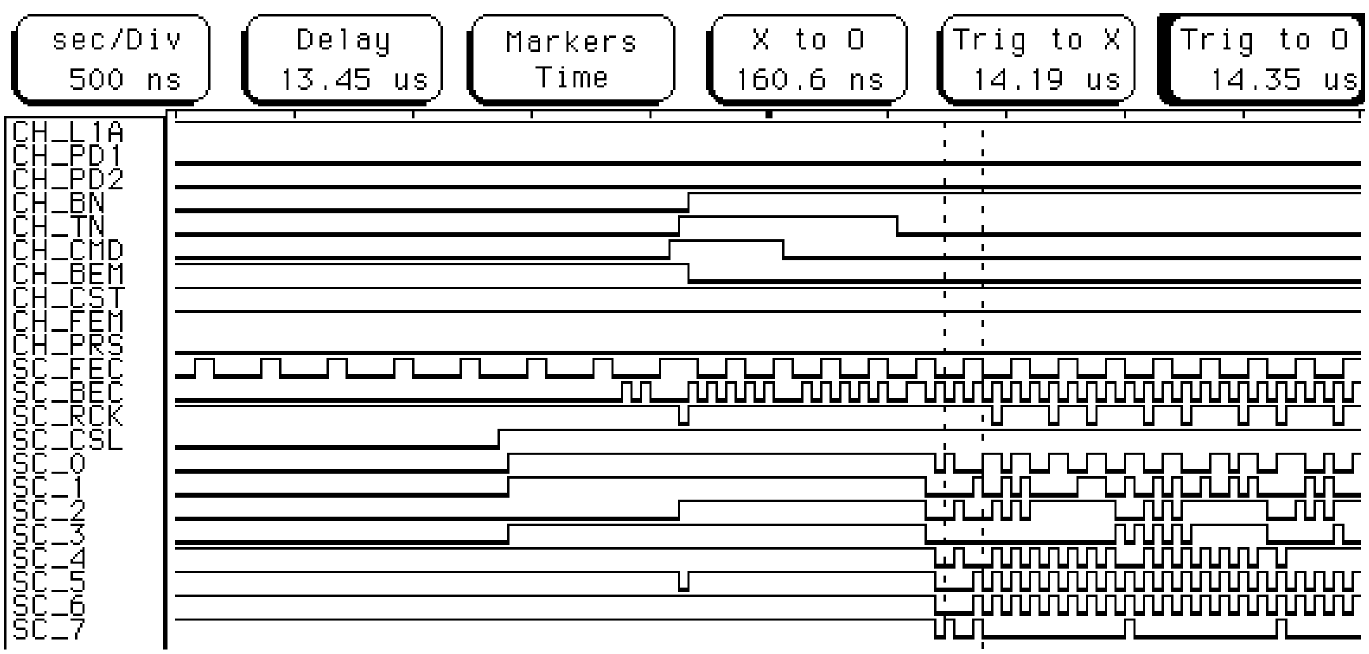


Figure B.7: XTL: End of Digitization, Start of Readout.

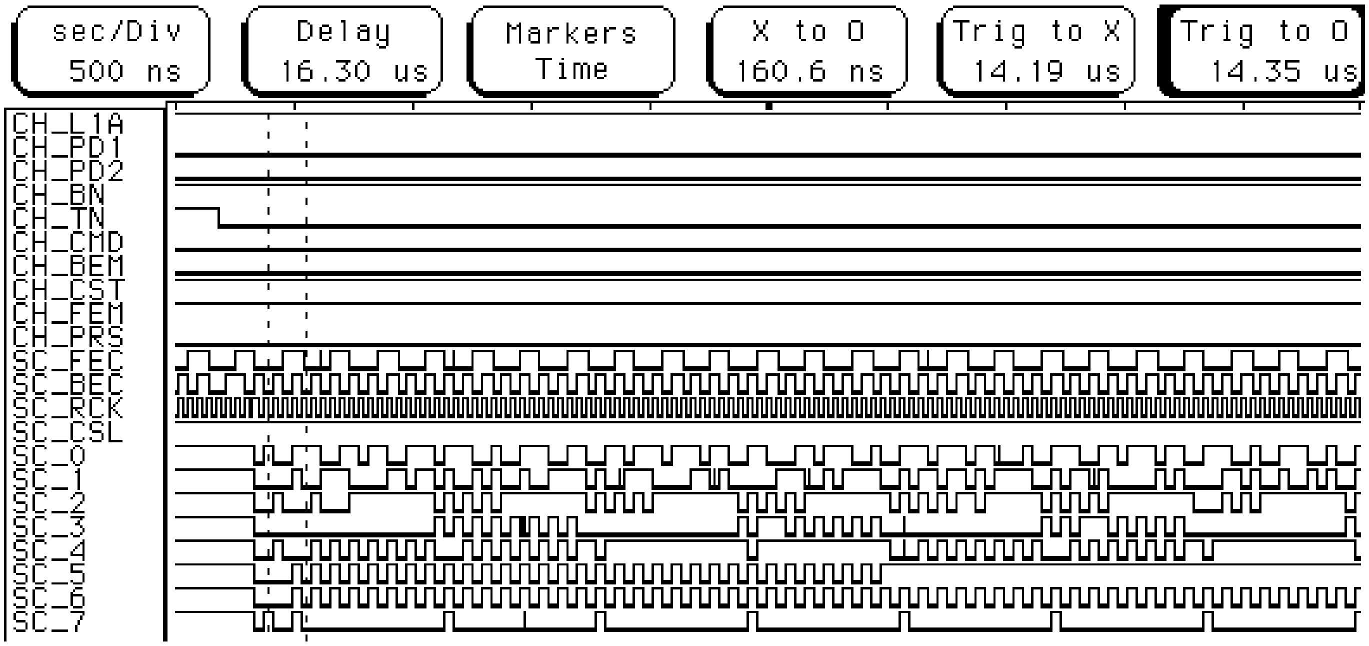


Figure B.8: XTL: Beginning of Data Readout.

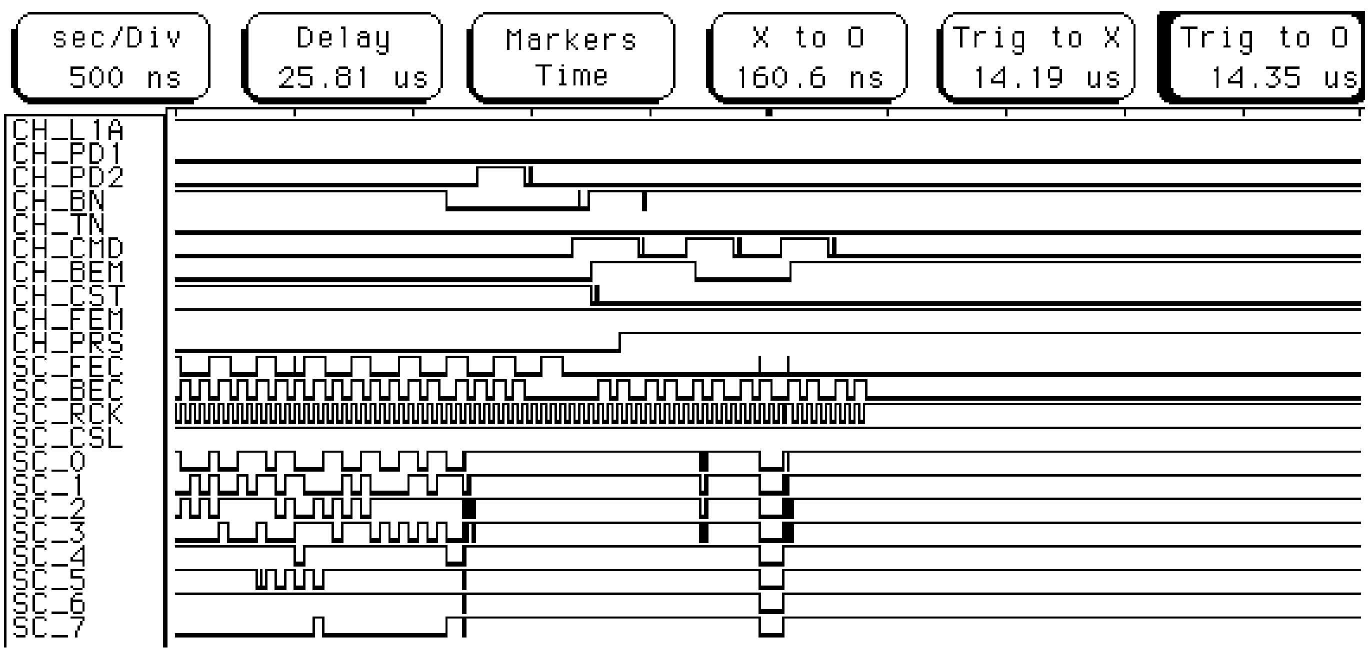


Figure B.9: XTL: End of Data Readout. **Note mini-digitize at end of sequence**

CALSR is issued while these are low. After this, the FECLK starts to run. There is no PRD2 as there is in the case of the XTL system. Thus, the reference pipeline cell is not reset and the first event is corrupted.

As for the XTL system, a CALSR is given before the L1AİIn this system the threshold and charge injection was not set so that TNBR and BNBR would fall during digitization. An item worth noting is that the data lines oscillate rapidly at the end of digitization and before readout begins. They are not being specified by the Stimulus system.

The PRD2 is issued after the BEMODE is strobed in by the change mode. The preamp reset comes at the end of the readout and is only high for a short time. This is more like the realistic way to work.

The BECLK is running during the digitization for the stimulus system but not for the XTL system.

The preamp reset detail is shown in Figure B.12. As was mentioned above this comes at the end of readout rather than at the start and the preamp reset line is only held high for a short time. In fact, it is during this time that a "mini digitization" also occurs.

The start of the sequence measured in Figure B.13 does not show the complicated FECLK structure that is visible for XTL in Figure B.4. Differences in the other lines have already been noted.

The Level 1 accept portion of the sequence is detailed in Figure B.14. There is only one pulse but it does fit between two front end clocks. This is consistent with the specification indicated in Figure 2.17 and Table 2.5 of §2.3.4 The CALSR signal comes earlier than that in the XTL system.

The start of digitization measurement is shown in Figure B.15. The control signals come in the same order as for the XTL system; however, the RREF-SEL transition occurs during the second PRD1 and CNTR-RST occurs much closer to the rising edge of the second PRD1ṪThe CNTR-RST is specified in Figure 2.19 to come last, but it is coming first. COMP-RST should come first and before the second PRD1 but it is coming after the second PRD1.

In Figure B.16 the PRD2 signal comes just before the readout begins, in stark contrast to the PRD2 coming at the start of sequence for XTL as seen in Figure B.4. The TNBR and BNBR lines are already high and the setting of the four BUS lines, BUS0–BUS3 is not done for BUS1–BUS3 but BUS0 is raised.**So what are the rules?**.

The beginning of readout is shown in Figure B.17. A PRD2 is issued just before readout begins, refreshing the reference pipeline cell. The BUS0–BUS7 lines are left in an undetermined state until the chip begins to place data on them. The BECLK is started when TNBR drops and readout begins whereas in the stimulus system the BECLK was already running. During readout the BECLK runs four times faster than the FECLK instead of two times. **Why doesn't he get crap because TNBR drops when there is still stuff? Is he using OBDV ? How critical then is that timing?**. The OBDV signal is clearly out of phase by one half cycle with respect to FECLKṪThis is used to clock the data into the buffer and remove the sensitivity of setting up timing in clocking in the data relative to the drop of TNBRṪThis is to be used in the future in the XTL system as well.

The measurement of the timing at the end of data readout is shown in Figure B.18. PRD2 is not sent at this time as it was for the XTL system. BEMODE is simply set high and not raised and lowered as in the XTL system. There is a mini digitization although the number of BEMODE pulses is larger.

The bus lines are left floating in the stimulus system.

B.5 Measurements on DAQ

In this section, the DAQ is compared to the XTL and Stimulus systems as well as the specification. In this system, the differential signals are picked up at the Transition Module. This comes before the Port card. Thus, measurements on DAQ lack the command line resets that are on BUS0–BUS3 because these are sent as commands to the Port Card which decodes them and sends them to the chip. Chip MM12 was used for these measurements.

The full sequence of readout is shown in Figure B.19. Since the FECLK runs continuously in this system, there is no burst, hence no start of burst. The L1A is the first signal and the two PRD1ś follow after this. TNBR is raised in the DAQ, whereas it is already high in the Stimulus and left low in the XTL system. The BECLK runs during digitization as it does for the Stimulus system. As mentioned above, it is invisible in the XTL system because it is taken directly from the raw clock, as indicated by the clock select line being low. As is the case for the Stimulus system, PRD2 goes high and low after digitization but before the readout starts. This is different from what is in the XTL system. As in both other systems, the BECLK runs for a short time after the readout is complete, doing the "mini digitization".

The preamp reset detail for the DAQ is shown in Figure B.20. As for the XTL, and in contrast with the Stimulus system, the preamp reset occurs before the L1A. It is seven FECLK cycles long in the DAQ, whereas it is six FECLK cycles in the Stimulus and kept on between bursts in XTL.

The detail for L1A is shown for the DAQ in Figure B.21. As for the stimulus, and in contrast with the XTL system and the specification, there is only on pulse on level 1 accept. The detail for digitization in the DAQ is shown in in Figure B.22; however, the behaviour of the differential control signals on BUS0–BUS3 could not be measured. It is only worth noting that the data lines are stable after digitization, as they are for the XTL system but unlike the Stimulus system. The end of digitization and start of readout shown for the DAQ in Figure B.23 is the same as that for the other two systems examined thus far. The start of readout indicated in Figure B.24 for the DAQ, only differs from the other systems in that the BECLK runs seven time faster than the FECLK˙The ratio was 4:1 and 2:1 for the stimulus and XTL systems respectively. In the end of data readout shown for the DAQ in Figure B.25, there is a "mini digitization" as for the stimulus system but not with the complicated change mode structure of the XTL system. **We did not get the right scale at the tail end here so it needs another measurement**.

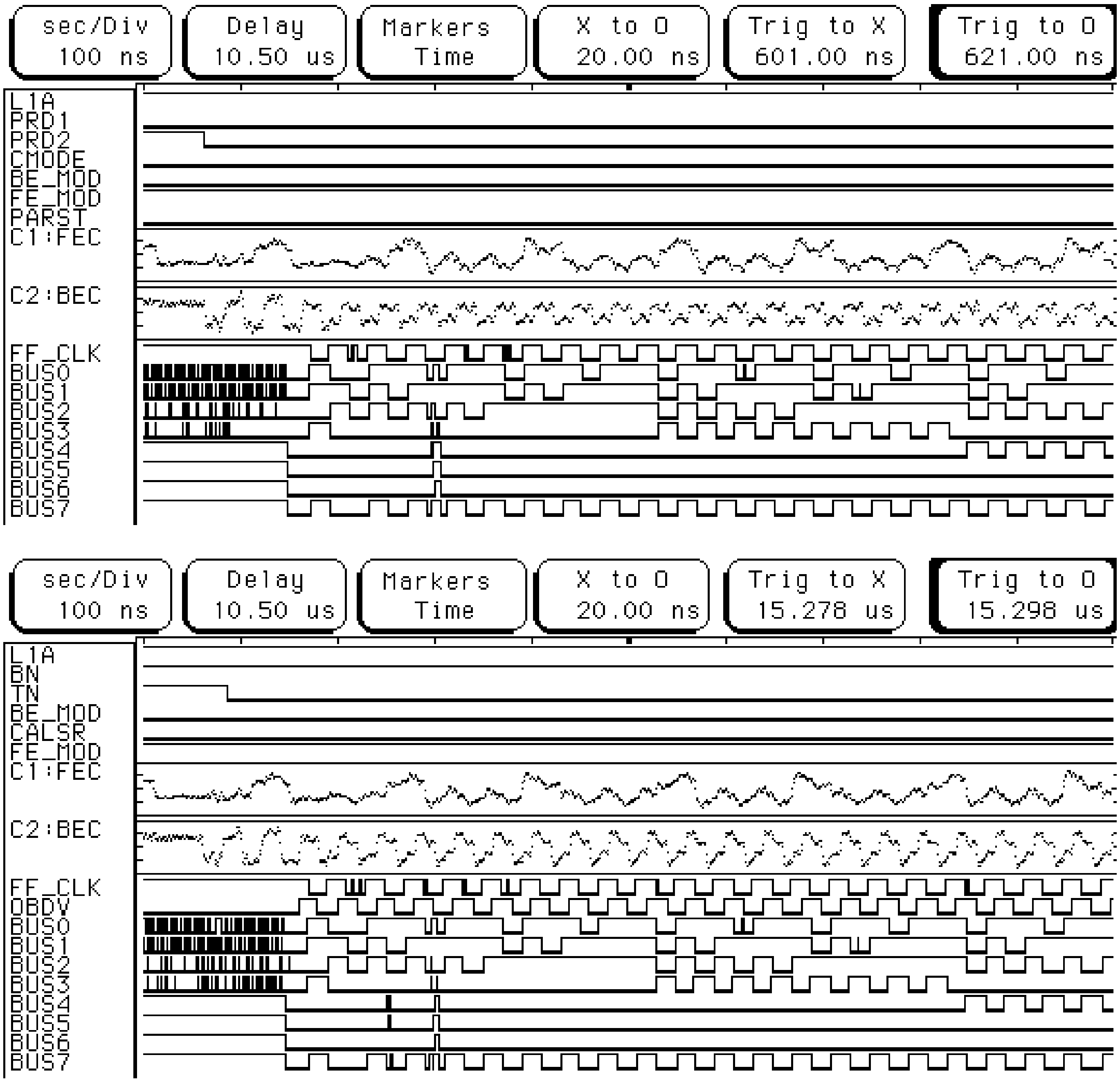


Figure B.10: Stimulus: Clock cycles.

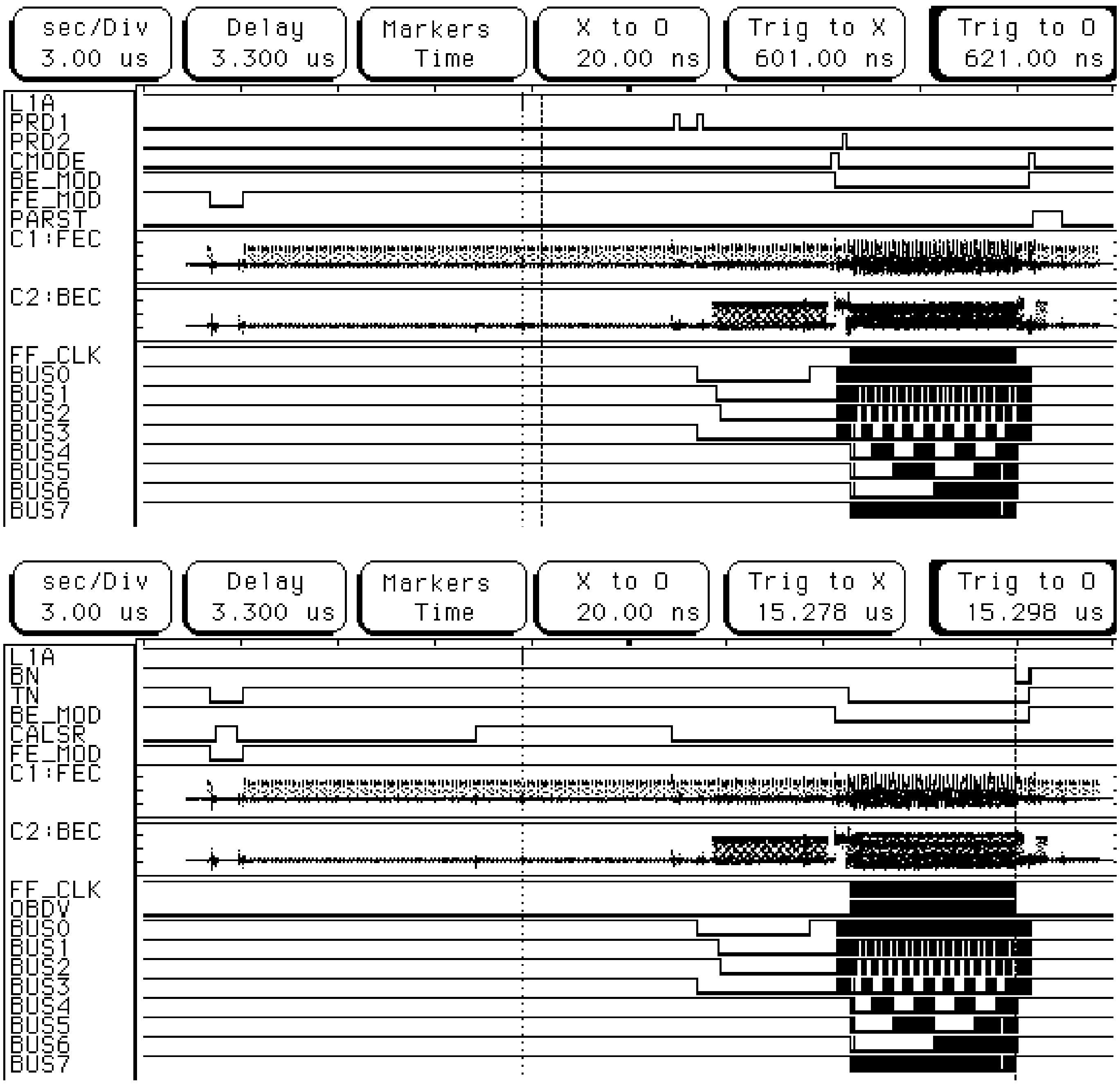


Figure B.11: Stimulus: Full Sequence.

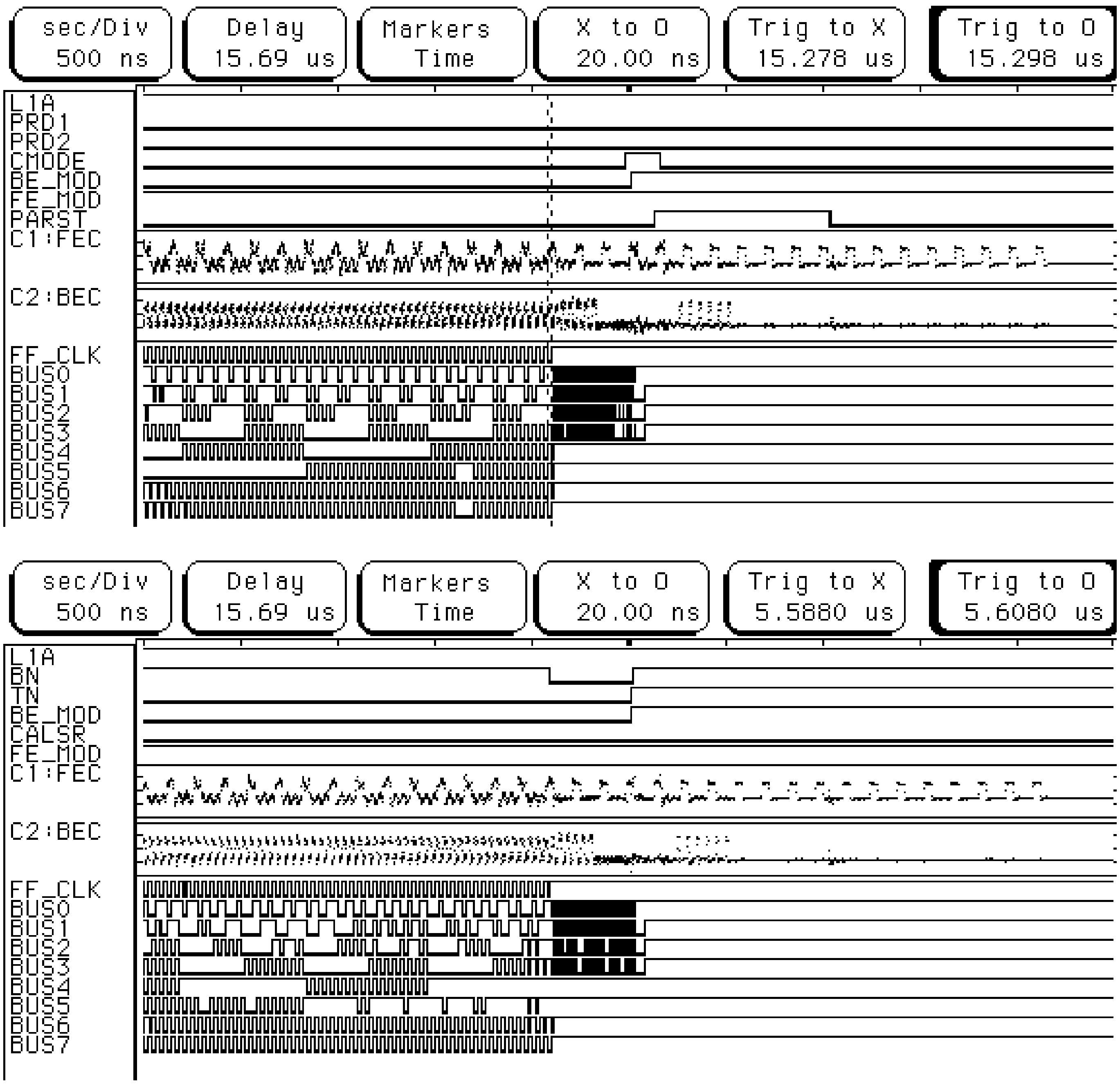


Figure B.12: Stimulus: Detail of Preamp Reset.

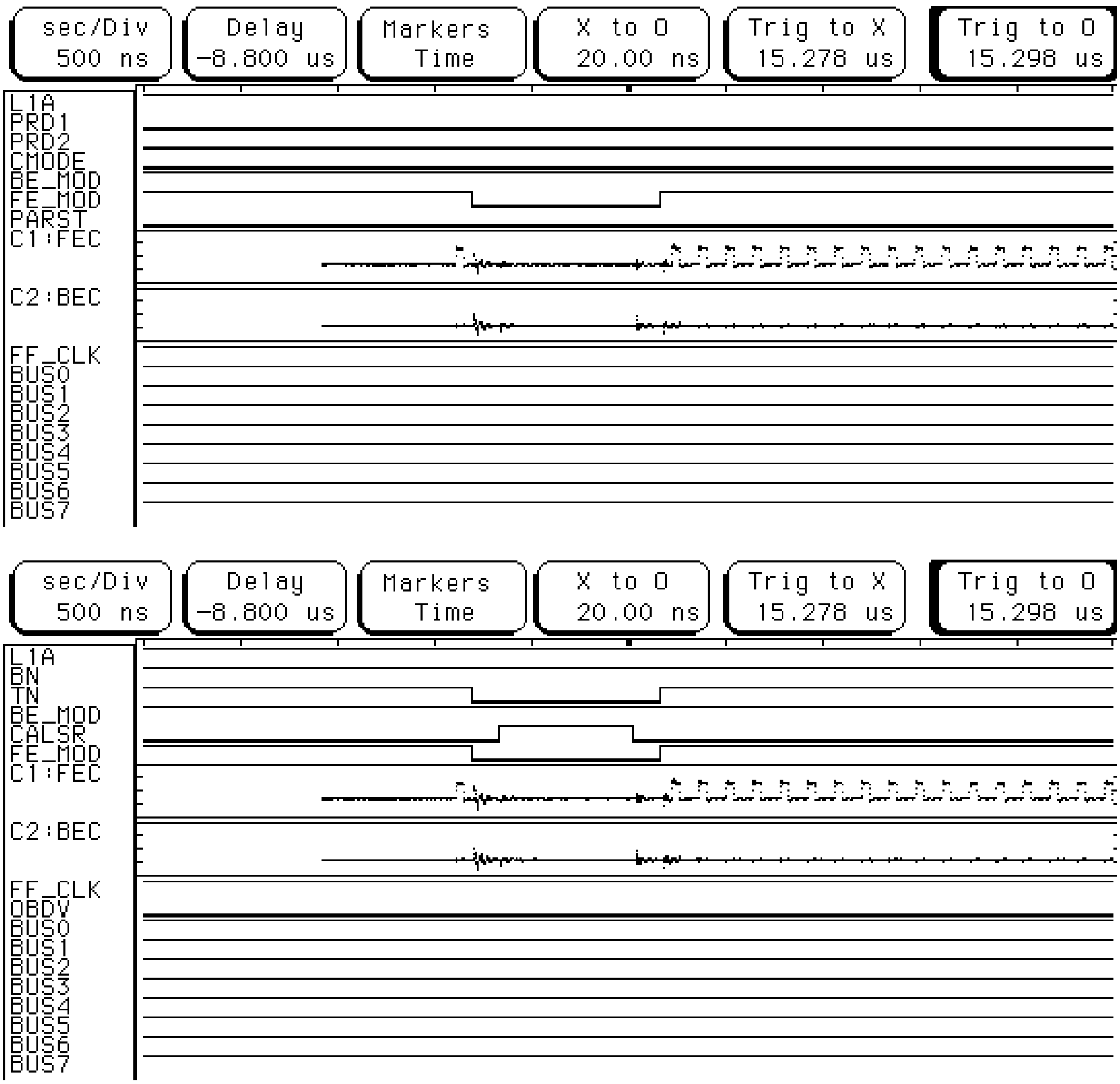


Figure B.13: Stimulus: Start of Sequence.

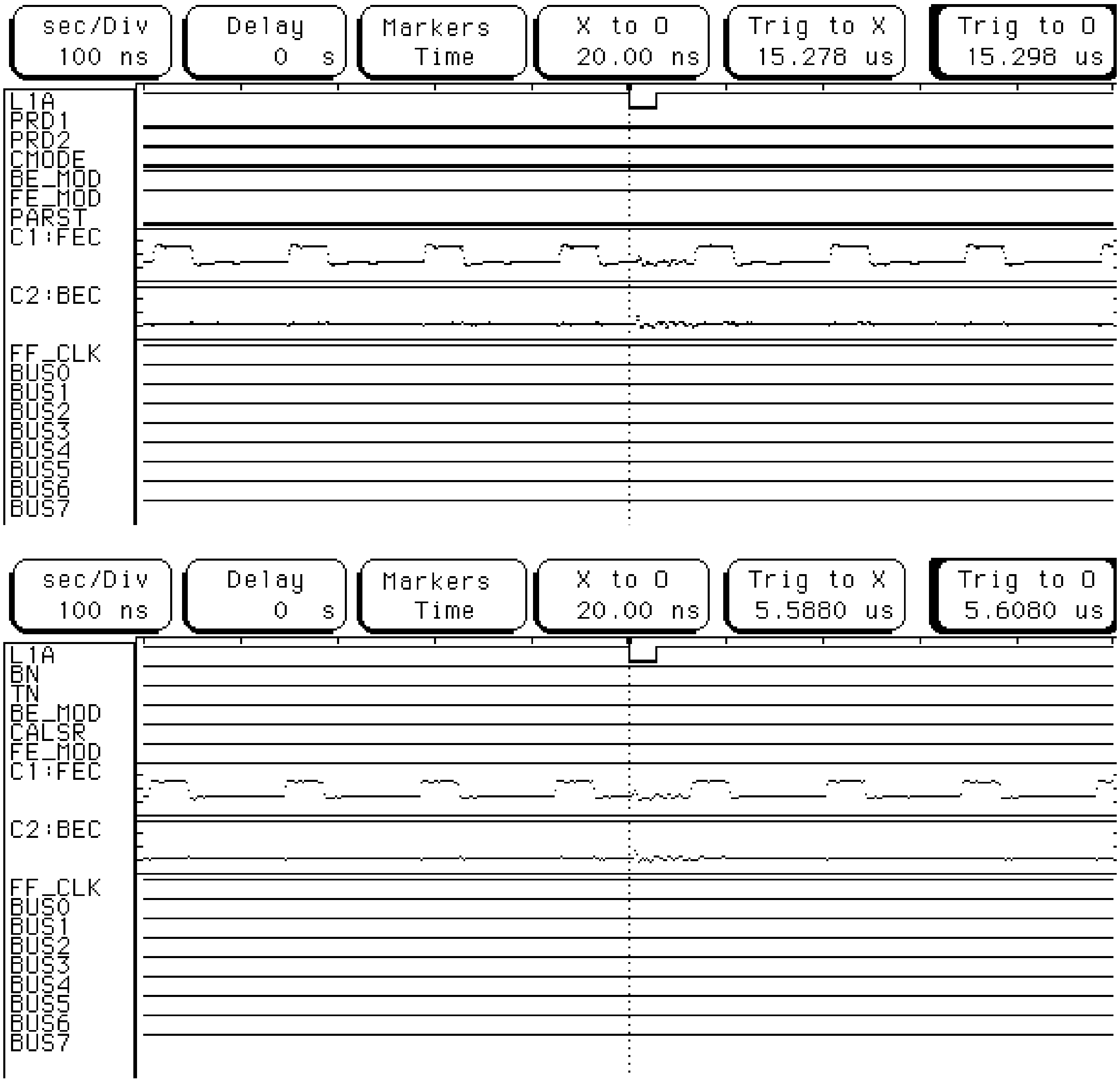


Figure B.14: Stimulus: Level 1 Accept.

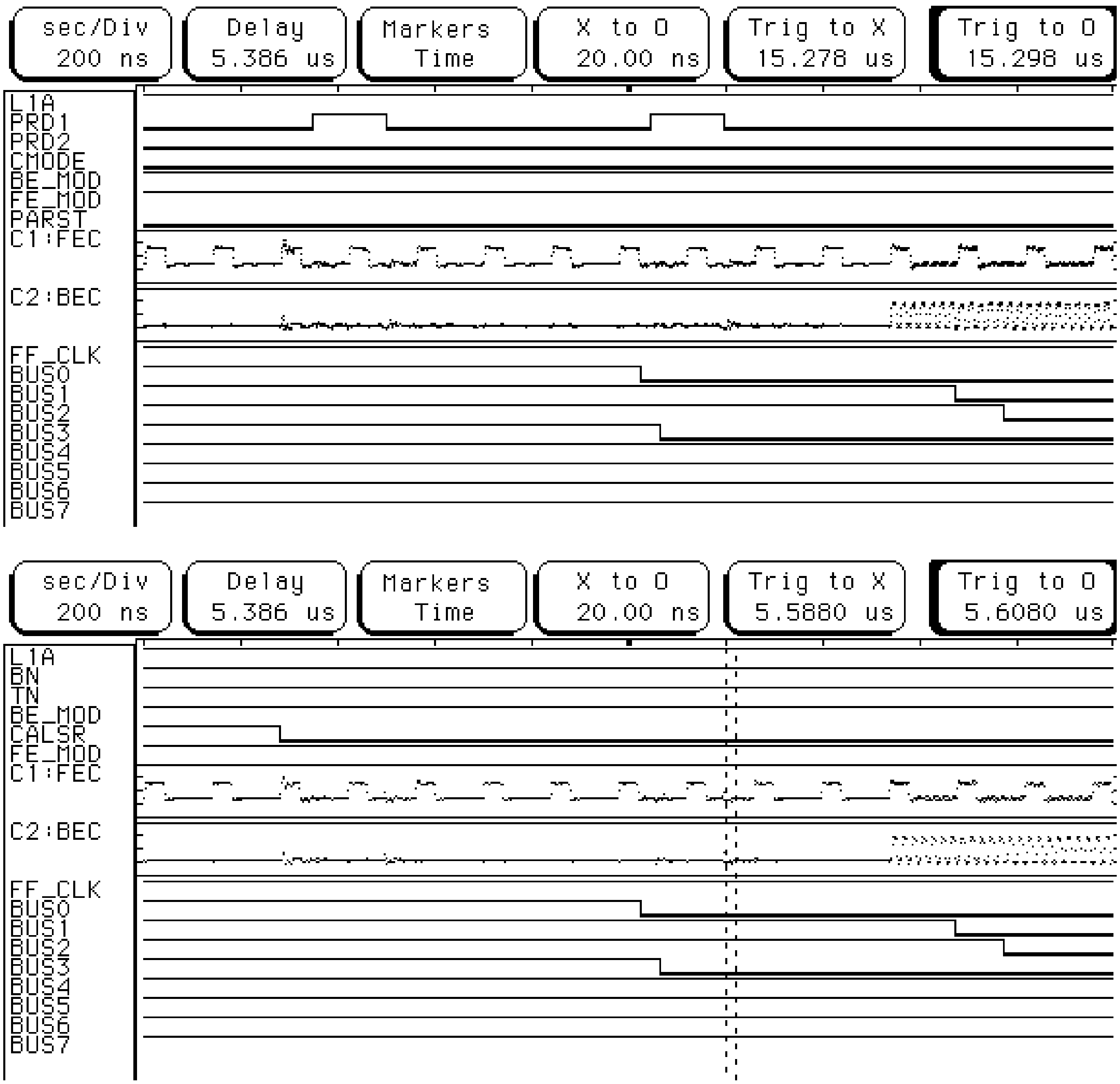


Figure B.15: Stimulus: Digitization.

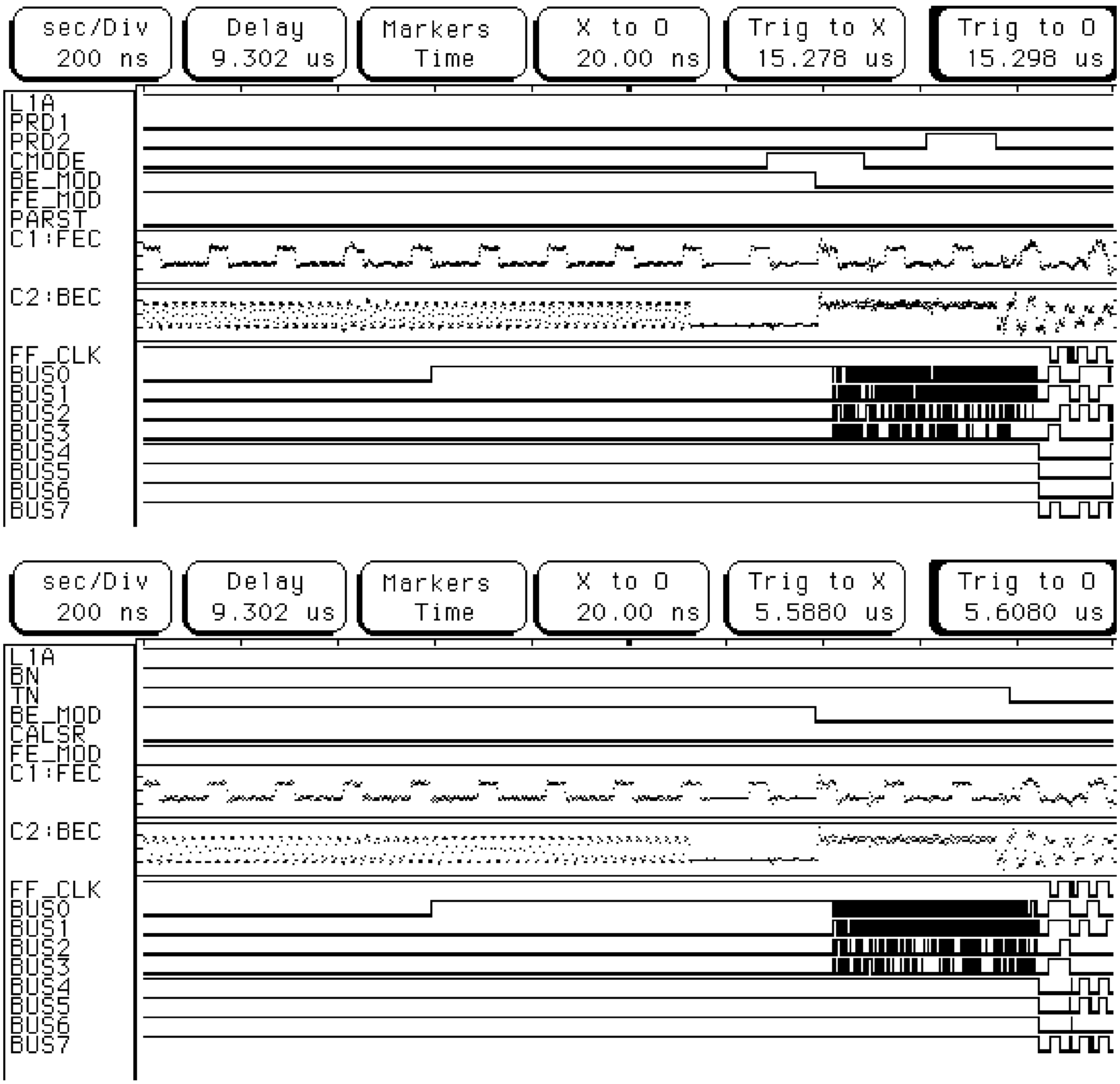


Figure B.16: Stimulus: End of Digitization, Start of Readout.

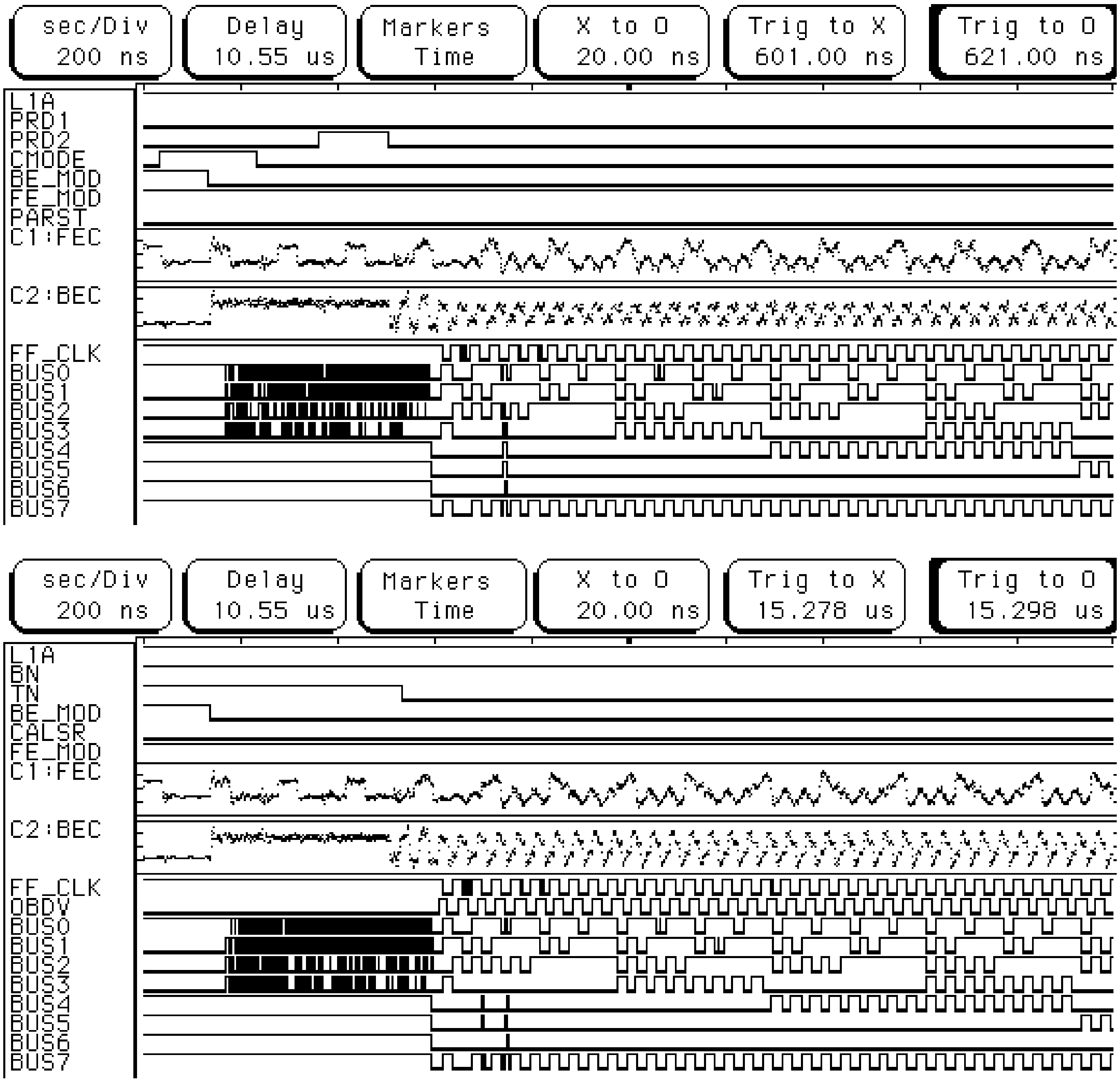


Figure B.17: Stimulus: Beginning of Data Readout.

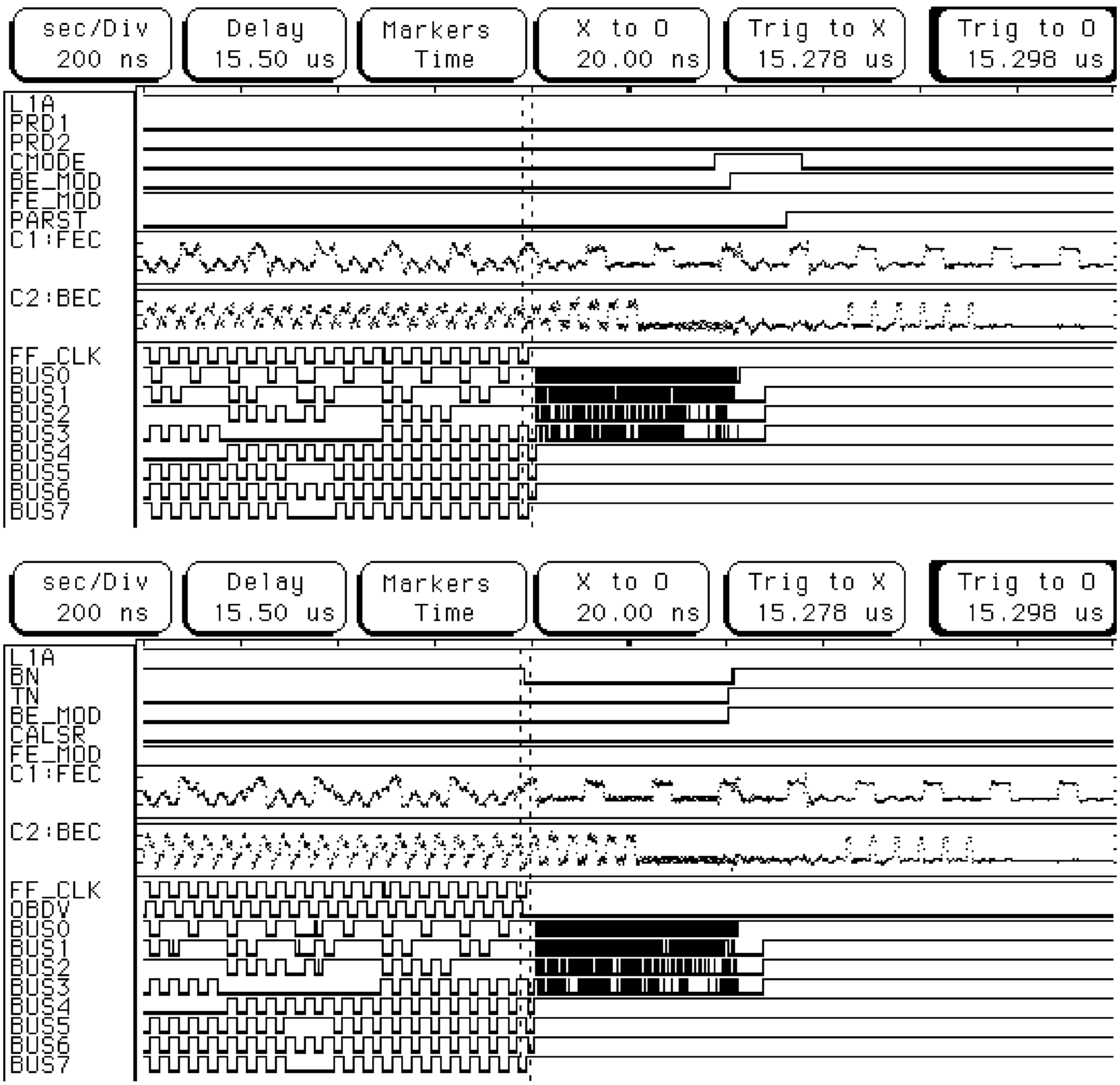


Figure B.18: Stimulus: End of Data Readout. **Note MiniDigitize at end of Sequence.**

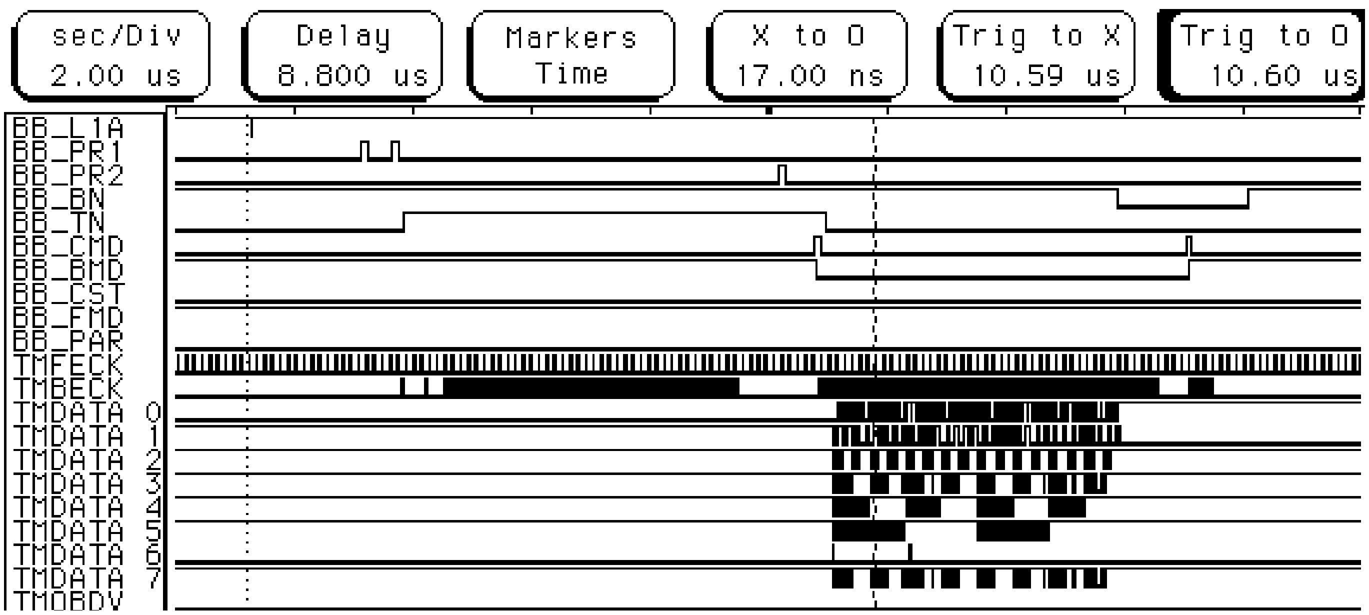


Figure B.19: DAQ: Full Sequence.

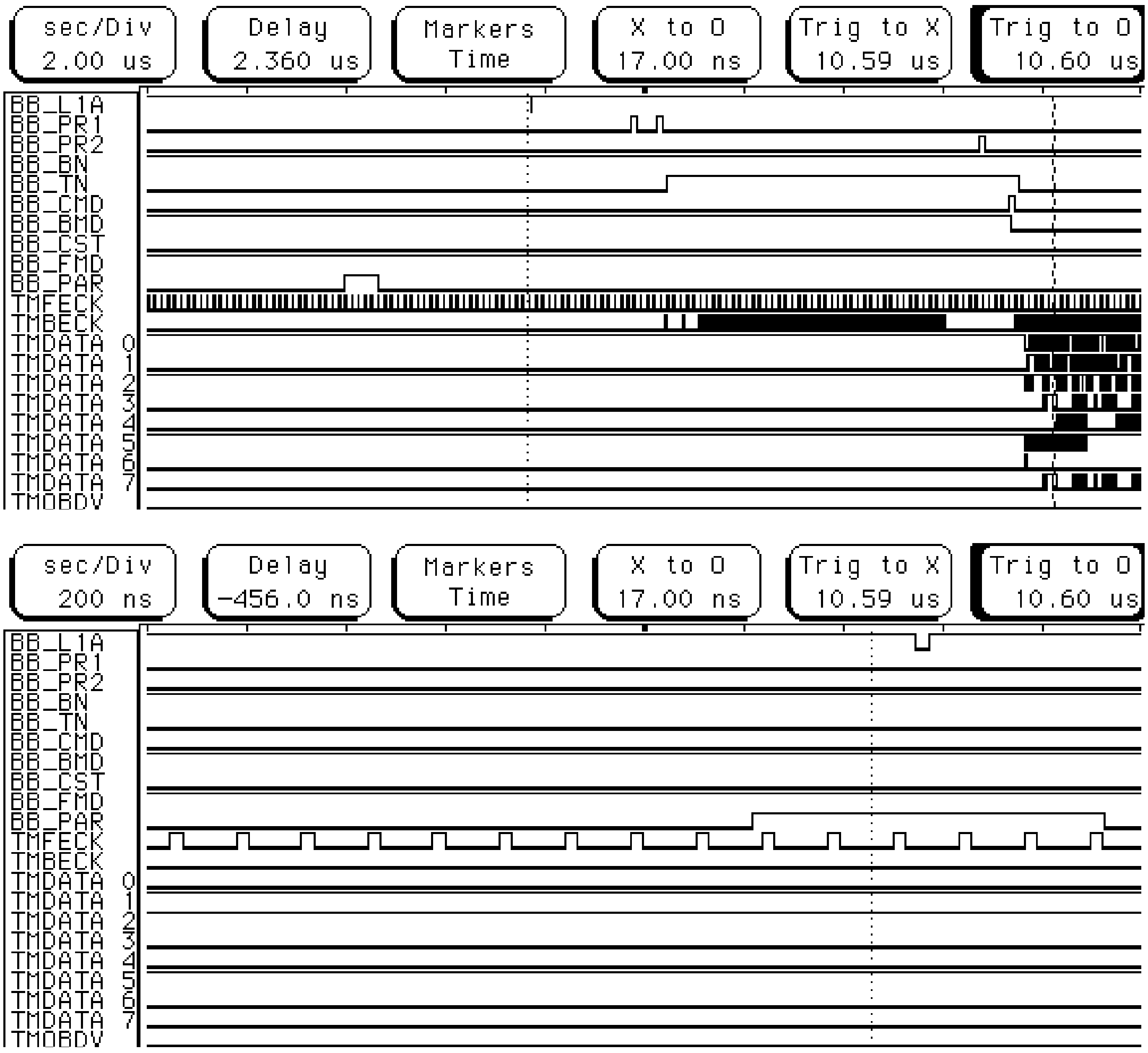


Figure B.20: DAQ: Detail of Preamp Reset.

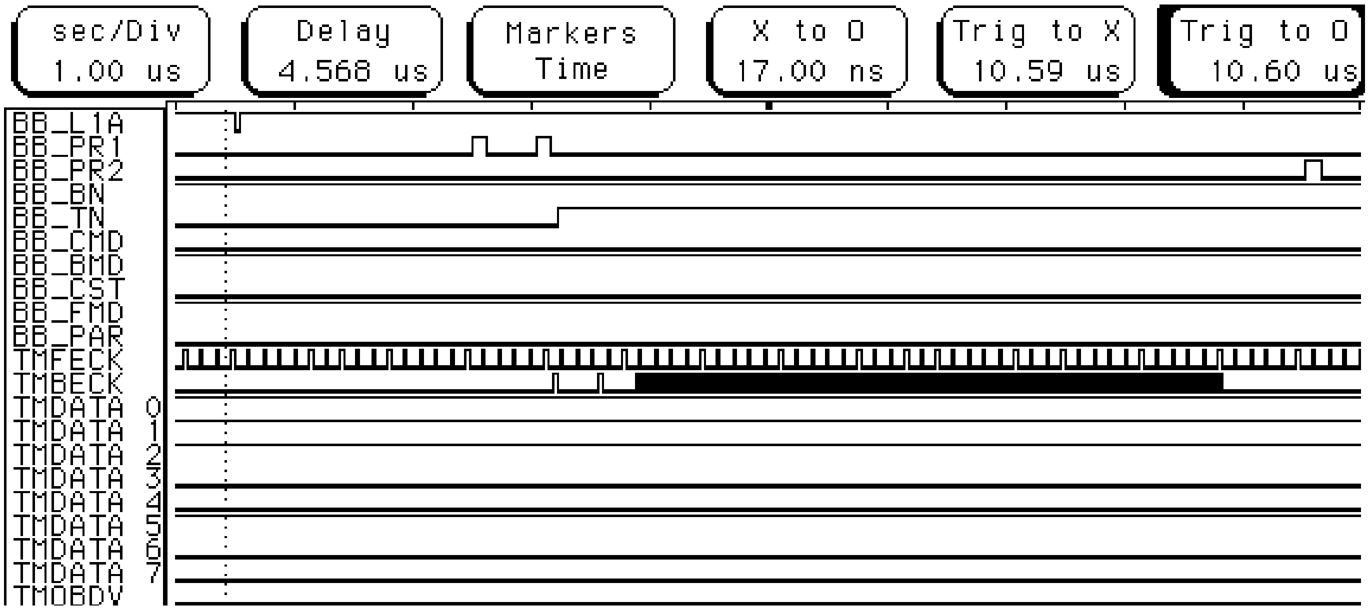


Figure B.21: DAQ: Level 1 Accept.

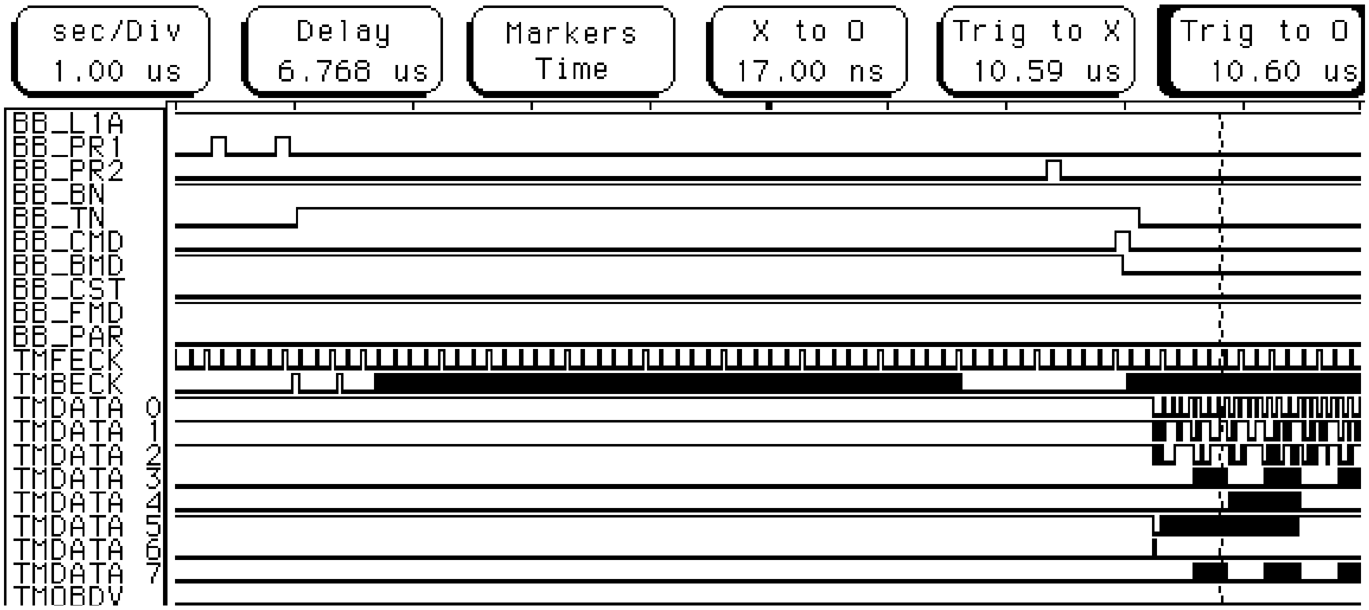


Figure B.22: DAQ: Digitization.

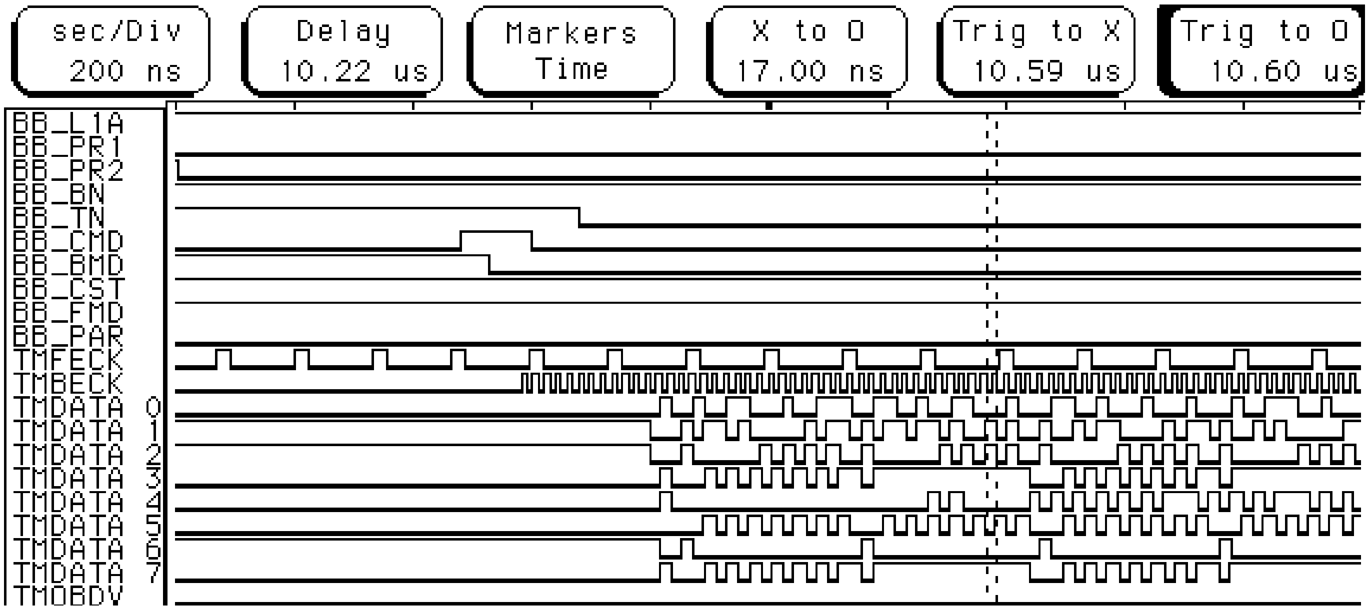


Figure B.23: DAQ: End of Digitization, Start of Readout.

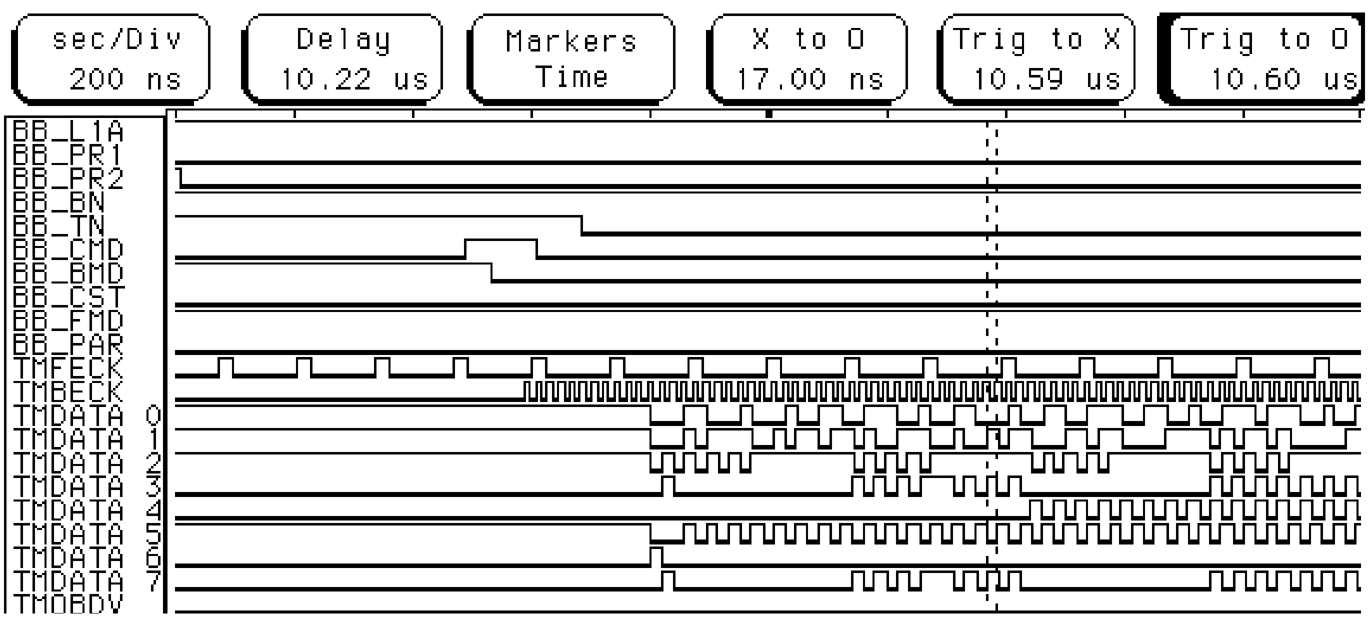


Figure B.24: DAQ: Beginning of Data Readout.

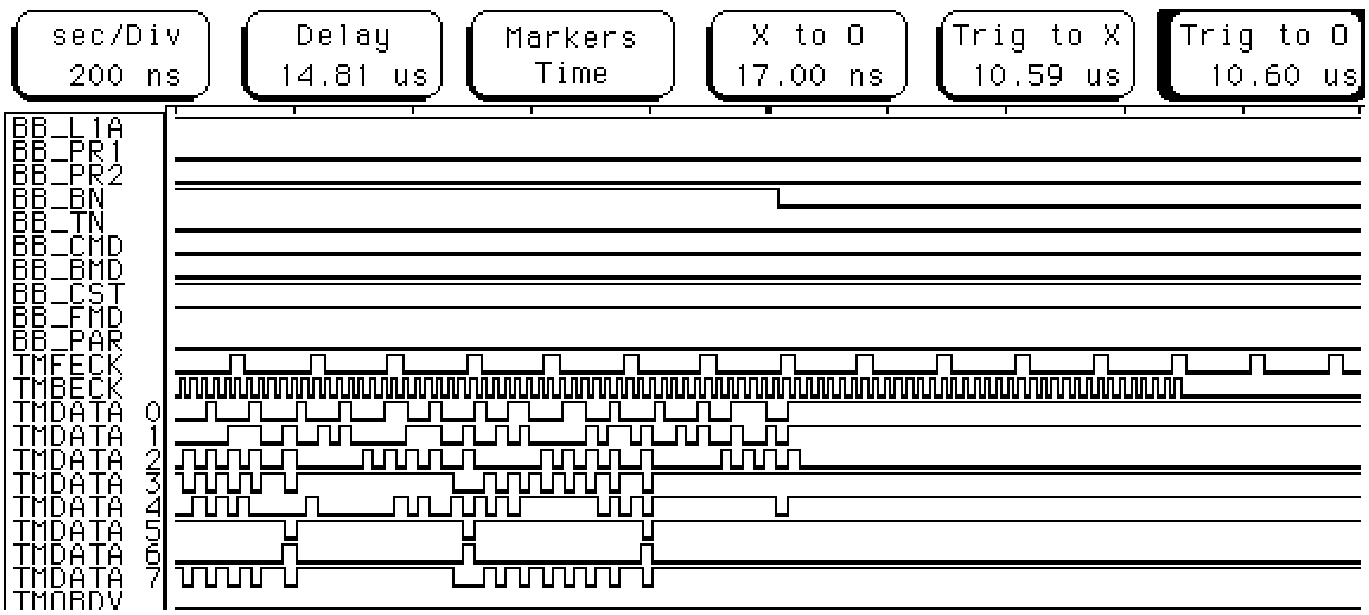


Figure B.25: DAQ: End of Data Readout.

Appendix C

Gray Code

Tables C.1 and C.2 contain lists of the gray code bits for numbers from 0 to 127 and 128 to 255 respectively. **need the Hex and Decimal versions if we take these as Binary**

0	0 0 0 0 0 0 0 0	32	0 0 1 1 0 0 0 0	64	0 1 1 0 0 0 0 0	96	0 1 0 1 0 0 0 0
1	0 0 0 0 0 0 0 1	33	0 0 1 1 0 0 0 1	65	0 1 1 0 0 0 0 1	97	0 1 0 1 0 0 0 1
2	0 0 0 0 0 0 1 1	34	0 0 1 1 0 0 1 1	66	0 1 1 0 0 0 1 1	98	0 1 0 1 0 0 1 1
3	0 0 0 0 0 0 1 0	35	0 0 1 1 0 0 1 0	67	0 1 1 0 0 0 1 0	99	0 1 0 1 0 0 1 0
4	0 0 0 0 0 1 1 0	36	0 0 1 1 0 1 1 0	68	0 1 1 0 0 1 1 0	100	0 1 0 1 0 1 1 0
5	0 0 0 0 0 1 1 1	37	0 0 1 1 0 1 1 1	69	0 1 1 0 0 1 1 1	101	0 1 0 1 0 1 1 1
6	0 0 0 0 0 1 0 1	38	0 0 1 1 0 1 0 1	70	0 1 1 0 0 1 0 1	102	0 1 0 1 0 1 0 1
7	0 0 0 0 0 1 0 0	39	0 0 1 1 0 1 0 0	71	0 1 1 0 0 1 0 0	103	0 1 0 1 0 1 0 0
8	0 0 0 0 1 1 0 0	40	0 0 1 1 1 1 0 0	72	0 1 1 0 1 1 0 0	104	0 1 0 1 1 1 0 0
9	0 0 0 0 1 1 0 1	41	0 0 1 1 1 1 0 1	73	0 1 1 0 1 1 0 1	105	0 1 0 1 1 1 0 1
10	0 0 0 0 1 1 1 1	42	0 0 1 1 1 1 1 1	74	0 1 1 0 1 1 1 1	106	0 1 0 1 1 1 1 1
11	0 0 0 0 1 1 1 0	43	0 0 1 1 1 1 1 0	75	0 1 1 0 1 1 1 0	107	0 1 0 1 1 1 1 0
12	0 0 0 0 1 0 1 0	44	0 0 1 1 1 0 1 0	76	0 1 1 0 1 0 1 0	108	0 1 0 1 1 0 1 0
13	0 0 0 0 1 0 1 1	45	0 0 1 1 1 0 1 1	77	0 1 1 0 1 0 1 1	109	0 1 0 1 1 0 1 1
14	0 0 0 0 1 0 0 1	46	0 0 1 1 1 0 0 1	78	0 1 1 0 1 0 0 1	110	0 1 0 1 1 0 0 1
15	0 0 0 0 1 0 0 0	47	0 0 1 1 1 0 0 0	79	0 1 1 0 1 0 0 0	111	0 1 0 1 1 0 0 0
16	0 0 0 1 1 0 0 0	48	0 0 1 0 1 0 0 0	80	0 1 1 1 1 0 0 0	112	0 1 0 0 1 0 0 0
17	0 0 0 1 1 0 0 1	49	0 0 1 0 1 0 0 1	81	0 1 1 1 1 0 0 1	113	0 1 0 0 1 0 0 1
18	0 0 0 1 1 0 1 1	50	0 0 1 0 1 0 1 1	82	0 1 1 1 1 0 1 1	114	0 1 0 0 1 0 1 1
19	0 0 0 1 1 0 1 0	51	0 0 1 0 1 0 1 0	83	0 1 1 1 1 0 1 0	115	0 1 0 0 1 0 1 0
20	0 0 0 1 1 1 1 0	52	0 0 1 0 1 1 1 0	84	0 1 1 1 1 1 1 0	116	0 1 0 0 1 1 1 0
21	0 0 0 1 1 1 1 1	53	0 0 1 0 1 1 1 1	85	0 1 1 1 1 1 1 1	117	0 1 0 0 1 1 1 1
22	0 0 0 1 1 1 0 1	54	0 0 1 0 1 1 0 1	86	0 1 1 1 1 1 0 1	118	0 1 0 0 1 1 0 1
23	0 0 0 1 1 1 0 0	55	0 0 1 0 1 1 0 0	87	0 1 1 1 1 1 0 0	119	0 1 0 0 1 1 0 0
24	0 0 0 1 0 1 0 0	56	0 0 1 0 0 1 0 0	88	0 1 1 1 0 1 0 0	120	0 1 0 0 0 1 0 0
25	0 0 0 1 0 1 0 1	57	0 0 1 0 0 1 0 1	89	0 1 1 1 0 1 0 1	121	0 1 0 0 0 1 0 1
26	0 0 0 1 0 1 1 1	58	0 0 1 0 0 1 1 1	90	0 1 1 1 0 1 1 1	122	0 1 0 0 0 1 1 1
27	0 0 0 1 0 1 1 0	59	0 0 1 0 0 1 1 0	91	0 1 1 1 0 1 1 0	123	0 1 0 0 0 1 1 0
28	0 0 0 1 0 0 1 0	60	0 0 1 0 0 0 1 0	92	0 1 1 1 0 0 1 0	124	0 1 0 0 0 0 1 0
29	0 0 0 1 0 0 1 1	61	0 0 1 0 0 0 1 1	93	0 1 1 1 0 0 1 1	125	0 1 0 0 0 0 1 1
30	0 0 0 1 0 0 0 1	62	0 0 1 0 0 0 0 1	94	0 1 1 1 0 0 0 1	126	0 1 0 0 0 0 0 1
31	0 0 0 1 0 0 0 0	63	0 0 1 0 0 0 0 0	95	0 1 1 1 0 0 0 0	127	0 1 0 0 0 0 0 0

Table C.1: Gray Code bit patterns for the numbers 0–127.

128	1 1 0 0 0 0 0 0	160	1 1 1 1 0 0 0 0	192	1 0 1 0 0 0 0 0	224	1 0 0 1 0 0 0 0
129	1 1 0 0 0 0 0 1	161	1 1 1 1 0 0 0 1	193	1 0 1 0 0 0 0 1	225	1 0 0 1 0 0 0 1
130	1 1 0 0 0 0 1 1	162	1 1 1 1 0 0 1 1	194	1 0 1 0 0 0 1 1	226	1 0 0 1 0 0 1 1
131	1 1 0 0 0 0 1 0	163	1 1 1 1 0 0 1 0	195	1 0 1 0 0 0 1 0	227	1 0 0 1 0 0 1 0
132	1 1 0 0 0 1 1 0	164	1 1 1 1 0 1 1 0	196	1 0 1 0 0 1 1 0	228	1 0 0 1 0 1 1 0
133	1 1 0 0 0 1 1 1	165	1 1 1 1 0 1 1 1	197	1 0 1 0 0 1 1 1	229	1 0 0 1 0 1 1 1
134	1 1 0 0 0 1 0 1	166	1 1 1 1 0 1 0 1	198	1 0 1 0 0 1 0 1	230	1 0 0 1 0 1 0 1
135	1 1 0 0 0 1 0 0	167	1 1 1 1 0 1 0 0	199	1 0 1 0 0 1 0 0	231	1 0 0 1 0 1 0 0
136	1 1 0 0 1 1 0 0	168	1 1 1 1 1 1 0 0	200	1 0 1 0 1 1 0 0	232	1 0 0 1 1 1 0 0
137	1 1 0 0 1 1 0 1	169	1 1 1 1 1 1 0 1	201	1 0 1 0 1 1 0 1	233	1 0 0 1 1 1 0 1
138	1 1 0 0 1 1 1 1	170	1 1 1 1 1 1 1 1	202	1 0 1 0 1 1 1 1	234	1 0 0 1 1 1 1 1
139	1 1 0 0 1 1 1 0	171	1 1 1 1 1 1 1 0	203	1 0 1 0 1 1 1 0	235	1 0 0 1 1 1 1 0
140	1 1 0 0 1 0 1 0	172	1 1 1 1 1 0 1 0	204	1 0 1 0 1 0 1 0	236	1 0 0 1 1 0 1 0
141	1 1 0 0 1 0 1 1	173	1 1 1 1 1 0 1 1	205	1 0 1 0 1 0 1 1	237	1 0 0 1 1 0 1 1
142	1 1 0 0 1 0 0 1	174	1 1 1 1 1 0 0 1	206	1 0 1 0 1 0 0 1	238	1 0 0 1 1 0 0 1
143	1 1 0 0 1 0 0 0	175	1 1 1 1 1 0 0 0	207	1 0 1 0 1 0 0 0	239	1 0 0 1 1 0 0 0
144	1 1 0 1 1 0 0 0	176	1 1 1 0 1 0 0 0	208	1 0 1 1 1 0 0 0	240	1 0 0 0 1 0 0 0
145	1 1 0 1 1 0 0 1	177	1 1 1 0 1 0 0 1	209	1 0 1 1 1 0 0 1	241	1 0 0 0 1 0 0 1
146	1 1 0 1 1 0 1 1	178	1 1 1 0 1 0 1 1	210	1 0 1 1 1 0 1 1	242	1 0 0 0 1 0 1 1
147	1 1 0 1 1 0 1 0	179	1 1 1 0 1 0 1 0	211	1 0 1 1 1 0 1 0	243	1 0 0 0 1 0 1 0
148	1 1 0 1 1 1 1 0	180	1 1 1 0 1 1 1 0	212	1 0 1 1 1 1 1 0	244	1 0 0 0 1 1 1 0
149	1 1 0 1 1 1 1 1	181	1 1 1 0 1 1 1 1	213	1 0 1 1 1 1 1 1	245	1 0 0 0 1 1 1 1
150	1 1 0 1 1 1 0 1	182	1 1 1 0 1 1 0 1	214	1 0 1 1 1 1 0 1	246	1 0 0 0 1 1 0 1
151	1 1 0 1 1 1 0 0	183	1 1 1 0 1 1 0 0	215	1 0 1 1 1 1 0 0	247	1 0 0 0 1 1 0 0
152	1 1 0 1 0 1 0 0	184	1 1 1 0 0 1 0 0	216	1 0 1 1 0 1 0 0	248	1 0 0 0 0 1 0 0
153	1 1 0 1 0 1 0 1	185	1 1 1 0 0 1 0 1	217	1 0 1 1 0 1 0 1	249	1 0 0 0 0 1 0 1
154	1 1 0 1 0 1 1 1	186	1 1 1 0 0 1 1 1	218	1 0 1 1 0 1 1 1	250	1 0 0 0 0 1 1 1
155	1 1 0 1 0 1 1 0	187	1 1 1 0 0 1 1 0	219	1 0 1 1 0 1 1 0	251	1 0 0 0 0 1 1 0
156	1 1 0 1 0 0 1 0	188	1 1 1 0 0 0 1 0	220	1 0 1 1 0 0 1 0	252	1 0 0 0 0 0 1 0
157	1 1 0 1 0 0 1 1	189	1 1 1 0 0 0 1 1	221	1 0 1 1 0 0 1 1	253	1 0 0 0 0 0 1 1
158	1 1 0 1 0 0 0 1	190	1 1 1 0 0 0 0 1	222	1 0 1 1 0 0 0 1	254	1 0 0 0 0 0 0 1
159	1 1 0 1 0 0 0 0	191	1 1 1 0 0 0 0 0	223	1 0 1 1 0 0 0 0	255	1 0 0 0 0 0 0 0

Table C.2: Gray Code bit patterns for the numbers 128–255.

Bibliography

[1] R. Yarema *et.al.*, A Beginner's Guide to the SVXIIE, revised FERMILAB-TM-1892 D0

[2] R. Strohmeir and W. Knopf SVX3 Device Specifications, ESE-SVX-950703, http://www-ese.fnal.gov/eseproj/svx/svx3/svx3spec.html

[3] S. Kleinfelder, "The LBL Silicon Vertex Detector Readout Integrated Circuit: An Introduction." Lawrence Berkeley Laboratory, November 16, 1986

[4] S. Kleinfelder, *et.al.*, "A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout." IEEE Transactions on Nuclear Science, Vol.35, No.1, February 1988, pp.171 - 175.

[5] C. Haber, "The SVX IC: A 128 Channel Charge Amplifier with Sparse Scan." Proceedings of the Workshops on Particle Identification, Fermilab, April, 1989.

[6] T. Zimmerman, *et. al.*, "Design of an Advanced Readout Chip for Silicon Strip Detectors." IEEE Transactions on Nuclear Science, Vol.40, No.4. August 1993, pp. 736-739.

[7] T. Zimmerman, *et. al.*, "SVXII Analog Pipeline Signals and Operation." Fermi National Accelerator Laboratory, April 4, 1993.

[8] L.Luo,*et. al.*, "SVXII ADC Counter and R-S Latch Introduction." Lawrence Berkeley Laboratory, Berkeley, California.

[9] L.Luo, *et. al.*, "SVXII Sparse Readout Circuit Introduction." Lawrence Berkeley Laboratory, Berkeley, California.

[10] T. Zimmerman, SVX3: A deadtimeless readout chip for silicon strip detectors The Use of low resistivity substrates for optimal noise reduction, ground referencing, and current conduction in mixed signal ASICs, Fermilab TM, TM-2035.

[11] T. Zimmerman, *et. al.*, SVX3: A deadtimeless readout chip for silicon strip detectors Nuclear Instruments and Methods in Physics Research A 409 (1998) 369-374

[12] M. Garcia-Sciveres, *et. al.*, The SVX3D Integrated Circuit for Deadtimeless Silicon Strip Readout CDF Note 4851, contributed paper to Vertex '98, to appear in NIM A

[13] M. Rehn, *et. al.*, Statistical Study of SVX3D Chip Dynamic Pedestal Subtraction Threshold Level CDF Note 4852