IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH, Plaintiffs, v. RAMBUS INC., Defendant.	No. CV-00-20905 RMW ORDER DENYING RAMBUS'S MOTION FOR SUMMARY JUDGMENT OF INFRINGEMENT RELATING TO "DELAY LOCKED LOOP" **[Re Docket No. 1020]**

Rambus seeks summary judgment that the Double Data Rate Synchronous Dynamic Random Access Memory ("DDR SDRAM") devices of Hynix[1] infringe claim 33 of U.S. Patent No. 6,034,918 ("the '918 patent"), claim 38 of U.S. Patent No. 6,324,120 ("the '120 patent"), claim 40 of U.S. Patent No. 6,426,916 ("the '916 patent"), and claim 34 of U.S. Patent No. 5,915,105 ("the '105 patent") (collectively "claims-at-issue"). The court has read the moving and responding papers and considered the arguments of counsel. For the reasons set forth below, the court DENIES summary adjudication that Hynix's accused devices contain elements covered by the "delay locked loop"

[1] Hynix designated product HY5DU2822T as a representative DDR SDRAM product accused by Rambus of infringement.

limitation. Rambus's assertion that the accused devices meet the agreed-upon construction of "delay locked loop" is subject to a material issue of fact and, therefore, summary judgment of infringement on claim 33 of U.S. Patent No. 6,034,918, claim 38 of U.S. Patent No. 6,324,120, claim 40 of U.S. Patent No. 6,426,916, and claim 34 of U.S. Patent No. 5,915,105 is DENIED.

I. BACKGROUND

On January 19, 2005, the court issued its Clarified and Corrected Order on Rambus's Motion for Summary Judgment of Infringement, ruling that Hynix's accused devices infringed several of Rambus's patents, including the claims-at-issue. Hynix failed to argue in response to Rambus's motion that its accused products did not meet the "delay locked loop" limitation. On January 24, 2005, Hynix moved for relief from the court's ruling. On February 11, 2005, prior to the court ruling on its motion for relief, Hynix moved for summary judgment that Rambus's patents are invalid for failure to meet the written description requirement with respect to the "delay locked loop" limitation. The court has denied Hynix's motion. *See* Order Denying Hynix's Motion for Summ. J. of Invalidity of Patent Claims Including "Delay Locked Loop."

The court granted Hynix's motion for relief on March 4, 2005 but permitted Rambus to move for summary judgment on claims including the "delay locked loop" limitation. Accordingly, on April 1, 2005, Rambus filed the present motion seeking summary judgment of infringement of claims including the "delay locked loop" limitation.

Rambus asserts that Hynix's DDR SDRAM devices infringe the '918, '120, '916 and '105 patents. The patents-at-issue in this motion descend from an original patent application filed on April 18, 1990 and contain essentially identical written descriptions. The issue raised in this motion is whether Hynix's accused DDR SDRAM products contain elements covered by the limitation "delay locked loop."

The parties have stipulated to the construction of the limitation here at issue. The parties' agreed construction of "delay locked loop" is:

> circuitry on the device, including a variable delay line, that uses feedback to adjust the amount of delay of the variable delay line and to generate a signal having a controlled timing relationship relative to another signal.

Joint Claim Construction and Prop. at 3. Rambus's motion relies heavily upon apparent conflict between Hynix's invalidity contentions regarding the lack of written description for a "delay locked loop" in the patent specification and its non-infringement position with regard to the same limitation.

II. ANALYSIS

Each of the claims-at-issue are dependent claims reciting the term "delay locked loop" as an additional limitation to the corresponding independent claims in the '918 patent (claim 18), '120 patent (claim 26), '916 patent (claim 26), and '105 patent (claim 36). Claim 38 of the '120 patent is exemplary of the use of "delay locked loop" in the asserted claims:

> 38. The memory device of claim 26 further including **delay locked loop** circuitry coupled to the clock receiver circuitry to generate an internal clock signal, wherein the plurality of output drivers output data in response to the internal clock signal.

'120 patent, claim 38.

A. Hynix's Use of "DLL"

A "delay locked loop" is typically represented by the acronym "DLL." Murphy Decl. Supp. Infringement ¶ 6. It is undisputed that schematics and datasheets for HY5DU2822T, the representative Hynix DDR SDRAM product, label certain elements with the acronym "DLL." *See, e.g.*, Taylor Decl. Supp. Hynix's Mot. Relief ("Taylor Decl. Supp. Mot. Relief "), Ex. 5 ("Hynix DDR SDRAM Datasheet") at 7-9 (block diagram including block labelled "DLL Block" with a "CLK_DLL" output); *id.* at 3 (listing an "On chip DLL" as a feature of the HY5DU2822T); Murphy Decl. Supp. Infringement, Ex. B ("schematics") (HR905_146223 schematic labelled "DLL").

Rambus asserts that the depictions of elements labelled "DLL" indicate the presence of a delay locked loop as agreed upon by the parties in Hynix's DDR SDRAM devices, especially when taken in conjunction with arguments made in Hynix's motion for summary judgment of invalidity for claims including "delay locked loop." In its motion for summary judgment of invalidity, Hynix asserted that the Rambus claims, as issued, "include[] any form of delay locked loop circuitry." Hynix's Mot. Summ. J. Invalidity Re: Delay Locked Loop at 10. Hynix relied upon testimony by its expert, David Taylor, that it is "known to one of skill in the art" that "a delay-locked loop ("DLL") is a special type of phase locked loop ("PLL") which uses a variable delay line." Taylor Expert Report Re: Invalidity, Noh Decl.

Supp. Rambus's Mot. Summ. J. Infringement Delay Locked Loop, Ex. B ¶ 72. Rambus thus contends Hynix has conceded that the "DLL" element depicted in the datasheets and schematics for the accused devices is a "delay locked loop" utilizing a "variable delay line." Rambus asserts that a "delay locked loop" is necessarily present in Hynix's DDR SDRAM products because (1) Hynix's datasheets confirm the existence of a "DLL," (2) Hynix has admitted that Rambus's claims-at-issue include "any form of delay locked loop circuitry," and (3) Hynix has established that all delay locked loops use a variable delay line.

Hynix, on the other hand, contends that Rambus's reliance on the use of the "DLL" acronym or label in its product materials cannot be the basis for summary judgment of infringement. Pursuant to the agreed-upon construction, Rambus must demonstrate that there is no remaining issue of material fact that the Hynix "DLL" includes a variable delay line in order for it to meet the "delay locked loop" limitation. The "admissions" Rambus cites, according to Hynix, are taken out of context and cannot be used to dispel remaining jury issues as to whether the "DLL" depicted includes a variable delay line. Although Rambus notes that Hynix's own expert utilizes the acronym "DLL" to describe how one of skill in the art would understand a "delay locked loop," Taylor Decl. Re: Invalidity ¶ 72, Hynix clarifies that Taylor's statement was not made in the context of the elements in the accused DDR SDRAM devices labelled "DLL." Hynix contends that, taken in the appropriate context, the use of "DLL" as an acronym to describe the generic concept of a delay locked loop does not serve as an admission that the "DLL" elements depicted in its datasheets and schematics represent delay locked loop circuitry pursuant to the agreed-upon claim construction.

The court agrees that Rambus may not merely rely upon the presence of elements labelled "DLL" in Hynix's schematics and datasheets or Taylor's use of the acronym "DLL" to describe the general understanding of "delay locked loop" to one of skill in the art. Even when considered in conjunction with the arguments and expert testimony presented by Hynix in its motion for summary judgment of invalidity, Hynix's use of the "DLL" acronym does not sufficiently establish that the element so labelled meets the agreed-upon limitation. The parties' agreed construction requires that, to be a "delay locked loop" under the patent, the circuitry must include a variable delay line. Rambus's argument is: Hynix products include an element identified as "DLL"; "DLL" is an acronym for "delay

locked loop"; all delay locked loops have a variable delay line; therefore, Hynix elements labelled "DLL" have a variable delay line. Rambus's argument permits the court to find the "delay locked loop" limitation met without requiring a showing that the element labelled "DLL" in Hynix's product datasheets and schematics includes a "variable delay line." Rambus cannot assume a "variable delay line" exists in the Hynix element labelled "DLL."

B. Selectable delay network

The parties do not dispute that the element labelled as a "DLL" in the accused product's schematics is coupled to clock receiver circuitry. Nor do they appear to dispute that the "DLL" element operates to introduce a delay between the input and output signals, as required by the agreed construction. Hynix argues, however, that its "DLL" circuitry does not include a "variable delay line" and thus is not a "delay locked loop" pursuant to the agreed construction. It contends that its "DLL" element utilizes a "selectable delay network," making it distinguishable from a "variable delay line." Taylor Non-Infringement Expert Report ¶ 66. Rambus, on the other hand, asserts that the Hynix schematics demonstrate the presence of a "variable delay line" and that Hynix's argument is mere wordplay, substituting "selectable" for "variable" and "network" for "line."

1. Meaning of "variable delay line"

Hynix's expert contends that "variable delay line" is a term of art. He opines that one of skill in the art would recognize the term "variable delay line" to mean "a specific type of circuit which has a single, fixed input and a single, fixed output and uses voltage control to vary the amount of total delay across a fixed number of variable delay elements on a line between input and output." Taylor Decl. Opp. Infringement ¶ 9. In his expert report addressing infringement issues, Taylor cites to U.S. Patent No. 4,922,141 and UK Patent App. No. 2,197,553-A (the "Lofgren reference") and two articles by and U.S. Patent No. 5,101,117 issued to Mark Johnson (the "Johnson references") as exemplars of the term "variable delay line" as would be recognized by one of skill in the art. Taylor Decl. Opp. Infringement, Ex. A ("Taylor Report Re: Non-Infringement") ¶¶ 63-70; Taylor Decl. Supp. Mot. Relief ¶¶ 35, 36. All references cited in Taylor's report and declarations require voltage control to vary the delay serially across the delay stages in order to create a delay between input and output signals. However, these references do not otherwise explain whether one of skill in the art would understand that either voltage

control or a fixed number of delay elements between input and output are required for a "variable delay line."

Rambus objects to Taylor's definition of "variable delay line" as an attempt to introduce a construction of "variable delay line" that has not been agreed to by the parties or adopted by the court. Nevertheless, Rambus offers an alternate explanation of "variable delay line" based upon Taylor's declarations and reports regarding the delay locked loop limitation. First, Rambus contends that a "delay line" is merely a delay circuit for providing an output signal which is delayed by a precise amount with respect to an input signal. In support, it relies on Taylor's citation of the Lofgren reference, as "relating to a delay circuit for providing an output signal which is delayed by a precise amount with respect to an input signal. Such circuits are typically referred to as 'delay lines' and have many applications." Taylor Report Re: Invalidity ¶ 74 (quoting U.S. Patent No. 4,922,141, col. 1, lns. 14-18). Next, Rambus asserts that the term "variable" preceding "delay line" merely means that the delay value can be changed, citing a dictionary definition listing "vary" as a synonym of "change." WEBSTER'S II NEW COLLEGE DICTIONARY, "change" at 186 (2001).

2. Presence of a "variable delay line"

Hynix contends that there is an issue of fact as to whether a variable delay line is present in the elements labelled "DLL" in the Hynix accused devices. Rambus counters that all issues of material fact are undisputed and summary judgment is appropriate because no reasonable jury could find that Hynix's devices lack a "variable delay line" and accordingly meet the "delay locked loop" limitation.

In support of its argument, Hynix notes that the experts arrive at conflicting conclusions as to whether a variable delay line is present in Hynix's inventions. Both analyze the dll_dly_mon cell in the schematics. Taylor concludes that this schematic does not disclose the presence of a variable delay line; Murphy concludes that a variable delay line is present. *See* Taylor Report Re: Non-infringement ¶ 69, Murphy Decl. Supp. Infringement ¶ 9 (analyzing Schematic HR905_146307, Murphy Decl., Ex. 2, (HR905_146307, HR905_146309).

Taylor characterizes the circuitry as utilizing a number of delay stages each having a fixed delay value. The total delay on the path is determined by selecting which delay stage is enabled; it does not rely upon variable voltage control. Thus, the Hynix circuitry applies an input signal in parallel to

several delay stages each with a fixed value rather than applying a single input which is varied across the number of variable delay stages each represented on the path. Taylor Decl. Supp. Mot. Relief ¶¶ 29-38.

Rambus's expert, Robert Murphy, contends that it does not matter whether the delay stages have a fixed value and are selectively applied. The result of applying one of the parallel delay stages is a delay between the input and output, as is required for a delay line. Hynix's devices, then introduce a delay along a path. He contends that the fact that the delay state is "selectable" means that the delay between the input and output "variable" by the amount designated by the selected stage. Thus, the "dll_dly_mon" is a variable delay line for purposes of the "delay locked loop" limitation.

3. Remaining questions of fact

Although Rambus's alternative explanation of "variable delay line" is based entirely upon Taylor's expert reports and declarations, there appears to be a question of fact as to whether one of skill in the art would understand a "variable delay line" to require the variation in the delay line to be voltage-driven and as to whether the application of parallel inputs onto the delay path meets the "delay line" limitation. As the evidence must be viewed in the light most favorable to Hynix, there remains a question of fact as to whether a variable delay line is present in Hynix's accused DDR SDRAM devices.

III. ORDER

In conclusion, the court DENIES summary adjudication that Hynix's accused devices contain elements covered by the "delay locked loop" limitation. Therefore, summary judgment of infringement on claim 33 of U.S. Patent No. 6,034,918, claim 38 of U.S. Patent No. 6,324,120, claim 40 of U.S. Patent No. 6,426,916, and claim 34 of U.S. Patent No. 5,915,105 is DENIED.

DATED: 2/23/06

/s/ Ronald M. Whyte
RONALD M. WHYTE
United States District Judge

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