Standard Interface – Twin-Coaxial Converter

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The Network Operations Control Center standard interface has been adopted as a standard computer interface for all future minicomputer-based subsystem development for the Deep Space Network. A previous article in this report series presented a discussion of an intercomputer communications link using a pair of coaxial cables. This unit is capable of transmitting and receiving digital information at distances up to 600 m with complete ground isolation between the communicating devices. This article describes a converter that allows a computer equipped with the standard interface to use the twin-coaxial link.

I. Introduction

A twin-coaxial intercomputer communications link (Ref. 1), capable of communicating at distances up to 600 m (2000 ft), has been operational for over three years. The advantages of such a link include complete ground isolation between communicating computers as well as the capability of operating in a noisy environment.

When the Network Operations Control Center (NOCC) Standard Interface Adaptor (SIA) was adopted as a standard computer interface for all minicomputer-based subsystem development for the DSN, it was decided to develop a converter to enable any computer equipped with an SIA to interface with, and communicate across, a twin-coaxial link. This article provides a description of the operational characteristics of such a converter.

II. Review of the Twin-Coaxial Link

The twin-coaxial link was designed as an intercomputer link, i.e., the signaling format and priorities are identical at both ends of the link. The link functions in a half-duplex mode; i.e., it can transmit data in either direction, but only one way at a time. Signals on the two coaxial cables are balanced and transformer-isolated to minimize effects of ground-level imbalances between the two communicating devices. The two cables each carry signals in one direction only. The cable connected to the transmit connector at one end of the link must be connected to the receive terminal at the other end.

When the link is inactive, there is no signal in either cable. From the inactive state, the switching on of a 1-MHz carrier by one of the computers (say, computer A)

constitutes a 1-bit message to computer B that communication is desired, and when computer B returns a similar carrier, it acknowledges that message. Symmetrically, the switching off of the carrier is an emphatic "I quit!" message used to terminate transmission or which could be used to reinitialize from erroneous link operation.

Transmission over the link is, in fact, bit-serial, but it is conceptually on a byte-by-byte basis. Bits are transmitted by deleting one cycle of carrier, with the phase of the last cycle of carrier determining the value of that bit. Eight data bits (one byte) and an associated parity bit are sent in consecutive 2-μs intervals. When the receiving computer has room in the buffer associated with the link, it sends a 2-bit control message as a request for the next byte. This "transmit-byte/receive-control packet" handshaking provides synchronization between the communicating controlling software in both computers that accommodates the link data rate to the capabilities of the computers.

Since nine bits are transmitted per byte and two received before the next transmission, a minimum of 22 μs are needed to send each byte. This converts to a maximum rate of 45 kbytes per second but due to computer interrupt timing and software overhead only 25 kbytes have been achieved in practice.

III. Review of the Standard Interface

The NOCC standard interface output consists of fourteen signals and a power sense line. The fourteen signals consist of eight data signals, two function code signals, and four control or handshaking signals. Three of the four combinations of function codes are available for tagging data transmission while the fourth, the 1 1 condition, is reserved for commands out of the computer or status in from the device connected to that computer. Two of the control signals are used as stimulus signals; one from computer (stimulus from computer (STC)) and one from the device (stimulus from device (STD)). Both of these signals are unidirectional and go true for the complete duration of a message. The remaining two signals are bidirectional control signals called response (RSP) and ready (RDY), which control the handshaking of data across the interface. Response and ready each make one complete cycle (false to true to false) for each byte transferred across the interface.

Computer and device SIAs have been assigned different access priorities (Ref. 2). The computer has the highest priority when it wants to send a command. The device has the next two priority levels: first, when it wants to send a status byte to the computer, and next when it wants to transfer data. The lowest priority is the data output mode for the computer. The converter described in this article has the device priority assignment.

IV. Converter Control Signals

Control of the twin-coaxial link through the converter and an SIA is accomplished by sending commands and receiving status. Table 1 shows how the 8 bits of a command are interpreted in the hardware and which bits are returned as status from the converter. D1 is the least significant bit. Following is a detailed description of each bit in the command and status.

D1 **Command** When a 1 is received in this bit position, it will cause the twin-coaxial link to start transmitting if the carrier enable flip-flop has been or is simultaneously set (see D3) and the link is not in the busy receiving mode.

D2 **Command** Unassigned.

D3 **Command** This bit controls the carrier enable flip-flop for the twin-coaxial link. When set to zero, the link is disabled. It must be set to 1 before transmitting or receiving is possible.

D4 **Command** When this bit is set to a 1 in a command, a reset pulse is developed which resets the end-of-message flag and any error flags in the twin-coaxial hardware.

D5 **Command** This bit steers the control message flip-flop. This flip-flop determines the value of the two-bit control message sent by the twin-coaxial link in the receive mode. Normally, the control message is 0 0 while the 1 1 value is used for errors or buffer overflow conditions. (See D7 **Status**.)

D6 **Command** Unassigned.

D7 **Command** There are eight pairs of outputs from the twin-coaxial driver–receiver unit. A multiplexer has been provided to select one of these. The loading of the multiplexer register is controlled by D7. When D7 is a 1, D1 through D4 are copied into this 4-bit register, and not used otherwise; D5 and D6 are ignored. The extra bit in the multiplexer address register allows future expansion to 16 channels.

D8 **Command** This bit, when set to 1, asks the converter to immediately return its present status. When this bit is set, D1 through D6 are ignored.

D1 **Status** A one in this position signifies that the twin-coaxial link received a packet of bits of the wrong length; i.e., not 2 or 9 bits.

D2 **Status** A one in this position signifies that the twin-coaxial link received a bit while it was in the process of transmitting a bit.

D3 **Status** This bit is a copy of the carrier enable flip-flop.

D4 **Status** When this bit is a one, it signifies that an incoming carrier has terminated.

D5 **Status** This bit is a copy of the control message flip-flop.

D6 **Status** A one in this position signifies a parity error in the received byte.

D7 **Status** A one is set in this position when the twin-coaxial link receives the control message 1 1.

D8 **Status** This bit is a 1 or 0 depending on whether the incoming carrier is on or off, respectively.

V. Automatic Control Features

The twin-coaxial link was originally designed to be on a direct I-O port of a computer. It was found that with the SIA between the programmer and the twin-coaxial link, it was more convenient for the programmer if some automatic features were added to the twin-coaxial link converter. These automatic features are:

(1) The converter automatically sends a status byte to the computer when an incoming carrier is detected. This will happen in both the transmitting and receiving modes.

(2) The twin-coaxial hardware is automatically reset when the status byte with the end message flag set (D4) is taken by the SIA. This reset has the same effect as the reset generated when the computer sends a command with the reset bit (D4) set, and, in addition, the carrier enable and control message flip-flops are also cleared.

(3) When the program terminates a transmission, the standard interface will drop its stimulus signal STC. The last byte delivered to the converter may still be there, however, since the twin-coaxial link has to wait for a control message from the device with which it is communicating. To accommodate this case the converter saves the last byte until it is requested, and then terminates the transmission. The software will be notified at the end of transmission, when the carrier coming in to the converter is cut off, generating a status byte delivery to the computer.

(4) Any twin-coaxial error condition (D1, D2, D6, D7 described above) causes a status byte to be delivered to the SIA. Since these error flags are not cleared until a reset pulse is generated in the hardware, an inhibit was provided to let the error status condition be sent only once.

(5) To facilitate programming, the controller can be commanded (by bit D8 in a command) to return its present status to the computer.

VI. Conclusion

An SIA-to-twin-coaxial converter has been built. It will enable any computer equipped with an SIA to interface with the twin-coaxial intercomputer communications link and communicate over ground-isolated coaxial cable up to 600 m. Two complete units have been built to date, one with an eight-way multiplexer at the driver and receiver interface of the twin-coaxial link, which allows the SIA to selectively communicate over one of several coaxial links. Both converters have been successfully tested between an SIA in a Modcomp II computer and a twin-coaxial unit in an XDS 920.

References

1. Lushbaugh, W. A., "A Driver/Receiver Unit for an Intercomputer Communications Link" in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. XV, pp. 109–114, Jet Propulsion Laboratory, Pasadena, CA, June 15, 1973.

2. *Detailed Specifications for Deep Space Network Standard Interface*, Specification No. ES508534, Rev. B, Nov. 26, 1974 (JPL internal document).

Table 1. Status and command bytes

	Command from computer	Status to computer
D1	Start transmitting	Error number bits received
D2	–	Bit received while transmitting
D3	Carrier enable flip-flop	Carrier enable flip-flop
D4	Reset	End message flag
D5	Control message flip-flop	Control message flip-flop
D6	–	Parity error
D7	Multiplexer select*	Control message 1 1 received
D8	Request status return	Incoming carrier on

*When a command is received with D7 set to 1, a multiplexer register is loaded with bits D1 through D4.