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Glenn Research Center

Jet Propulsion Laboratory
California Institute of Technology

Ka-Band Wide-Bandgap Solid-State Power Amplifier Technology

Jet Propulsion Laboratory

Mid-Year Review

Pasadena, California

January 27, 2004

Agenda

- Welcome
- Task Overview
- JPL Design Task
  - Requirements
  - Architectures
  - Detailed Analyses
- Break
- Discussion
- GRC Design Task
  - Overview
  - Notional Architectures
  - Thermal/MMIC Analysis
- Feedback & Wrap-Up

Welcome

- JPL welcomes partner contractors, sponsors, interested parties and guests.
- Purpose & Goals
  - Communicate task status
  - Describe key accomplishments
  - Define future plans
- JPL is a partner contractor for WBG SSPA Study
  - Partner Contractors
    - HRL
    - NGST
  - NASA Glenn is the JPL Managing Organization
    - Also plays a technical role

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A Key Accomplishment

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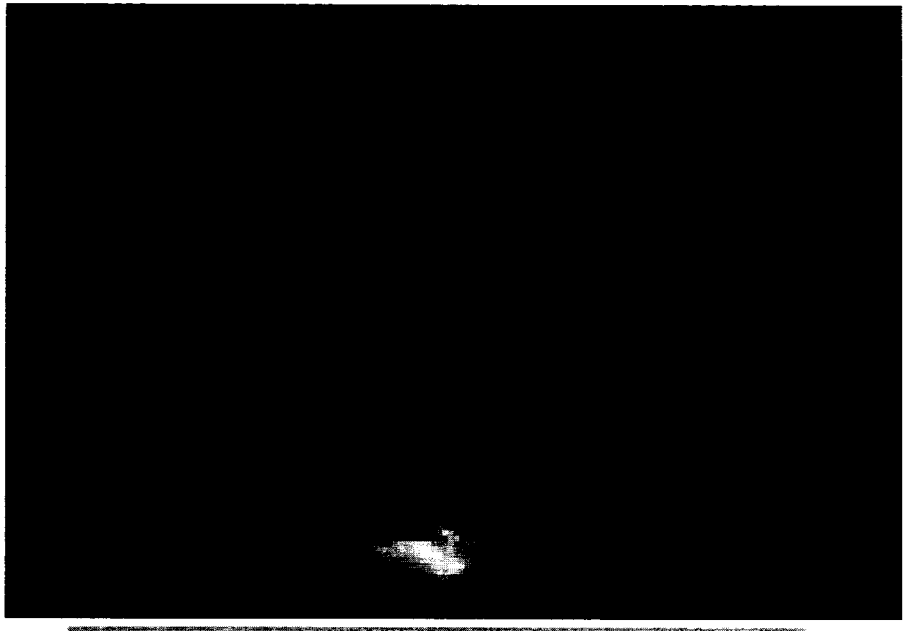
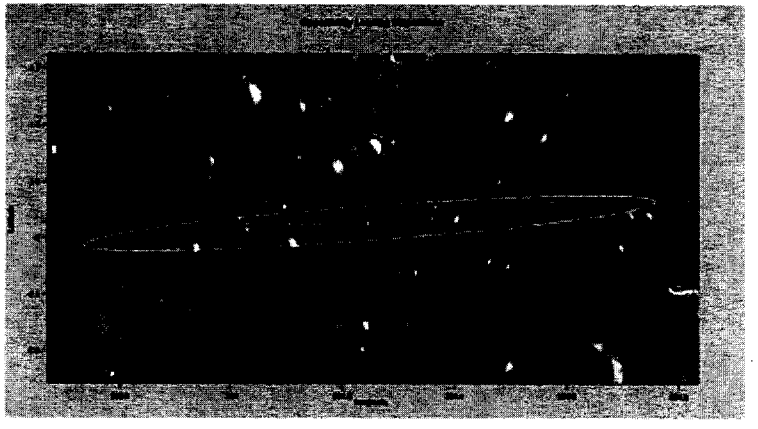
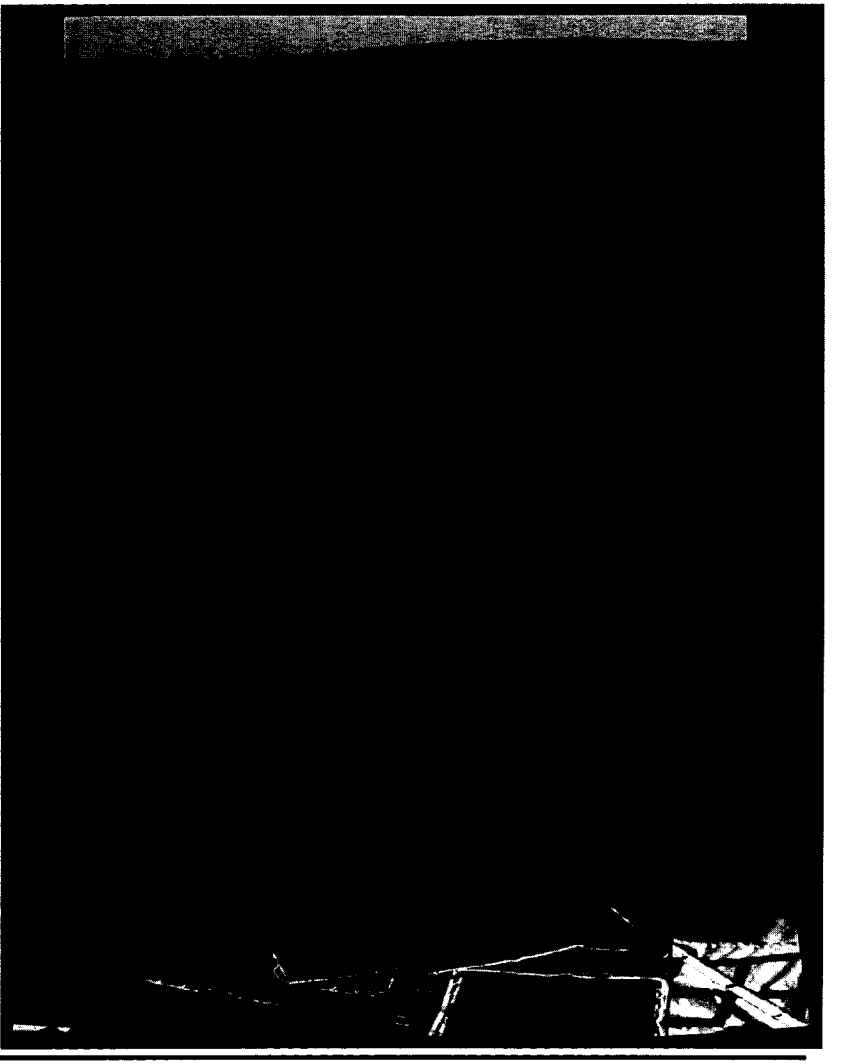
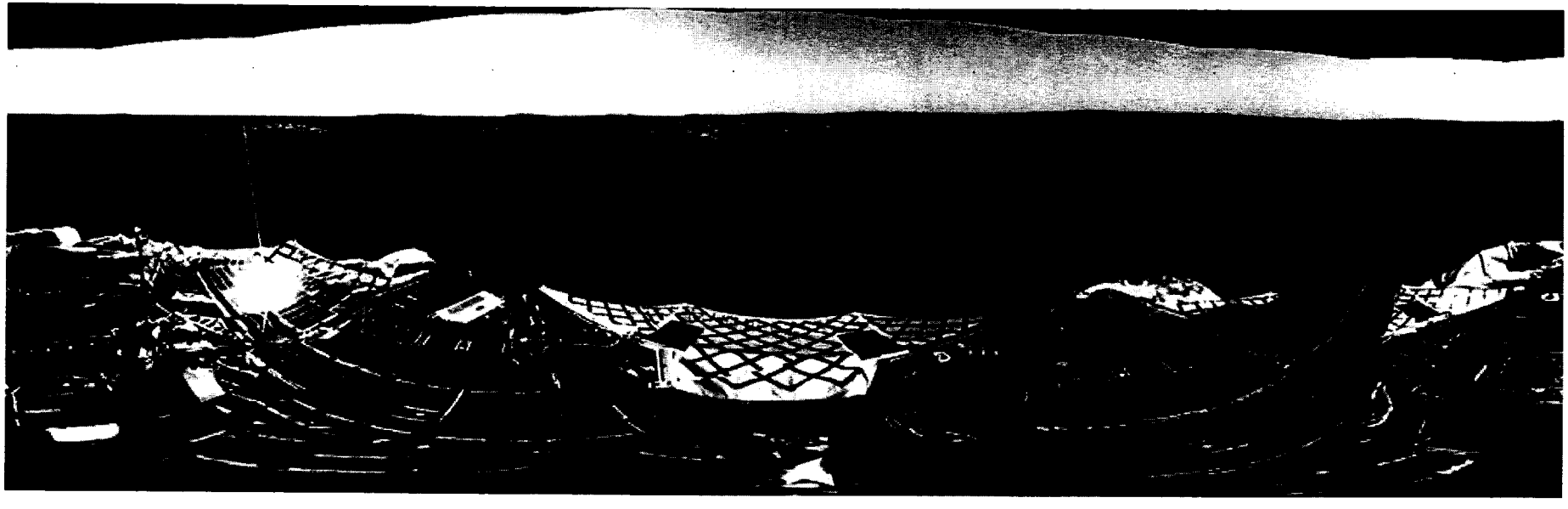






First Panoramic Look



Meridiani Planum, Mars

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TASK OVERVIEW

Program Objective

To determine the feasibility of a WBG semiconductor based 120–150 W Ka-band SSPA as an alternative for space TWTAs with an engineering model build in 3–5 years leading to a flight model build in 7–8 years.

Target SSPA

	PARAMETER	VALUE	NOTE	35 W TWTA	100 W TWTA
1	Power Output	120 to 150 Watts		35 Watts	100 Watts
2	Power Added Efficiency	40%	@P_{1dB}	52% (46% w/EPC)	60%
3	Band of Operation	31 to 36 GHz		31.8-32.3 GHz	31.8-32.3 GHz
4	Bandwidth	10%			
5	Gain	50 dB		51 dB	50 dB
6	Noise Figure	<20dB			
7	AM/PM Conversion	<2°/dB		<4°/dB	<4°/dB
8	Phase Ripple	<3° peak to peak			
9	Input Bus voltage	50 Volts±5 Volts	DC	28 V±4 V	
10	Mass	< 4 kg	incl. EPC	2.5 kg	2.5 kg
11	Environment	GEO or Deep Space			

Additional architecture-dependent requirements include redundancy, graceful degradation, and adequate thermal management.

Noise figure, AM/PM conversion, bus voltage and radiation tolerance are primarily MMIC/semiconductor technology driven.

SSPA Study Task Status

SOW TASK 1: Architecture Identification

- Reviewed over 100 published articles relevant to millimeter-wave power combining and have begun focusing on three general architectures for further detailed study
- Delivered report of findings to sponsor (11/7/03)

SOW TASK 2a: Detailed Architecture Considerations

- Defined sub-system requirements and trade space
- Currently evaluating electrical performance of architectures identified in task 1 at component and system levels (80% complete)
- Have started to evaluate mechanical and thermal performance

SOW TASK 2b: MMIC Considerations

- Established subcontract with Rock Systems LLC to evaluate WBG reliability status and identify critical path/develop roadmap for insertion into high-reliability applications

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GaN Reliability Subcontract

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- Contract established with Rock Systems LLC, December, 2003
  - S. Kayali (JPL), G. Ponchak (GRC), R. Shaw (Rock Systems), "GaAs MMIC Reliability Assurance Guideline for Space Applications"
  - Reliability Lead – Roland Shaw, Rock Systems LLC
- 6 month study of WBG device reliability status and roadmap

- Phase I results due 2/3/04
  - Current reliability status of GaN broad state-of-the art devices and comparison with GaAs technology
  - Critical path for GaN insertion in space and high-reliability applications

- Phase II results due 7/10/04
  - Recommendation for core reliability guideline for WBG RF semiconductors
  - Possible failure mechanisms
  - Accelerated life test methodology requirements
  - Critical development roadmap required for 3-5 year technology insertion

- Phase I results will be included in NASA interim report #2

Progress Summary

- We have examined promising architectures and believe we can meet requirements outlined for the program
  - Low combiner losses (approximately < 1.0 dB total)
  - Projected GaN MMIC performance (not outside the realm of possibility)
    - Advances still required
    - Challenges still ahead
- PAE is what may differentiate WBG technologies at Ka-band to be competitive with the tube
  - A lower power MMIC (3W) but high PAE (greater than 40%) may afford a reasonable compromise in terms of thermal footprint and graceful degradation
  - May be the most viable approach consistent with the customer timeline
- Important next steps in the current phase are key component proof of concept hardware demonstrators and modeling for high efficiency
  - Combining circuits
  - Thermal studies

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Phase I Schedule

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Tasks	Months after start of contract											
	1	2	3	4	5	6	7	8	9	10	11	12
	AUG	SEP	OCT	NOV	DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL
1. Architecture Identification												
2. Detailed Analysis												
3. Hardware Validation												
4. Technology Roadmap												

- **Task Start: August 4, 2003**
- **Task 1 – Architecture identification, completed**
  - **Interim Report #1 delivered November 7, 2003**
- **Task 2a – Detailed analyses of selected architectures currently underway**
- **Task 2b – WBG technology review**
  - **Reliability study subcontract established**
- **Interim report #2 on detailed analysis due March 2004**

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SSPA Roadmap

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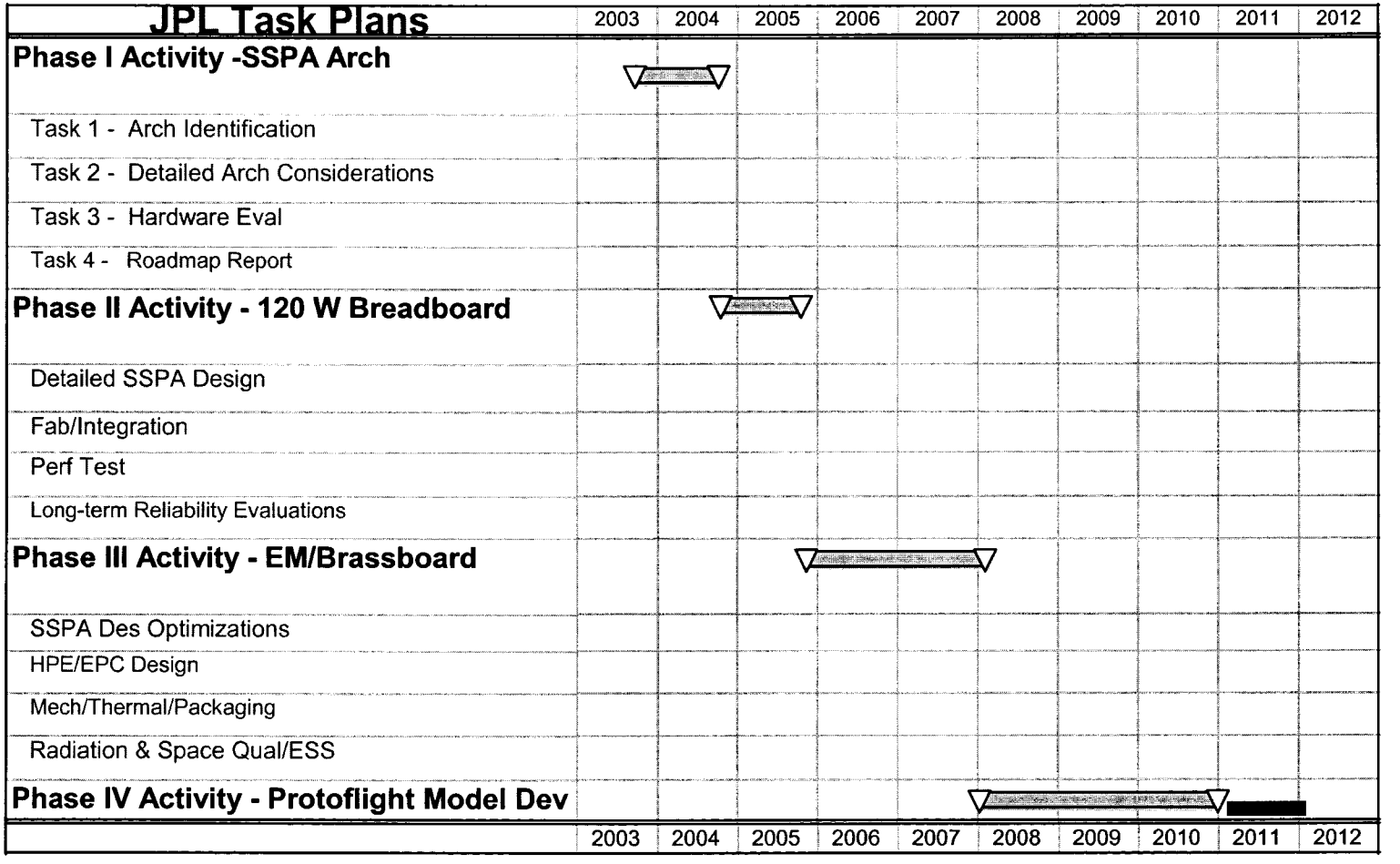

WBG SSPA Roadmap

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