Fermi National Accelerator Laboratory

BTeV PIXEL DETECTOR

DATA IN AND OUT/
OPTICAL RECEIVER CHIP

--PRELIMINARY--

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1. INTRODUCTION

The principal function of BteV's Pixel Detector is to acquire and deliver a very high data volume. However, some information must travel in the opposite direction. Clock, Initialization and Control signals must be delivered to the Pixel Detector planes. We can define *the pixel detector slow control and monitoring* as the group of actions which allow us to interact and supervise the pixel detector amplifier chips. These actions can be performed at a slower speed compared to the pixel data readout speed. This document starts the specification of an optical link receiver chip. The problem of sending data from the Pixel Detector's plane for supervision purposes is not considered here. However, at first sight exist the idea of using the high-speed data channels to send this information. The minimization of the number of fiber optic channels is very important for several reasons like space available in the pixel plane, power budget, fault tolerance, and cost. The estimated price for an optical link is about $200 and there are about 2000 optical links in the Pixel Detector.

1.1 Overview of the Pixel Plane

A block diagram of the Pixel Plane is shown in Figure 1. The Pixel chips need a clock to operate. Most of its actions are synchronous with this clock. Even when the FPIX chips can operate at a wide range of clock frequencies, the most likely will be to use the 53 MHz clock provided by the accelerator. This clock may be internally divided by two to operate some sections of the FPIX chip where the speed is not so critical or where a better noise margin is required. Some chips may, also require a 106MHz clock.

Another important component in the Pixel Detector's plane is the fiber optic link Serializer/Transmiter. This chip will need a "very clean" clock, with less than 100ps of jitter. The Serializer/Transmiter is being designed to operate up to 60 MHz, so the 53 MHz clock will be appropriated as well.

The pixel chip needs a BCO clock to provide temporal information to hit occurrence. The BCO clock is 7 times slower than the 53 MHz clock and synchronous with it. Furthermore, the pixel chip needs some control and initialization signals. Most of these signals must be provided from outside the Pixel Detector plane. We can classify them as Initialization, Reset, and Control. All these signals can be run at a lower speed.

The initialization signals, including the initialization clock, are driven during the initialization of the load and kill pattern and the mask for each pixel cell. The speed of this pattern faces a trade off between the speed of the download and the error rate probability. A clock of few MHz seems appropriate. For details see [1]

All control signals, like Reset, Throttle, etc can be operated with a response time of few μs.

In order to minimize power consumption, physical space, and cost, the number of optical links will be as few as possible. Since all the commands are slow they can be serialized onto a single fiber. The BCO clock (~7.5MHz) will, also, be codified in the same fiber channel. Figure 1 shows the proposed fiber optic links for both the receiver and the transmitter ends, and the connection to the Pixel chips. The receiver end will codify a 53MHz (or 106 MHz) clock, the BCO clock and control/data information onto a single fiber.

The FPIX Initialization and Control functions are not concurrent. The Initialization functions are the ones used to configure the FPIX for the Analog Input Charge Inject or Detector Charge Inject modes of operation. Several data patterns are stored into the FPIX memory. This memory is laid out as a set of shift registers into the FPIX. The initialization is performed through a serial input, shifting the data with a clock and selecting a specific shift register with some control lines.

The Control functions send a command to the chip while the chip is operating (either in the Analog Input Charge Inject or Detector Charge Inject mode). A control action can stop the acquisition of hits as with Data or Program Resets, throttle the FPIX or request status information without interfering with the FPIX normal operation. A detailed specification of each signal and timing information is provided in the following sections.

The FPIX chip needs three clocks Rdoutck (53MHz), BCOck (7.5MHz) and ShiftCk (in the few MHz range). The Rdoutck and BCOck run concurrently; the ShiftCk runs while the other two are stopped.

The cost of each optical link is estimated between $100 and $200. Each fiber added to the optical system will cost at least $150. If the addition of a fiber is one per half pixel detector plane, the total cost of an additional fiber, multiplying by ~200 half planes is $30K. If the fiber must be added in more than one place in each half plane, the costs will be higher. This is the case if a fiber to be added, such us for BCO clock, must be duplicated to meet electrical constrains (like noise, crosstalk, etc) or physical constrains in a tight layout design (flex circuit).

Schematic diagram:

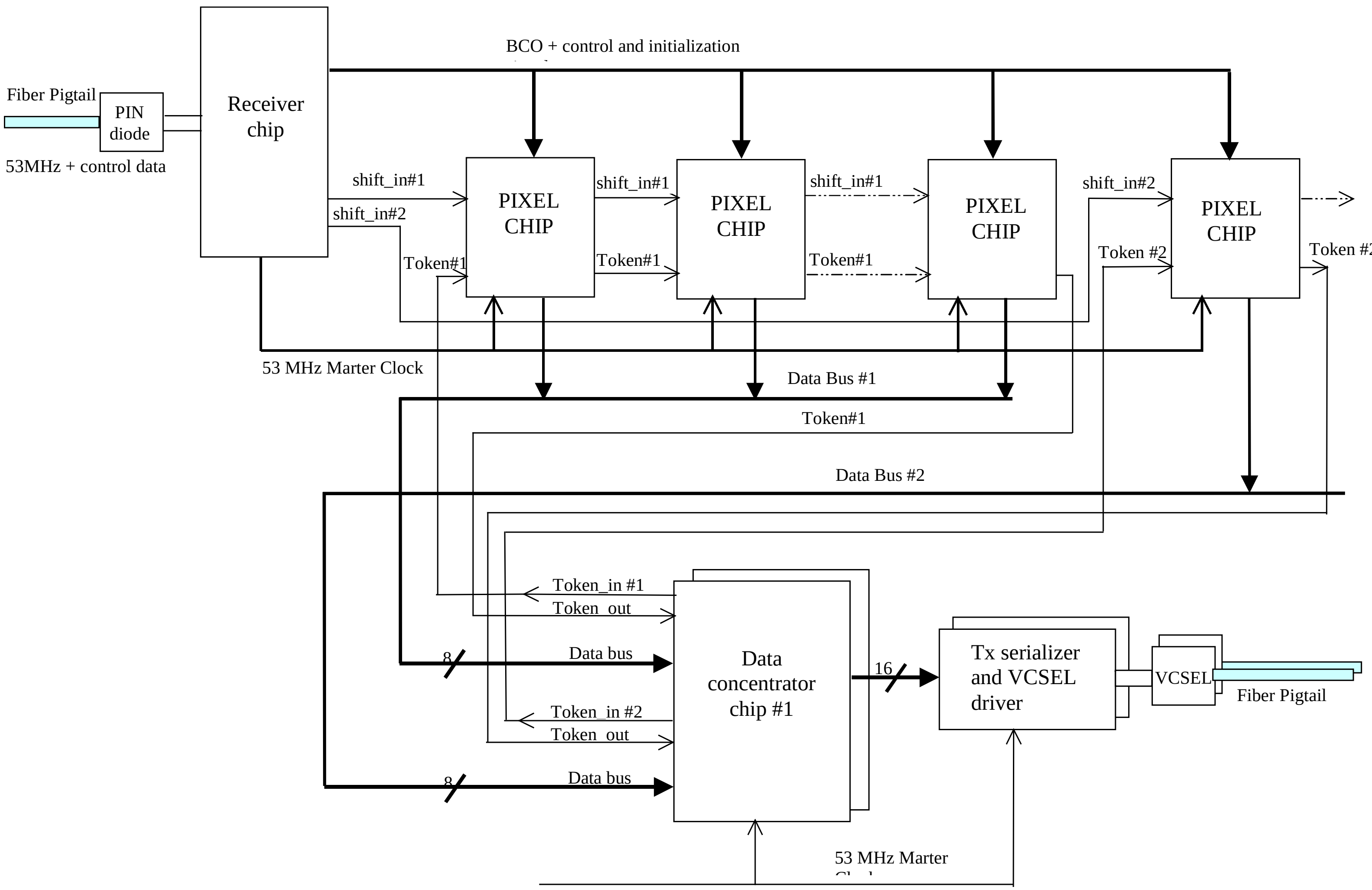


Figure 1

1.2 The Optical Receiver Chip

The Optical Receiver chip is an analog and digital device. Its main functions are the following:

- Decodes the PIN diode signal
- Interfaces the DAQ system to the input of the FPIX chips.
- Decodes and generates timed Control and Initialization Data to the FPIX chips.
- Provides the adequate electrical protocol (CMOS and LVDS) to the FPIX chips.
- Cleans up the 53MHz (106MHz) clock with a PLL.
- Generates the BCO clock.

1.2.1 The Optical Receiver Input protocol

The input electrical protocol will follow a bi-phase mark encoding. The bi-phase mark encoding codifies clock and data onto the same channel. The fundamental reasons for this are:

- Reduces the number of fiber channels
- Guaranties transitions every clock for PLL synchronization
- It is a DC balanced protocol.

Figure 2 shows a timing diagram of the bi-phase mark protocol.

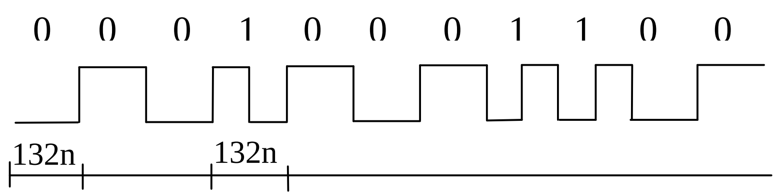


Figure 2

1.2.2 Data Frame

The data can be framed as shown in Figure 3. The first field is a pattern of zeros used for synchronization. Every word has 14 bits the first bit is used to synchronize the BCO clock. The next bits are used for commands and data. Note that since the data is bi-phase encoded with the 106MHz clock, there will always be transitions present, even when the data is a string of 0’s. The Sync. Pattern, all zeros, is used to delimit the and of one frame and the beginning of the next one. The Command field will perform an internal action, setting FFs or generating timing conditions needed to interface with the Pixel chips or Data Concentrator chips. The data is loaded into the Pixel chips in series. In case more than one chip is daisy chained together, the initialization sees the chain of chips as a single chip.

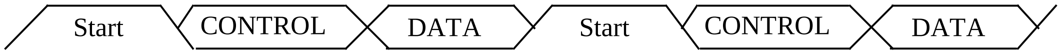


Figure 3

The transmitter must send a synchronization pattern of at least 2 words of 0's, after which the receiver must guarantee to be ready to accept a command frame. When the receiver is synchronized, it will be waiting for the first 1 to signal the beginning of a word. The size of the Command field will depend on the number of commands needed (5 bits at least).

2. DECODER

The Optical Link Receiver decoder receives a current from the PIN photodiode. The current is converted to a voltage by a transimpedance amplifier. Figure 4 shows two possible block diagrams of the PIN current decoder. The characteristics of the optical input signal are critical to the design of the PIN decoder. The bi-phase mark protocol of the optical signal is DC balanced. However, the wide tolerances of optical components make very difficult to keep a stable DC level in the channel. PIN diode AC coupling eliminates the DC component. However, some signal level adjustment may be necessary at either the transmitting or receiving end.

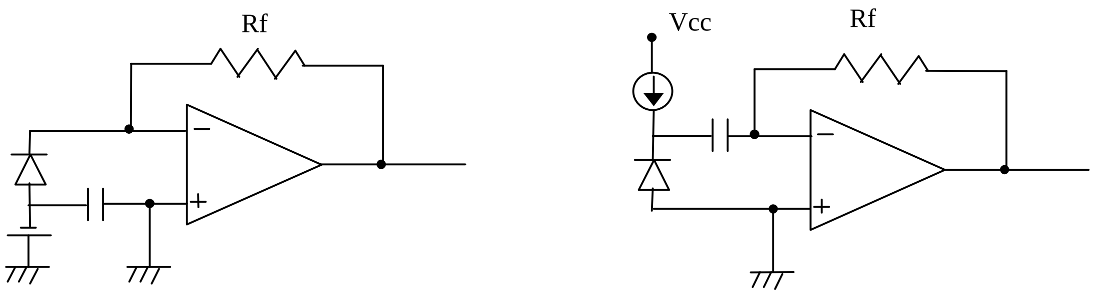


Figure 4 a) and b)

The decoder in Figure 4a) can be implemented with a differential input based amplifier. The one on Figure 4b) uses a cascode amplifier.

2.1 The Optical Input signal

VCSELs are excellent optical transmitters due to their low power consumption, low threshold current, and high radiation tolerance among other advantages. However, like other optical sources, they have some negative features. The most critical one is the wide tolerance in the L-I (light-current) characteristic. Figure 5 shows a typical L-I curve of the VCSEL 444 from Mitel. The output power of the two tested VCSELs differs in a factor of two. Other major sources of optical power variation are due to:

- connectors in the optical link
- coupling between the optical devices and fibers

- temperature and radiation effects

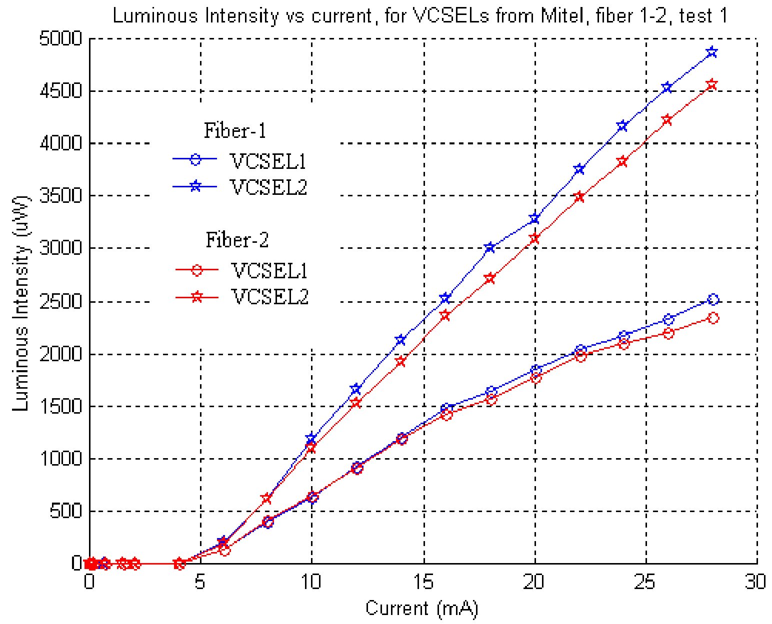


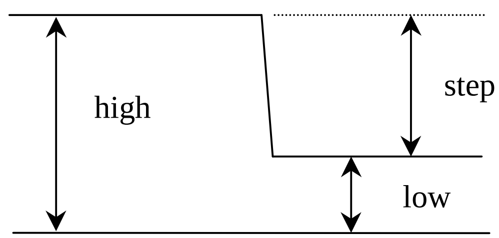
Figure 5

The current at the output of the PIN diode for the best and worst case can be a factor of 5 or more. This complicates the decoder's function to discriminate a zero from a one. The upper value of a signal (discriminated as a one) will be lowered by:

- VCSEL optical power dispersion (Figure 5)
- VCSEL to fiber assembly misalignment
- Fiber to fiber assembly misalignments and dispersions: Connector assembly and splicing.
- Radiation effects

The Lower level of a signal (discriminated as a zero) will be risen up by:

- PIN diode "dark" current in the order of
- Minimum current generated to keep the VCSEL biased close to the threshold.



The step size can be as big as 600µA or as small as 50µA.

Figure 6

The minimum and maximum values of an optical one will lie between 200µW and 2mW. Assuming a typical responsivity in the PIN of 0.3A/W, the high level signal current will be in the range of 60µA to 600µA. The low level signal can be estimates to be in the range 0µA to 200µA.

It is evident that the transimpedance amplifier must handle a wide dynamic range, be low noise and have some kind of gain control.

More results on VCSEL, PIN and fiber testing can be found in [2][3][4] or http://www-ese.fnal.gov/eseproj/BTeV/BTeV_Optical_Links/BTeV_DIO_webpage.htm

3. OPTICAL RECEIVER'S LOGIC

The logic is in charge of generating the appropriate signals to interface to FPIX chips. The Optical Receiver Outputs must be general enough to interface to future versions of FPIX as well as to similar chips in other BTeV detector subsystems. The Optical Receiver Outputs are of three different electrical protocols:

- CMOS: to FPIX initialization and control inputs
- LVDS: to FPIX clocks and some control inputs
- Differential PECL: to feed the CHFET clock

The input serial data is paralleled by a shift register. The frame synchronization is given by the first bit in the serial data frame. The parallel data is decoded by a command decoder. This block is pure combinatorial logic. The command decoder sets or resets a FF synchronously with the 53MHz clock. Figure 7 shows a block diagram of the proposed architecture.

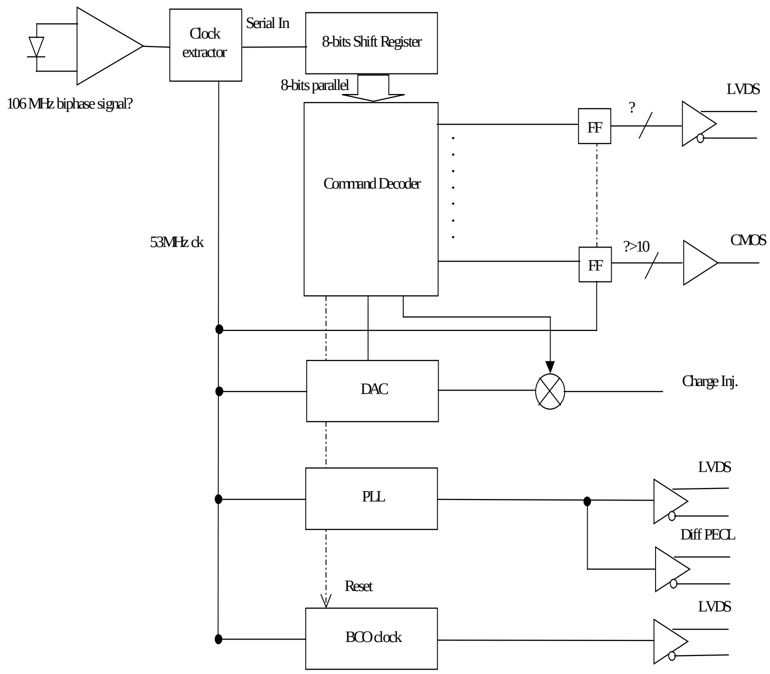
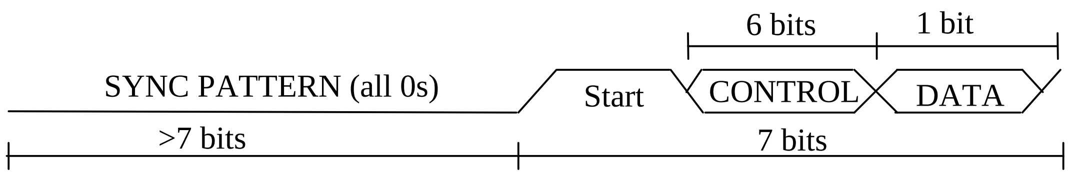


Figure 7

3.1 Frame synchronization

Frame synchronization is provided by a long stream of 0s. The number of 0s must be greater than the length of a data frame (i.e 7 bits). The first 1 after the sync pattern is used as frame delimiter.



The shift register must shift the data using the rising edge of the recovered 53MHz clock provided by the PLL circuit.

3.2 Command decoder

The command decoder is a pure combinatorial demultiplexer. The five control lines C(0:4) allow for 32 different commands. Each command code activates a single output of the demux logic activating the enable of a FF type D. The enabled FF is synchronously latched at the rising edge of the 53MHz clock using the DATA bit as input. The FF can also be asynchronously reset (or preset, one but not both) when a software reset command is received.

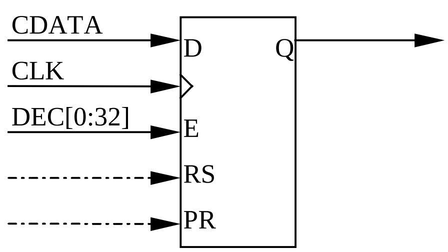


Figure 8

Not all of the 32 commands are used for FF decoding. The command 00000 is defined as NOP and the command 11111 as software reset. The NOP command generated no operation in the ORx chip. The reset command will preset and reset every FF.

3.2.1 Command table

	Command	Value
0	NOP	00000
1	Data Reset	
2	Program Reset	
3	BCO_ck_en	
4	ShiftIn#1	
5	ShiftIn#2	

6	ShiftIn#3	
7	ShiftIn#4	
8	Load/Kill_set	
9	Set_ScanPath_FF#0	
10	Set_ScanPath_FF#1	
11	Set_ScanPath_FF#2	
12	Trigg/Acc	
13	Reset BCO counter	
14	Token_eneble	
15	Report_Status	
16	DAC_FF#0	
17	DAC_FF#1	
18	DAC_FF#2	
19	DAC_FF#3	
20	DAC_out_en	
21	LVDS_en	
22	PECL_en	
23-30	(Reserved)	
31	Receiver reset	11111

Table 1

3.2.2 Command timing

Parameter	Description	Min	Max	Units
t_1	Clock high time	8		ns
t_2	Clock low time	8		ns
t_3	Clock cycle time	20		ns
t_4	Setup time	6		ns
t_5	Hold time	3		ns
t_6	Setup time	4		ns
t_7	Hold time	3		ns
t_8	Reset/preset pulse width	15		ns
t_9	Reset/preset to Q output		8	ns

DV_{DD}=3V±5%, T_A=+5°C to +65°C

Table 2

3.3 BCO clock decoder

The BCO clock is a 7.57MHz clock, which indicates a new bunch crossing of the accelerator. This signal is synchronized with the START bit of the frame. This is the reason why the length of the frame is fixed to 7 bits. Since the data is transmitted at 53MHz and the BCO clock is 1/7 of that frequency, a sync bit every 7 provides the BCO clock. The BCO clock will be adjusted in phase at the transmitting end, outside the Pixel Plane detector.

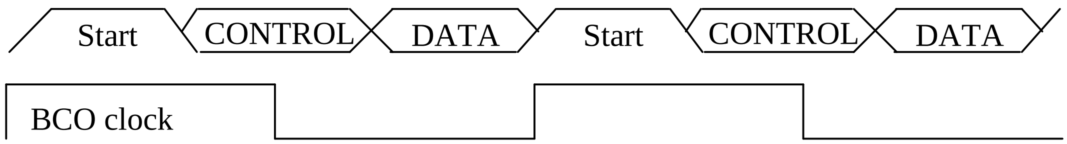


Figure 9

The BCO clock is only routed to the FPIX chips when the BCO_ck_en FF is on (i.e high). The BCO clock is used to increment the BCO counter into the FPIX chips. It is not necessary that the BCO clock be a 50% duty cycle signal. The minimum widths are given in the table below. The outputs of this clock are LVDS differential.

3.4 The 53MHz clock

The 53MHz clock is recovered from the signal by a Phase Lock Loop circuit (PLL). The characteristics of the PLL are specified below. The 53MHz clock must be output in two different protocols, differential PECL to feed the CHFET gigabit transmitter chip [ref] and differential LVDS for the FPIX chips. The CHFET chip requires a very clean clock, with less than 100ps of jitter. The clock must also be close to a perfect 50% duty cycle signal. The number of clock outputs will depend on the number of chips per Pixel Plane and the electrical characteristics of the flex circuit.

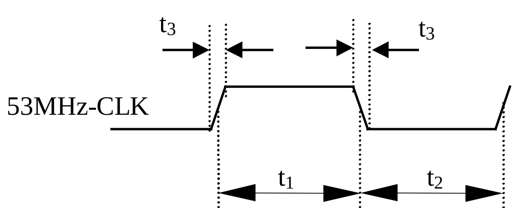


Figure 10

Parameter	Description	Min	Max	Units
t_1	Clock high time @ 53 MHz 50% duty cycle	9.38	9.48	ns
t_2	Clock low time @ 53 MHz 50% duty cycle	9.38	9.48	ns
t_3	Rise and fall times		100	ps

DV_{DD}=3V±5%, T_A=+5°C to +65°C

Table 3

4. PHASE LOCK LOOP

The PLL circuit recovers the 53MHz clock, provides phase synchronization and rejects the jitter. The PLL is the most crucial circuit in this chip since the jitter specification for the 53MHz clock at the output is very low (better than 100ps). The block diagram of a digital PLL is shown in

Figure 11

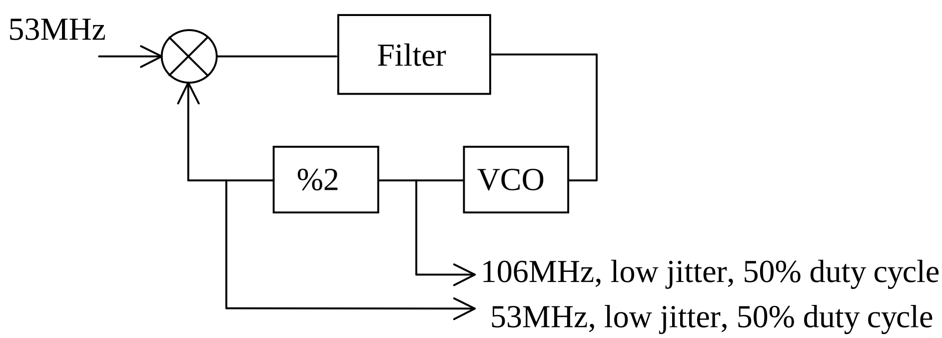


Figure 11

The PLL divides by 2 before comparing the phase of the 53MHz signals. Hence the output of the VCO will stabilize at 106MHz. This frequency may be used as the readout clock of some “hot” chips in the pixel plane closest to the beam.

5. DIGITAL TO ANALOG CONVERTER

The ORx chip will have a 4 bit DAC to generate the Calibration Inject pulse to the FPIX chips. A DAC_en analog switch will enable the output of the DAC (Figure 7). Table 4 shows the specifications of the DAC.

Parameter	Condition	Min	Max	Unit
Analog output voltage				
Resolution		4		bits
One bit resolution		115	135	mV
Temperature dependency	Full temp. range, any bit combination		10	%
Output voltage	All bits at one	1.9	2.1	V
Output voltage	All bits at zero	0.0	0.1	V
Degradation	1Mrad		50	mV
Power supply sensitivity	AV_{DD}=2.75V to 3.25V		50	mV

AV_{DD}=3V±5%, T_{DIE}=+5°C to +65°C, V_{REF} = ?V,

Table 4 DAC specifications

The only AC performance characteristic of the DAC to impose major constrains on the design is the output noise spectral density, which generates a RMS noise voltage in the output of the DAC. One way to limit the RMS noise is to limit the bandwidth of the output amplifier of the DAC, or, similarly, its slew rate. Other AC characteristics like settling time, channel-to-channel isolation, digital crosstalk, digital feedthrough, etc. will not be specified.

a) Temperature dependence: this measure is done with AV_{DD} = 3V and with the reference voltages fixed, and includes all effects of temperature. The DAC characteristics specify the maximum variation of the DAC output voltage considering a temperature variation from -10°C to +50°C.
b) Degradation: this measure is done with all voltages and temperature fixed, and with the DAC submitted to a dose rate of 0.01 rad/s. The DAC characteristics specify the maximum variation of the output, due to radiation or any other aging or degrading effect.

6. ELECTRICAL CHARACTERISTICS OF THE DIGITAL LINES

We will now specify the electrical characteristics of the single ended and differential inputs and outputs of the DDR lines.

6.1 Single Ended Lines

All the single ended lines must be CMOS compatible. Table 5 describes the requirements of the single ended lines.

Electrical Characteristics of the Single Ended Outputs

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output voltage low	V_{CC} = 3.25 V I_{OL} = 5mA		0.4	V
V_{OH}	Output voltage high	V_{CC} = 2.75 V I_{OH} = - 5mA	2.4		V
t_{Of}	Fall time	C_L= 20pF, R_{LOAD} = 500Ω[1]	1	3	ns
t_{Or}	Rise time	C_L= 20pF, R_{LOAD} = 500Ω[2]	1	3	ns

DV_{DD}=3V±5%, T_A=5°C to +65°C

Table 5

6.2 Differential Lines (LVDS)

All differential lines must conform to the Low Current Differential Signals (LCDS) electrical protocol [4]. The main characteristics of this protocol are the following:

a) Specified for a maximum frequency of 53 MHz (106MHz??).
b) Driver and receiver with controllable tri-state output mode.
c) Specified minimum and maximum rise and fall times.
d) Intended for cables with characteristic impedance between 25 Ω to 120 Ω.
e) Allows for different types of cable termination.

6.3 Differential PECL

1. Specified for a maximum frequency of 53 MHz (106MHz??).
2. Driver and receiver with controllable tri-state output mode.
3. Specified minimum and maximum rise and fall times.

????

7. POWER SUPPLY CONSUMPTION

The power supply consumption of the ORx chip should be as small as possible. Estimation: ???

[1]Fall time is the time the output takes to fall from 2.4 V to 0.4 V.
[2]Rise time is the time the output takes to rise from 2.4 V to 0.4 V.

8. PIN ASSIGNMENT

9. REFERENCES

[1] "BTeV Pixel Detector: Data In and Out Optical Links", G. Cancelo, Fermilab, March 1999.
[2] "MITEL VCSEL 444 tests", S.Vergara-Limón, G. Cancelo, Document # ESE-PIX-?????, Fermilab, May 1999.
[3] "MITEL VCSEL array tests", S.Vergara-Limón, G. Cancelo, Document # ESE-PIX-?????, Fermilab, May 1999.
[4] "Honeywell VCSEL HFE4080 tests", S.Vergara-Limón, G. Cancelo, Document # ESE-PIX-?????, Fermilab, May 1999.