Hiroshi Takeuchi et al.: A VSI-compliant 2-Gsps DAS for Spacecraft Differential VLBI, IVS 2006 General Meeting Proceedings, p.221–225
http://ivscc.gsfc.nasa.gov/publications/gm2006/takeuchi

A VSI-compliant 2-Gsps DAS for Spacecraft Differential VLBI

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Abstract

A 2048-Msps (2048 Mega samples per second) data acquisition system (DAS) that complies with VLBI Standard Interface (VSI) has been developed. The new A/D sampler, named ADS-3000, is upward compatible with ADS-1000, current-generation 1-Gsps sampler used for wide-bandwidth astronomical observations. This new DAS has two VSI-H output ports and each operates at a clock frequency of 32 MHz or 64 MHz. Thus the maximum output rate reaches 4096 Mbps. The first-ever 4-Gbps (2048 Msps/2 bits) VLBI experimental observations were successfully performed between Kashima 34m and Kashima 11m antennas on November 25,2005 by using these samplers. Both the data sampling rate (2 Gsps) and the total data rate (4 Gbps) recorded the highest rate ever used for VLBI.

1. Introduction

High speed data acquisition is one of the key technologies for sensitive radio continuum observations in VLBI. To detect fainter radio sources with a shorter integration time, NICT has developed high-speed Gigabit A/D samplers, named K5/VSI series, that support the VSI-H specifications [1]. ADS-1000 [2] is a VSI-compliant, single-channel, 2-bit A/D sampler whose sampling rate is 1 GHz. It is widely used at Japanese domestic VLBI stations especially for wideband astronomical observations. ADS-2000 is a VSI-compliant, 2-bit A/D sampler equipped with 16-channel analog input ports, which is dedicated to geodetic VLBI observations. Sampling rate is selectable from 2,4,8,16,32 or 64 MHz and thus total data rate is up to 2 Gbps. As a successor of these samplers, we developed a new A/D sampler named ADS-3000 having the following features:

- Data sampling rate is increased to 2 GHz, providing $\sqrt{2}$ times improved sensitivity for astronomical purposes than using ADS-1000. The frequency difference between the lowest and the highest frequency channels at X-band exceeds 500 MHz in some recent IVS sessions. This data sampling rate is high enough for such geodetic sessions.
- The number of quantization bits is increased to 8 bits. While 2-bits quantization is enough for normal radio sources in conventional VLBI sessions, it is not enough for high SNR signals such as satellite downlink signals or for single-dish power-measurement experiments such as pulsar timing observations. This wide quantization bit depth allows it to be used not only for VLBI but also for a variety of general applications.

We describe the specifications of the ADS-3000 and report on the first VLBI experiments with the DAS.

2. System Overview

The main specifications of the sampler are summarized as follows:

- Reference signal: 1 pps signal, reference 10-MHz clock (0 dbm± 3dbm, 50Ω)
- A/D input: 0V±250mVp-p(50Ω), Sampling rate: 2048 MHz (fixed), 3.3 GHz full power input bandwidth(-3dB)
- Gain flatness: ±0.2dB(from DC up to 1.5 GHz)
- Low input VSWR: 1.2 Max From DC to 2.5 GHz
- SFDR = -54dBc, 6.5 Effective Bits for 2 GHz input [-1 dBFS]
- Bit error rate: 10e-12 at 2Gsps
- PLO phase noise: 100 Hz-up to 70 dBM/Hz, 1 kHz-up to 80 dBm/Hz, 10 kHz-up to 90 dBm/Hz, 100 kHz- up to 110 dBm/Hz
- Dimension: 88.1mm(H) x 482.6mm(W) x 430mm(D)
- Power supply voltage: AC100V-230V

In the sampler, 8-bit digitalized data with a 2-Gsps,10-bit A/D converter (Atmel Corporation, TS83102G0B) are sent to Field Programmable Gate Array (FPGA) device (Xilinx, XC2VP40) to be processed (Fig.3). This 16-Gbps input data can be decimated with the FPGA to limit the total output rate within 4Gbps, the highest output rate realized with two VSI-H ports. Selectable output modes are listed in Table 1. Because the used A/D converter chip has a sensitivity up to 3.3 GHz, the higher order sampling method, in which band-limited signals which have the higher frequency components compared to the Nyquist frequency of the sampler (1 GHz), is also available. FPGA code is easily programmable by inserting a CompactFlash (CF) memory card, on which FPGA program is written, into the CF slot (Fig.2) of the ADS-3000 so that it can be used for multiple independent applications.

Table 1. Selectable output modes of ADS-3000. There is a trade-off between sampling rate and number of quantization bits.

Total rate	**Sampling rate**	**# of bits**	**Clock rate**	**Output VSI-H ports**
1Gbps	128 Msps	8	32 MHz	Port1
2Gbps	1024 Msps	2	32 MHz	Port1(MSB) + Port2(LSB)
2Gbps	512 Msps	4	32 MHz	Port1(Upper 2bits) + Port2(Lower 2bits)
2Gbps	256 Msps	8	32 MHz	Port1(Upper 4bits) + Port2(Lower 4bits)
2Gbps	256 Msps	8	64 MHz	Port1
4Gbps	2048 Msps	2	64 MHz	Port1(MSB) + Port2(LSB)
4Gbps	1024 Msps	4	64 MHz	Port1(Upper 2bits) + Port2(Lower 2bits)
4Gbps	512 Msps	8	64 MHz	Port1(Upper 4bits) + Port2(Lower 4bits)

Figure 1. Front view of ADS-3000.

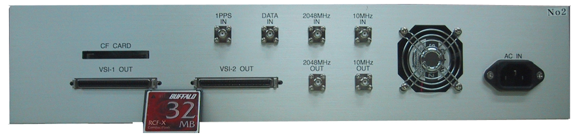

Figure 2. Rear view of ADS-3000. FPGA logic is easily programmable with a CompactFlash card, or an Ethernet port which will be equipped after the next upgrade. 2048-MHz PLL-output port and 2048-MHz input port are directly connected in most cases. 2048-MHz reference signal can be distributed to other units by using these ports.

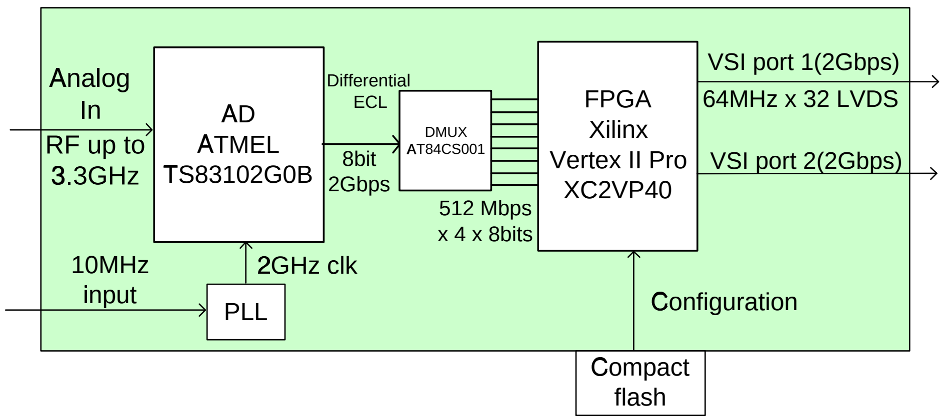

Figure 3. Schematic diagram of ADS-3000.

3. Applications

By configuring the FPGA device, a wide range of applications will be possible such as digital baseband converter for multi-channel geodetic VLBI, software demodulator for spacecraft downlink signal in spacecraft VLBI or satellite communications, or spectrometer for broadband astronomical observations (see Table 2). Some applications can be realized with free IP (Intellectual Property) cores distributed by FPGA vendors. Digital baseband converter (DBBC) is one of the expected applications, which substitutes the conventional multi-channel analog baseband converters. If the input IF signals are band-limited and 128Msps mode is available, general-purpose IP-core product [3] can be used for it. To utilize the full 1 GHz band, the input signal to the DBBC should be multiplexed and the dedicated parallel-processing digital mixer circuit, in which the number of bits is lower than general-purpose ones, should be used. Such FPGA-based DBBC systems dedicated to the backend system of radio telescopes have already been developed and used in several projects (See [4],[5],[6]). DBBC is also useful in differential VLBI observations for spacecraft navigations. In the observations, the target source is switched between spacecraft and phase-reference quasars in order to cancel out phase variations. To ensure a sufficient number of phase-reference quasars near the spacecraft, wide-bandwidth IF sampling is effective. On the other hand, DBBC is useful for spacecraft observations because the bandwidth of the spacecraft signals is very narrow. Using the digital BBC system, the total data size can be reduced and the signal-to-noise ratio of the data can be improved for the narrowband spacecraft signals. Moreover, it is easy to compensate for the Doppler shift of the spacecraft signals by real-time tuning with direct digital synthesizer. Because the phase relationship is preserved through the baseband conversion processes, we can use wideband quasar signals as phase reference for narrowband spacecraft signals.

Table 2. Expected applications realized by FPGA IP cores.

Applications	**Available IP-cores**
DC-cut,RFI mitigation	Substractor,FIR filter
DBBC	DBBC, FIR filter, DDS
Spectrometer, Wideband P-cal detector	FFT, Integrator
Format converter (K5,Mark 5,PC-EVN...)	CRC, Look-up table
Dispersion compensator for pulsar observations	FFT, Complex multiplier
Software receiver for satellite communications	FIR filter, DBBC

4. Observations

The first-ever 4-Gbps VLBI fringe was successfully detected (Fig.5) in the HAYABUSA spacecraft navigation differential VLBI experiments performed between Kashima 34m and Kashima 11m antennas on November 25-26, 2005. Two-sets of PC-VSI recorders [7] were used at each

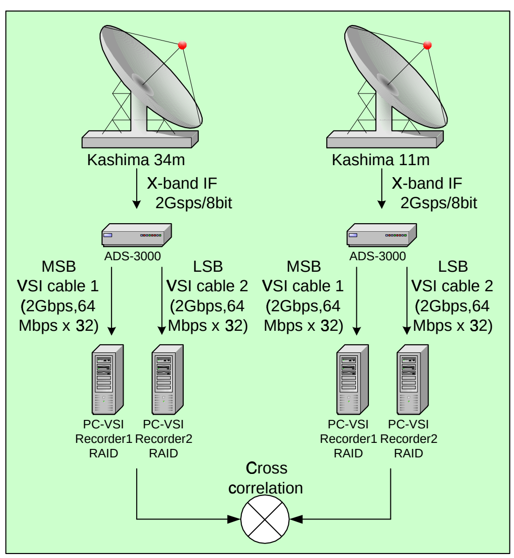

Figure 4. Schematic diagram of recording system for the 4-Gbps VLBI experiments.

station (Fig. 4). While 4-Gbps (2Gsps/2bit) of wide-bandwidth sampling mode was used for the scans for reference quasars, 512-Mbps/8bit mode was used to capture the high-SNR signals from HAYABUSA spacecraft.

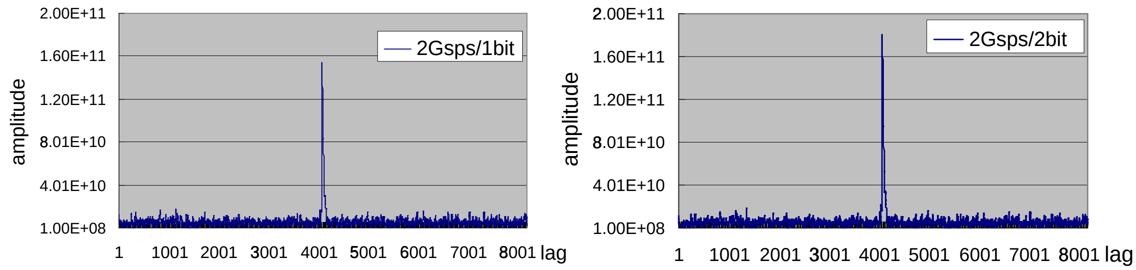

Figure 5. The first-ever 4-Gbps fringes between Kashima 34m and Kashima 11m antennas at X-band observation toward 3C273B on November 25,2005. Integration time is 4s. The over-sampling factor is 2, because the current IF bandwidth at Kashima 11m station is limited to 500 MHz. A correlation amplitude with 2-bit correlation was 123% of that with 1-bit correlation (using only the MSB data). This is consistent with the theoretical value of 124%(= 0.935/0.744).

5. Conclusion and Future Plan

We have developed a VSI-compliant 2048-Msps A/D sampler named ADS-3000, which is upward compatible with ADS-1000. The first-ever 4-Gbps (2 Gsps/2 bits) VLBI experiments were successfully carried out using the samplers. This sampler has an FPGA-based extensibility to enable it to be used for a wide range of applications. We expect that it will be used for not only a VLBI observation but also a general-purpose experiment which requires precise time label. We will install an FPGA-based DBBC system to perform spacecraft-navigation differential VLBI experiments, in which wideband IF signals are directly recorded in the scans for reference quasars and digitally extracted baseband signals are recorded for the narrow-band signals from spacecrafts to measure phase delays.

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