Effect of Area Array Package Types on Assembly Reliability
And Comments on IPC-9701A

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Abstract

Status of thermal cycle test results for a nonfunctional daisy-chained peripheral ceramic column grid array (CCGA) and its plastic ball grid array (PBGA) version, both having 560 I/Os, were presented in the last year conference. Test results included environmental data for three different thermal cycle regimes (-55/125°C, -55/100°C, and -50/75°C). The updated findings for these test vehicles with two different package types will be presented.

In a recent reliability investigation a fully populated CCGA with 717 I/Os was also considered for assembly reliability evaluation. The functional package is a field programmable gate array that has much higher processing power than its previous version. This new package is smaller in dimension, has no interposer, and has a thinner column wrapped with copper for reliability improvement. This paper will also present thermal cycle test results for this package assembly and its plastic version with 728 I/Os, which were exposed to two different cycle regimes. The cycle profiles were those specified by IPC-9701A for tin-lead, i.e. -55 to 100°C and -55 to 125°C. Per IPC-9701A, test vehicles were built using daisy chain package and were continuously monitored. The effects of many process and assembly variables including corner staking, commonly used for improving resistance to mechanical loading such as drop and vibration loads, were also considered as part of the test matrix. Optical photomicrographs were taken at various thermal cycle intervals to document damage progress and behavior. Representative samples of these along with cross-sectional photomicrographs at higher magnification taken by scanning electron microscopy (SEM) to determine crack propagation and failure analyses for packages are also presented. Appendix A was added to provide back-up information for IPC-9701A and discuss the effects of key thermal cycle parameters and projection for lead-free versus lead-based solder joints.

Key Words: Ceramic column grid array (CCGA), thermal cycle, staking, solder joint

Introduction

Ball grid arrays (BGAs) and chip scale packages (CSPs) are now widely used for many electronic applications, including portable and telecommunication products. Systems-in-a-package (SIP) development is the most recent response to further even increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. The BGA version has now started to be extensively implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. The plastic BGA version of the area array package, introduced in the late 1980s and implemented with great caution in the early 1990s was further evolved in the mid 1990s to the CSP (also known as fine pitch BGA) with a much finer pitch from 0.4mm to 0.3mm. Because of these developments, it is becoming even more difficult to distinguish different array packages by size and pitch.

Extensive work has been carried out by the JPL consortia in understanding technology implementation of area array packages for high reliability applications. These included process optimization, assembly reliability characterization, and the use of inspection tools, including X-ray and optical microscopy, for quality control and damage detection due to environmental exposures. Lessons learned by the JPL-lead team have been continuously published [1-5].

BGA packages with 1.27 mm pitch have been the packages of choice for commercial applications. However recently, a ceramic package version specifically tailored for high reliability applications was used to provide processing power required for the Spirit and Opportunity Mars Rovers built by NASA-JPL. Both Rovers successfully completed their 3-months mission requirements and continued exploring the Martian surface for many more moths, providing amazing new information on previous environmental condition of Mars and strong evidence that water exists on Mars. It is important to note that the field programmable gate array (FPGA) area array packages were kept in a benign warm electronic box (WEM) environment and the mission is considered to be relatively short. Electronics in WEM are heated in order to avoid exposure to the extreme Martian weather that could reach as low as -130°C. Thermal cycling represents the on-off environmental condition for most electronic products and therefore is a key factor that defines assembly reliability.

This paper will first provide a summary of most recent assembly reliability data presented in the literature for I/Os from 255 to 1657 and pitches to 1mm for CBGAs and CCGAs. It will then provide details on the design and assembly of experimental test vehicles, including the design of the test printed wiring board (PWB) and solder paste print efficiency using automatic and manual printing. Manual printing using a mini-stencil was needed in order to achieve the much higher localized solder paste print recommended for CCGAs. Failure mechanism changes due to two different maximum thermal cycle temperatures for the CCGA and PBGA are compared. Finally, thermal cycle data and cross-sectional photomicrographs for these packages under two different thermal cycle regimes are presented.

Literature Review on 2nd-Level CCGA Reliability

Area arrays come in many different package styles. These include plastic ball grid array (PBGA) with ball composition of eutectic Sn63Pb37 alloy or slight variations such as Sn60Pb40. The ceramic BGA package uses a higher melting ball (Pb90Sn10) with eutectic attachment to the die and board. The column grid array (CGA or CCGA) is similar to a BGA except that it uses column interconnects instead of balls. The lead-free CCGA uses a copper instead of high melting lead/tin column. The flip chip BGA (FCBGA) is similar to the BGA, except that a flip chip die rather than a wire bonded die is used.

Three array configurations are popular. These are a) full array; b) staggered array; and c) peripheral array. Plastic packages come in all styles, whereas ceramic package are generally limited to a full array configuration. Fully populated array packages presents some significant routing challenges if a conventional PWB with plated through-hole (PTH) vias are considered for the design. Peripheral plastic packages have been developed to reduce solder joint failures at the die edge as well as to improve routability characteristics. However, for ceramic packages there is a lesser need for a peripheral array because the CTE mismatch between die and package material is negligible. Hence, most ceramic packages are supplied in full array configuration including CCGA717 I/Os used in this investigation. Note though that the CCGA560 used in previous investigation was a peripheral array since the package pad pattern simulates its plastic package version.

Table 1 lists cycles to failure for a number of CCGAs/CBGAs with different configurations, selected from very limited data reported in the literature. Data were chosen to illustrate the effects of a few key parameters on reliability. The following parameters were considered when test data were tabulated even though in some cases specific information was not reported and is missing.

Thermal cycle range, ramp rate, dwell times
- For example, the CT50%F (cycles-to-fifty percent-failure) for a CBGA 361 over the range of 0/100°C was 4535 cycles (Case #2). It reduced to 1190 cycles when the temperature range increased to –55/110°C (Case #6)

Package size, thickness, materials, configuration, and I/Os
- For example, comparing Case#2 to Case#3, a relatively large reduction in CT50%F is effected when the package thickness is increased from 0.8mm to 1.2 mm (4535 vs 2700 cycles). When package thickness is further increased to 2.9 mm, the CT50%F drops further by a reduction of 3.2 times relative to the package with 0.8mm thickness. A similar reduction was observed for the CCGA with 1657 I/Os when the package thickness increased from 1.5 mm to 3.7 mm (Case #13). Reliability decreases by increasing package I/O since this means increasing the distance to the neutral point. The CT50%F reduced from 4535 cycles to 2462 cycles when the number of I/Os for the 0.8 mm thick package increased from 361 to 625 (Case #2 vs Case #5). Use of higher CTE ceramic materials, in order to better match the ceramic CTE to the PWB CTE, will also improve the reliability. For example, compare Case #6 to the Case #7 for the 361 I/O CBGA assemblies. CT50%F increased from 1190 to 2160 cycles for the HiCTE package.

Die size and its relation to the package size and ball configuration
- The effects of die size and package configuration (full vs peripheral arrays) on reliability are more pronounced for plastic than for ceramic package assemblies.

PWB thickness, definition of pad, surface finish
- Preferred thickness was defined as 2.3 mm in IPC-9701A[6] since it is known that generally plastic packages assembled on thinner PWBs show higher cycles to failure. The effect of board thickness for ceramic packages has not yet been well established, but its effect may be less critical for column grid array assemblies than for plastic package assemblies, especially when the dominant failure is column.

Single side or double side, relative offset of package on top and bottom
- This is not shown here, but discussed by this author in another paper[7,-8]. Reliability decreased for the double-sided PBGA assembly. The author is not aware of any published data on this subject for CBGA/CCGAs.

Table 1 Cycles-to-failure data illustrating the effect of a number of key variables)

| Case #	Package (I/O, Pitch)	Package Size (die size) mm	Thermal Cycle Condition (ramp, dwell, Cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
1	CBGA-255-1.27	21x21 (1mm substrate)	0 to 100°C (10, 5, 2cycles/hr)	1980 (1% failure)	2426 ($N_{50\%}$)	PWB, 1.55mm Thk Ref. Burrnette (Motorola)
2	CBGA-361-1.27	25x25 (substrate 0.8 mm Thk)	0 to 100°C (3 cycles/hr)	NA	4535 ($N_{50\%}$)	Avg solder paste vol 5,900 mil^3 PWB, 1.57 mm Thk Die 15x10 mm
3	CBGA-361-1.27	25x25 (substrate 1.2 mm Thk)	0 to 100°C (3 cycles/hr)	NA	2700 ($N_{50\%}$)	Note: Increase from die Thk .8 to 1.2 and 2.9, reliability reduction by 1.8 and 3.2 times Ref Master, 1998
5	CBGA-625-1.27	32.5x32.5 (substrate 0.8mm Thk)	0 to 100°C (3 cycles/hr)	NA	2462 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref [9]
6	CBGA-361-1.27	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	890 (100 ppm)	1,190 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref [10]
7	CBGA-361-1.27-HiCTE Substrate	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	1,310 (100 ppm)	2,160 ($N_{50\%}$)	Substrate CTE, 12.2 ppm Ref [10]
8	CGA-361-1.27-Interposer	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	1,350 (100 ppm)	2,320 ($N_{50\%}$))	NTK Interposer CGA PWB, 1.57 Ref [10]
9	CGA-361-1.27- IBM	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	1,080 (100 ppm)	1,520 ($N_{50\%}$)	Ref [10]
10	CBGA-1681-1.27-HiTCE	42.5x42.5x1.85 substrate)	-25 to 125°C (1, 9min, 3 cycles/hr)	613 (1st failure)	1142 ($N_{50\%}$)	PWB, 93 mm Thk Ref [11]
11	CBGA-625-1.0	32x32x2.4mm (substrate)	0 to 100°C (2 cycles/hr)	NA	740 ($N_{50\%}$)	Ref [12] IBM-2003
12	CBGA937-1.0	32x32x1.5 (substrate) 32x32x2.4	0 to 100°C (2 cycles/hr)	NA	1,860 ($N_{50\%}$) 1,310 ($N_{50\%}$)	Reference M. Ref [12]

| 13 | CCGA1657-1.0 | 42x42x1.5 42x42x2.55 42x42x3.7 | 0 to 100°C (2 cycles/hr) | NA | 1,530 ($N_{50\%}$) 990 ($N_{50\%}$) 620 ($N_{50\%}$) | Ref [12] |
| 14 | CCGA 1657-1.0 Cu | 42.5x42.5x 2.55 | 0 to 100°C (2 cycles/hr) | 1660 (1st failure) | 2410 ($N_{50\%}$) | Cu Column, solder paste 96.5 Sn3.5Ag Ref [13] |

Tin-lead and lead-free solders, ceramic column grid array (CCGA)

Figure 1 shows SEM photomicrographs and cross-sections of the 560 CCGA assemblies after cracking due to thermal cycling. Figure 2 shows the microstructure of another CCGA package assembled with lead-free (Sn/Ag/Cu) solder paste [14, 15]. For CCGA assemblies, the 3D optical microscopy and visual inspection are limited to inspection of the outer rows. Such inspection can be performed only when sufficient gaps are allowed between the assembled parts. The assemblies show signs of damage/cracking after thermal cycling.
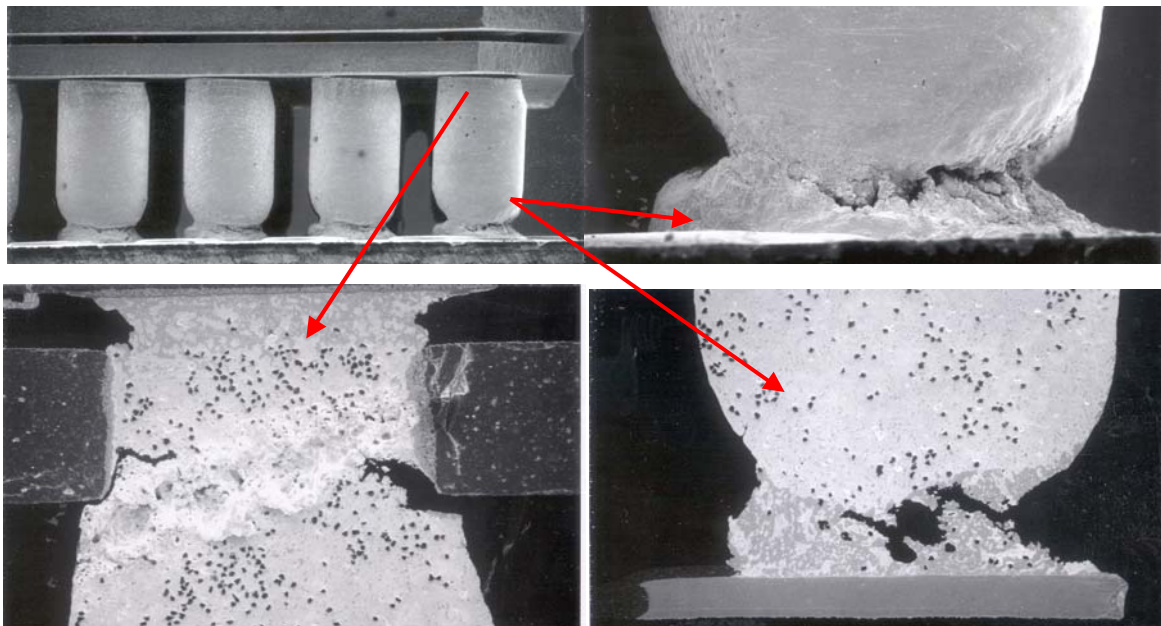
Figure 1 SEM photomicrographs and cross-sections of CCGA560 I/O assembled with tin-lead solder after thermal cycling showing damage/cracks
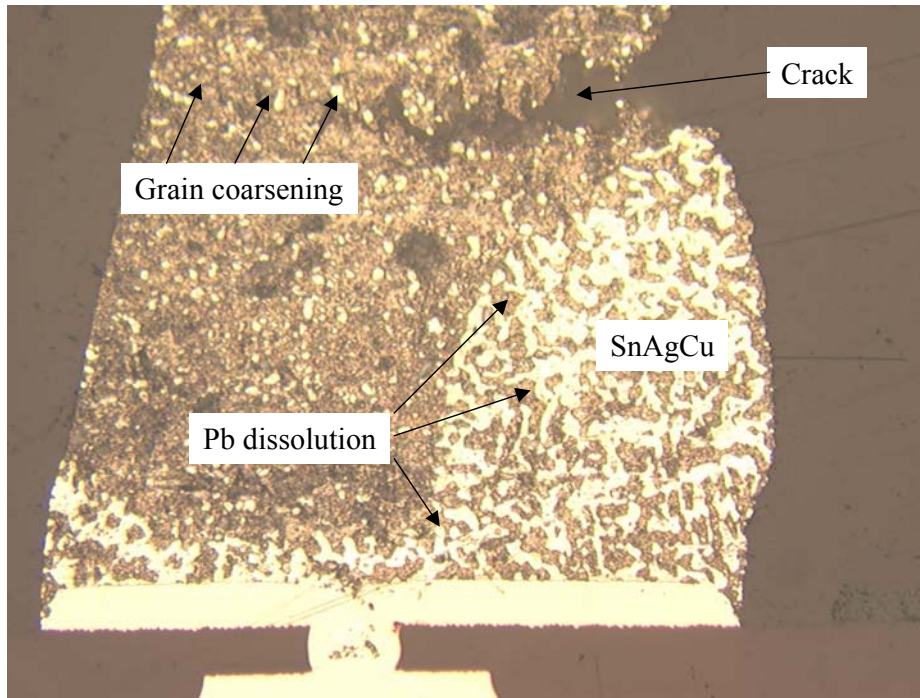
Figure 2 1657 I/O CCGA high-lead solder column on microvia pad PWB with Sn-Ag-Cu solder joints (Courtesy of Dr. D. Shangguan/T. Castello)

IPC Standard for Thermal Cycle Performance Requirement for SMT Assemblies

An industry-wide guideline document, IPC-SM785 for accelerated reliability testing of solder attachment, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, has been in use for more than a decade. Only recently industry has agreed to release an industry-wide specification, IPC-9701, in response to BGA and CSP technology implementation[6]. The IPC-SM785 guideline, although very valuable and still valid, did not answer the key question of what the data means in terms of product application and data comparison. As has been well established by industry and the JPL Consortia [1-5], many variables could be manipulated to either favor or disfavor test results. Considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing intermetallic rather than solder joint failure. This is especially likely for a novice user/supplier.

The IPC 9701 specification addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, numerous materials and process parameters including the following were specified.

- Specified 0.093 inch for PWB (e.g. FR-4) thickness in order to minimize bending and to achieve conservative values on cycles-to-failure data
- Limited surface finish choice to OSP (organic solder preservative) and HASL(hot air solder level) in order to eliminate potential of intermetallic failure
- Limited pad configuration to NSMD (non solder mask defined or Cu defined) in order to eliminate failure due to stress riser (non solder mask defined)
- Defined PWB-pad size to be 80% to 100% of package-pad size in order to have a realistic failure

The newest revision, IPC-9701A has updated to include guidelines for lead-free solder alloys. The appendix added to the specification requirement establishes guidelines for modifications required for lead-free solder joints. References to newly released documents on this subject, manufacturing of test vehicles, and thermal cycle profiles are also included. Recommendations for changes in the thermal cycle profile were given based on current industry understanding and test results. Data on the impact of various thermal cycle profiles on the results of accelerated testing in comparison to lead-based solder are still being gathered by industry with no unique conclusions as their relative reliability. Examples of such conflicts are shown in Appendix A. This appendix provides examples of test data and modeling approaches that are currently considered to better define the effects of various thermal cycle parameters on accelerated test results and projection for product reliability. Lack of field reliability data for lead-free electronic products make reliability comparison with tin-lead based on accelerated laboratory test data even more difficult.

For the SAC (SnAgCu) lead-free solder alloys, dwell (soak) time might be required to be increased in order to accommodate their slower creep rates. Requirement for increased dwell specified as another condition when experimental comparison between tin-lead and lead-free solder alloys are deemed to be necessary. The two conditions are as follows:

- Condition D10 (10 minute dwell), requiring 10-minute dwells at the hot/cold temperature extremes. Possibly the most efficient accelerated thermal cycle profile since it induces the most strain energy per unit of time (considering the entire cycle) or per unit dwell time. Cycles-to-failure data generated under this condition should generally be used as stand-alone only and only when damage accumulation is understood by modeling. The test results could be used for comparison to those of lead-based solder assemblies to show theoretically whether their performance is better or worse.

- Condition D30$^+$ (30 minutes or higher dwell), requiring condition requires dwells of 30 minutes and higher (60 minutes) at the hot/cold temperature extremes in order to induce experimentally creep damage somewhat comparable to lead-based solder. Modeling in conjunction with experimental data at different dwell times may be required to better define such comparison.

An OSP surface is recommended for the lead-free base solder alloys. For tin-lead, the acceptable surface finish was HASL. HASL is no longer allowed because is a lead-based alloy, it is not compatible with lead-free solder interconnections. Other surface finishes including silver (Ag) and tin (Sn) can be used for the manufacturer's internal data comparison. A nickel/gold (Ni/Au) surface also can be used for internal data comparison; however, there is a risk of introducing an intended brittle failure. The thermal cycle (TC) test ranges, test profile, and the number of test cycles (NTC) reported were also standardized. These include the reference cycle in the range of 0 to 100° C (TC1) and the severe military cycle condition of –55 to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTC varied from a minimum value of 200 cycles to a reference value of 6000 cycles.

Objectives

The purpose of this investigation was to characterize the reliability of area array packages with 560, 717, and 728 I/Os. Preliminary results of the 560 I/O packages were previously given in the APEX conference [2004] included ceramic column grid array and its plastic counterparts with the same peripheral package configuration. The new version of this field programmable gate array package with higher processing power is smaller in dimension and of less weight and is fully populated with 728 I/Os in the plastic configuration and 717 I/Os in the ceramic column grid array (CCGA) package (see Figure 3). For the CCGA 717, the 3-corner solder columns have been removed by the package manufacturer to improve reliability (Figure 3). Comparing this Figure to Figure 1 for the CCGA 560 I/O package, it is evident that the columns for the CCGA 717 I/Os are thinner and present different features.

In addition to the package type and size, a design of experiment (DOE) was utilized to cover many aspects that are considered to be unique for the potential use of these packages for high reliability applications. Solder joint reliability is affected by many variables as briefly discussed in the previous section. The following parameters were either characterized or evaluated as part of the DOE implementation.

- Two pad designs, one for CCGA 560 I/Os and smaller pads for the PBGA attachment. PBGAs were assembled on both pad sizes to evaluate PBGA interchangeability with the CCGA.
- Both CCGA 717 I/Os and 728 I/Os were assembled on pad design for the CCGA 717 I/Os. PBGA corner balls were removed in the PBGA 728 assembly to utilize the 717 I/O pad pattern (Figure 4).
- Four different stencil designs, a relatively thicker mini-stencil up to 10.5 mil thick especially designed for the CCGA 560, and an 8 mil thick stencil designed for the CCGA 717 I/Os, and a standard 6 mil thick stencil to assemble PBGA and other surface mount packages. Solder paste print volumes were significantly varied depending on package types, stencil design , and paste printing process.
- CCGA and PBGA assemblies without and with corner stake adhesive bonds as well as conformal coat. Corner adhesive bonds are used to improve resistance to mechanical vibration and shock loads.
- A number of packages were assembled using a rework station to establish reliability differences for assemblies built with a vapor phase reflow machine and a rework station.

The assemblies were subjected to three types of thermal cycles. The process and results for reliability of CCGA package assemblies are discussed and compared to their PBGA counterparts in the following.
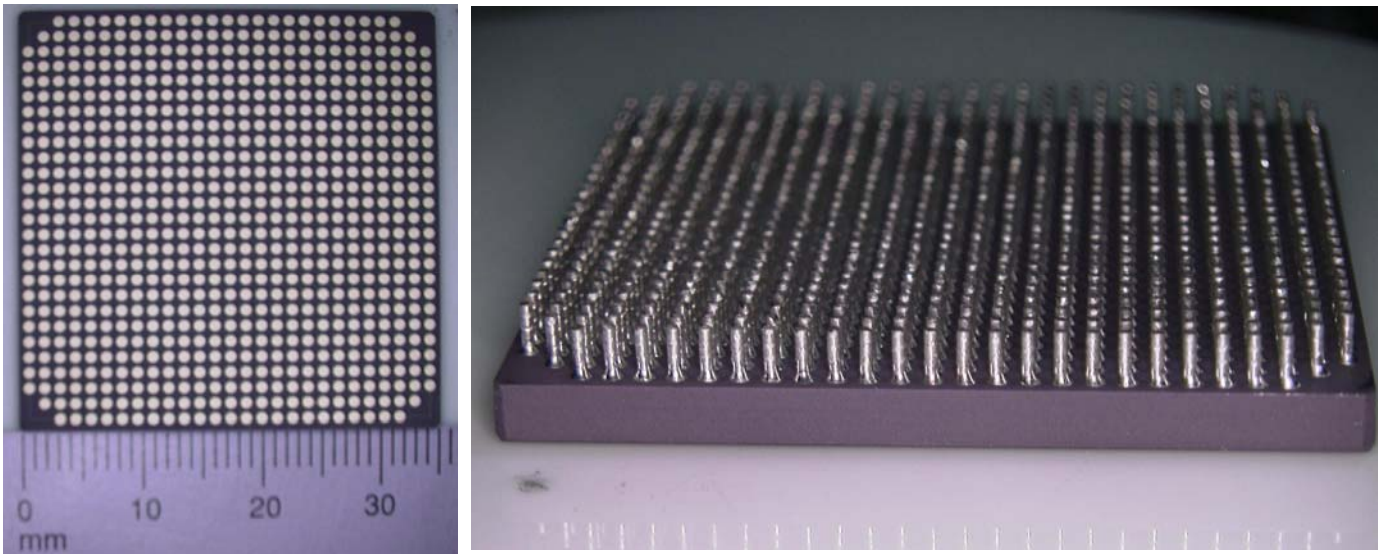
Figure 3 Photomicrograph of CCGA 717 I/O package dimension and its column feature showing no corner columns for reliability improvement
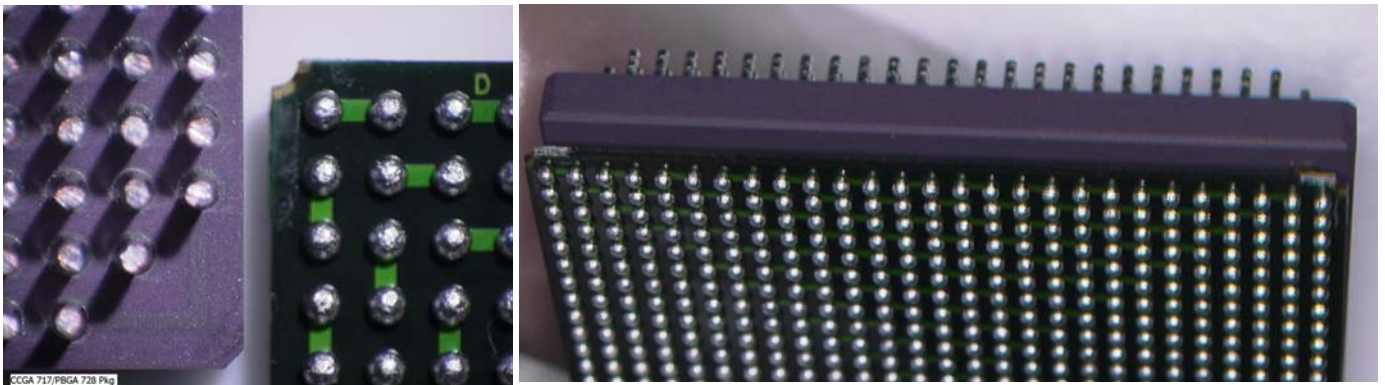
Figure 4 Photomicrograph of CCGA 717 I/O and its plastic counterparts with corner balls. Corner balls have to be removed in order to assemble the PBGA package on the CCGA PWB pad design.

Test Vehicle

For the CCGA/PBGA 560 I/Os, a polyimide printed wiring board (PWB) was designed to accommodate two pad configurations, one for the PBGA and the other for the column grid array [16]. The pad size for the PBGA was 24 mils, whereas for the CCGA it was 33 mils. They pads were connected through their plated through hole via (PTHV) with 24 mil diameter. The specific pairs of PWB pads designed such that their connections within a package pair after assembly completed daisy chain patterns. Four key daisy chains for each package were used for continuous monitoring during thermal cycling. Four additional pads were added at each side of the package for manual probing and failure identification. For the CCGA 717 I/O and PBGA 728 I/Os, a high temperature FR-4 PWB with 0.091 inch thickness as specified by IPC-9701A, with 32 mil pads connected to through hole vias was used. Figure 5 shows an assembled test vehicle having both CCGA and PBGA packages. Note the input and output traces extended to the board edge and also the probing pads at package peripheral for manually detecting failures.
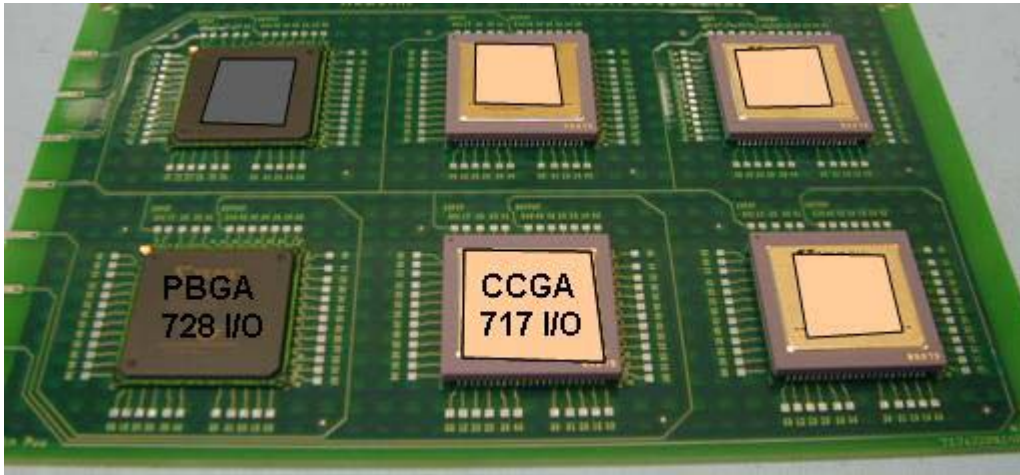
Figure 5 PWB design showing design-chained CCGA and PBGA packages, probing pads, and via daisy chains

The PWB's pads had HASL (Hot Air Solder Level) surface finish. HASL and OSP surface finishes are specified in IPC-9701A as the recommended surface finishes for solder attachment reliability evaluation of tin-lead solder alloy. This is to avoid potential immature intermetallic failures such as those occasionally observed for the Au/Ni surface finish. Only the OSP surface finish is recommended for lead-free solder alloys.

Stencil Design, Paste Print, and Volume Measurement

Table 2 lists estimated solder paste volumes that can be achieved with different stencil thicknesses and aperture openings. The 6 and 7 mil stencil thicknesses represent the general stencil that could be used for paste application on PBGA and other package pad patterns. The mini-stencil with 8 and 10.5 mil thicknesses were used only for the manual paste print application for CCGA in order to achieve the higher paste volume recommended by the package supplier. In one case, a step down stencil design from 8 mil to 6 mil thickness was used to accommodate both the CCGA assembly and other finer pitch standard surface mount packages. For this case, numerous conventional packages had to be hand soldered since they were masked during automatic stencil printing. CCGAs were assembled in two facilities. In each facility their approved RMA paste was used.

Table 2 Stencil parameter and solder volume

Solder volume	Solder volume (mil^3)	Stencil Type
BGA 560 I/O-Aperture 23 mil-Stencil 7mil	2909	Stencil
CCGA 560-Aperture 32 mil dia- stencil 7 mil	5632	Stencil
CCGA 560- Aperture 32 mil dia- Stencil 8 mil	6430	Stencil
CCGA 560-Aperture 32 mil dia- stencil 10.5 mil	8440	Mini stencil
PBGA 728- Aperture 6 mil dia- Stencil 28 mil	4823	MiniStencil
CCGA 717-Aperture 32 mil dia- stencil 8 mil	6430	Mini stencil

Two RMA pastes at two facilities, Type III (-325+500) mesh, were used for paste printing using automatic and normal manufacturing parameters. Manual paste printing was performed when the mini stencil was used. Each paste print on the PWB was visually inspected after printing for gross defects such as bridging or insufficient paste. Paste print quality was improved by adding paste when insufficient paste was detected and solder paste was removed when bridging was discovered. Special attention was given for the inspection of corner pads. Solder paste heights were measured using a two different laser profilometers and an optical microscope with 3D dimensional measurement capability. Measurement was carried out at numerous locations that included corner and peripheral center pads in order to accumulate solder volume data and their distributions.

An example of laser measurement for the top left corner and solder paste distribution values is shown in Figure 6. The specific tool provides automatic control for measurement and the maximum level cut-off value. These specific features made it very difficult to expand the measurement not only to larger values. This led on many occasion to wrong readings due to an abrupt paste print. Eventually, the print height had to be verified through filler gages and the uniformity of solder paste print

inspected by microscope. On the other hand, the 3D optical microscopy could reveal the distribution covering a larger area, but lacked accuracy (see Figure 7).
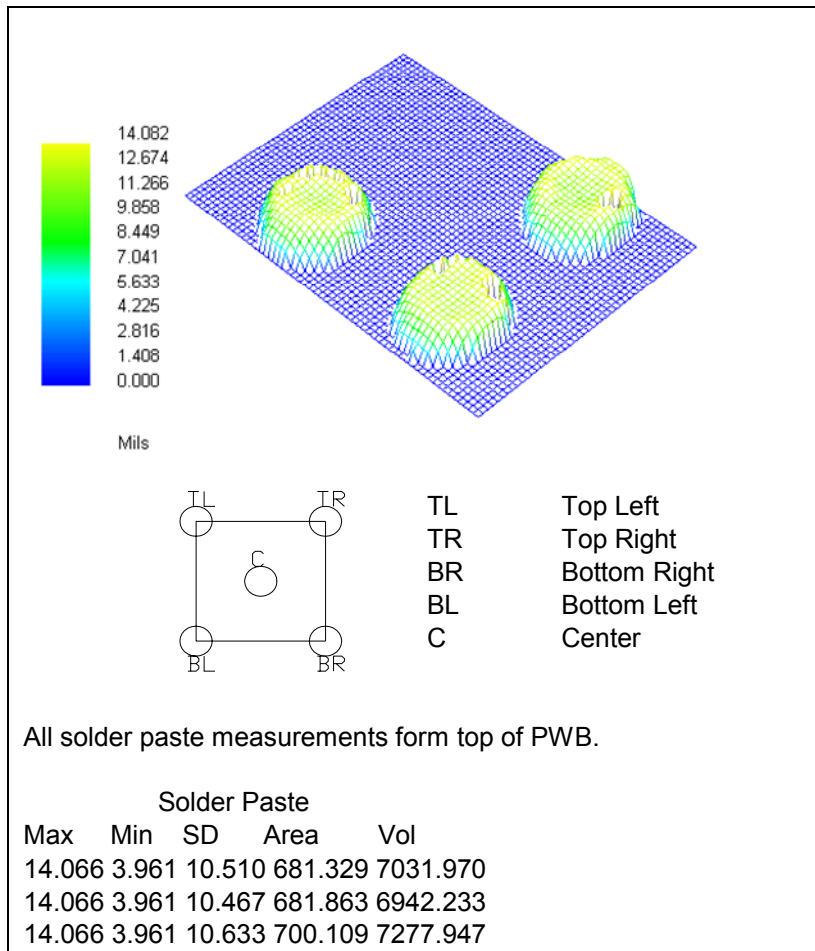

14.082
12.674
11.266
9.858
8.449
7.041
5.633
4.225
2.816
1.408
0.000

Mils

TL	Top Left
TR	Top Right
BR	Bottom Right
BL	Bottom Left
C	Center

All solder paste measurements form top of PWB.

Solder Paste

Max	Min	SD	Area	Vol
14.066	3.961	10.510	681.329	7031.970
14.066	3.961	10.467	681.863	6942.233
14.066	3.961	10.633	700.109	7277.947

Figure 6 Solder paste distribution using a laser profilometer showing calculated paste volume

CCGA 717 I/O
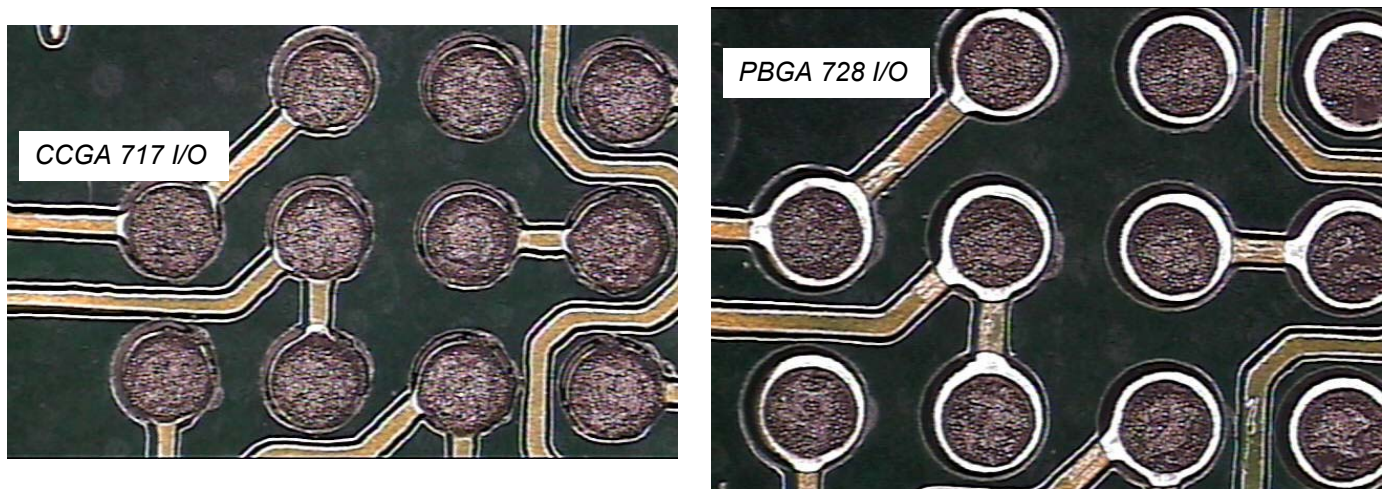
PBGA 728 I/O

Figure 7 Solder paste deposition for CCGA 717 and PBGA 728 using the pad design for CCGA 717 I/O. Higher solder paste volume is required for CCGA package assembly in order to achieve optimum reliability.

Test Results

Inspection before Environmental Tests

For high reliability electronic applications, visual inspection is traditionally performed by Quality Assurance Personnel at various levels of packaging and assembly, i.e., mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of criteria. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, etc. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space application, generally 100% visual inspection is performed at prepackage prior to its closure (precap) and after assembly prior to shipment.

Visual inspection is somewhat useful for the area array packages, but of no value for hidden balls and columns under the package. X-ray inspection is needed for area array packages. However, for CCGAs, the hidden solder joints could not be distinguished because of the heavy ceramic lid that inhibited X-ray penetration[7]. Visual inspection has a higher value for CBGA and CCGA assemblies since generally the solder fails at the exposed corners or periphery ball attachments. Peripheral balls and columns were inspected visually using an optical microscope at the start and during thermal cycling to document damage progress. Figure 8 shows photomicrographs of solder joints of CCGA 717 assemblies prior to thermal cycling. Note good solder joints with smooth surface adjacent to a joint with ridged solder.
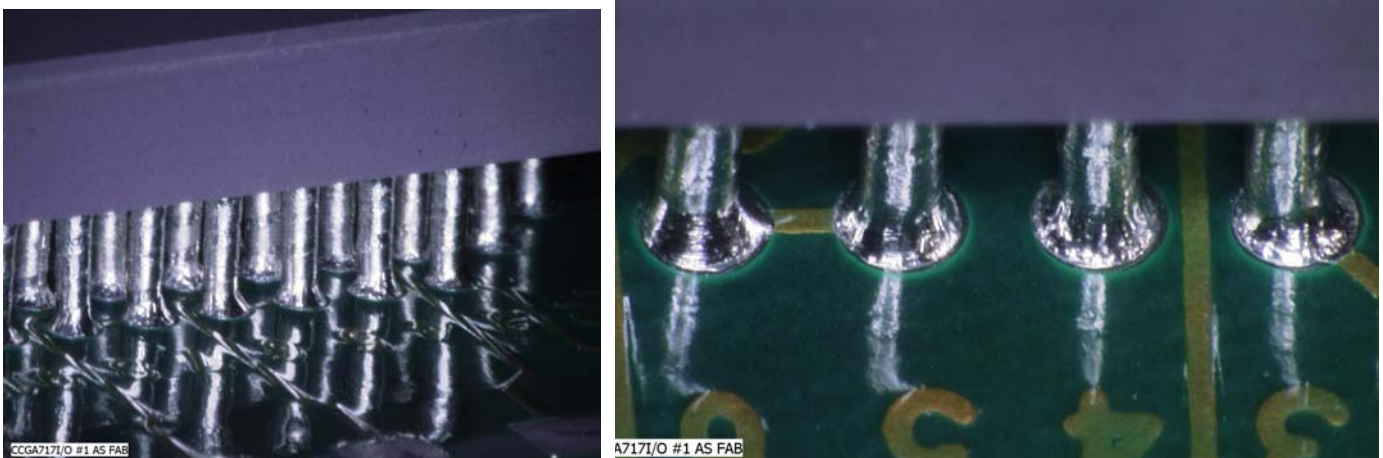
Figure 8 Optical Photomicrographs of PBGA and CCGA after assembly

Thermal Cycle Test Profile

Two different thermal cycle profiles were used. One is the same range specified by IPC9701A and the other one was specific to the mission specific thermal cycle range requirements. These were:

- Cycle A: The cycle A condition ranged from −50 to 75°C with a 2-5°C/min heating/cooling rate. Dwell at extreme temperatures was at least 10 minutes with a duration of 105 minutes for each cycle.
- Cycle B: The cycle B condition range from −55/100°C with 2-5°C/min. Dwell at extreme temperatures was 30 minutes.
- Cycle C: The cycle C condition ranged from −55 to 125 °C with a 2-5°C/min heating/cooling rate. Dwell at extreme temperatures was at least 10 minutes with a duration of 159 minutes for each cycle.

The criteria for an open solder joint specified in IPC-9701A were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, many additional interruptions within 10% of the cycle life were also observed. This was especially true for the ceramic packages. Open were manually verified after removal from the chamber at the earliest convenient time.

Test Results after Thermal Cycles

Figure 9 shows optical photomicrographs of a PBGA/CCGA 560 I/O assembly after 991 A condition (-50/75°C) thermal cycles. Even though no failure was yet observed. The solder joints showed some signs of damage. This is not significant if only solder interconnect to the board is considered. Figure 10 shows the first failure occurrence from a test vehicles detected by continuous monitoring at 1075 and removed at 1138 for inspection and failure verification. It is interesting to note that failure did not occur at the package site; therefore, solder joint damage at board interface may not be used as a representative of damage progress. In addition solder joint failure is not at the corner columns as expected.
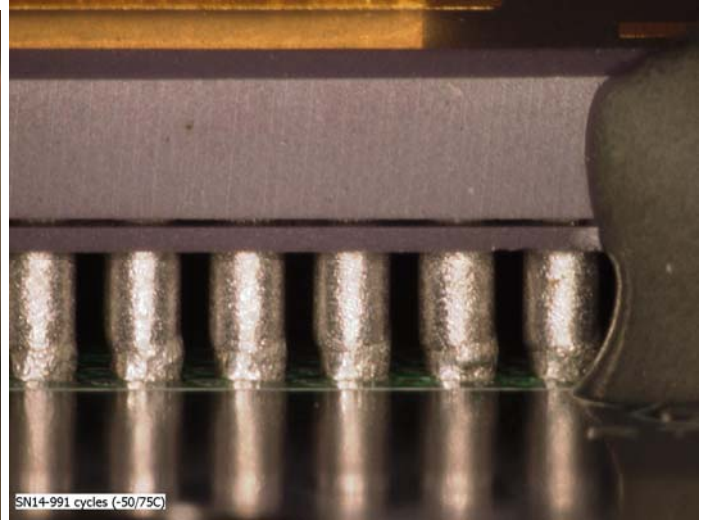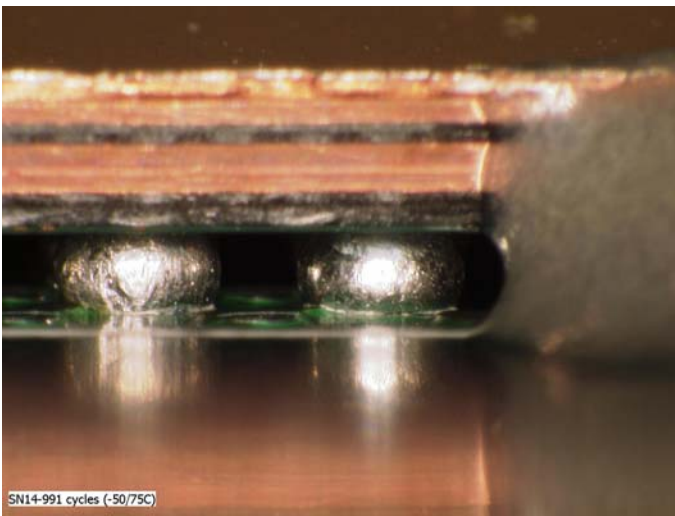
Figure 9 Optical photomicrographs of PBGA (left) and CCGA built with 105 mil thick stencil after 991 cycles (-50/75°C). Corner stakes are apparent on the right sides.
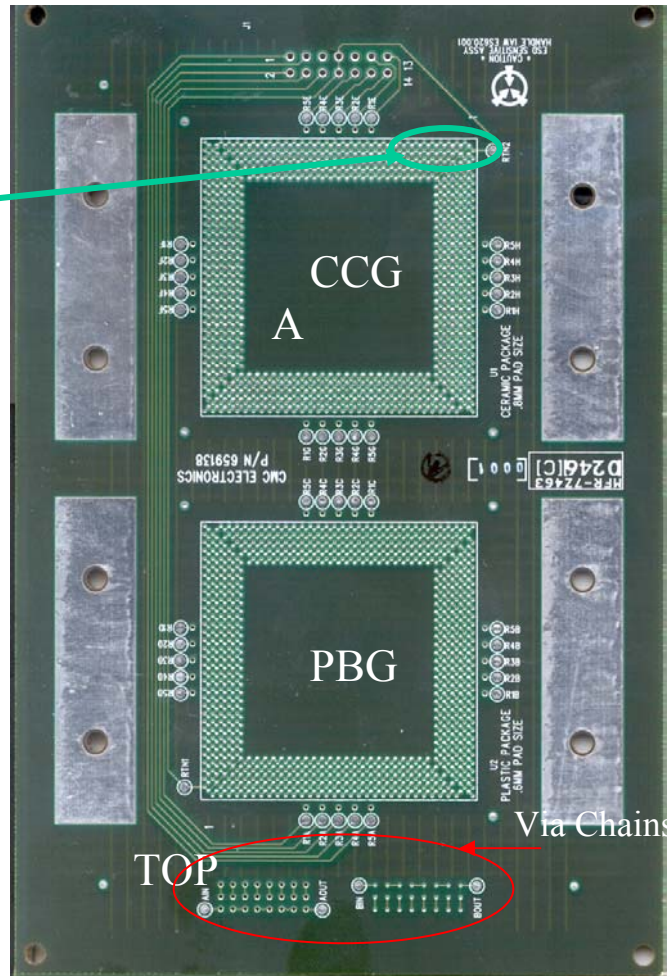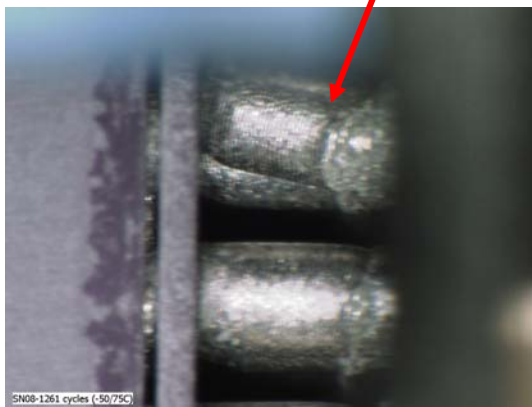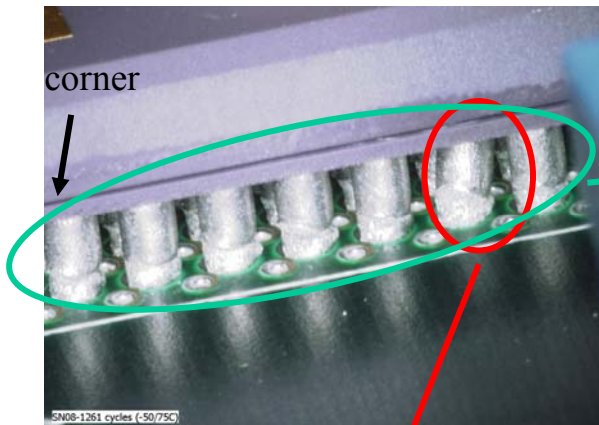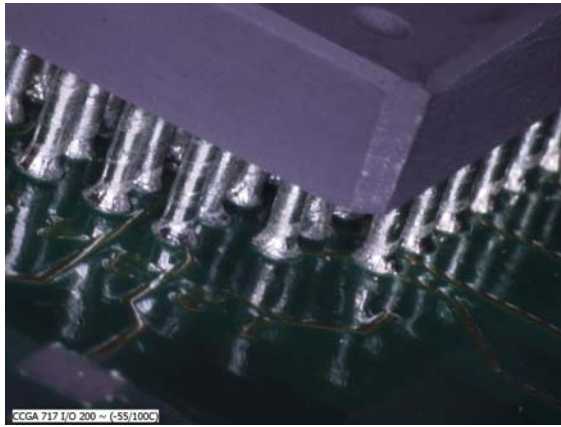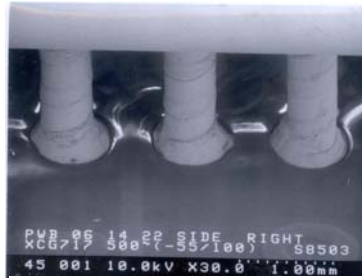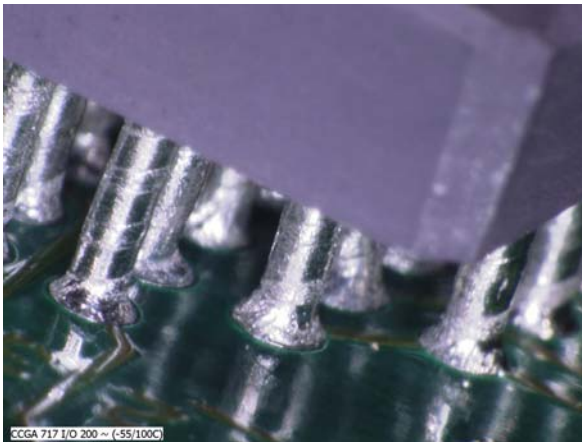

Figure 10 Optical photomicrographs of CCGA built with 10.5 mil thick stencil after 1138 cycles (-50/75°C). Note cracking from package site rather board site.

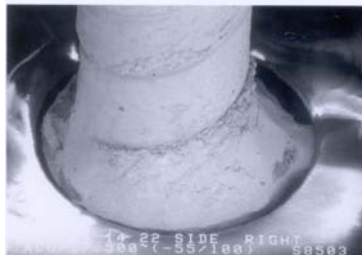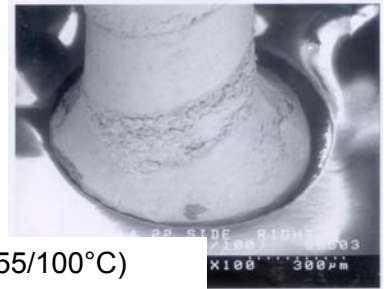Optical- 200 Thermal Cycles (-55/100°C)

SEM 500 Thermal Cycles (-55/100°C)

Figure 11 Optical photomicrographs of CCGA 717 I/O assembly (left) at 200 thermal cycles and their SEM Photomicrographs at 500 cycles. Some signs of damage at 500 cycles is apparent.

Conclusions

It is well established that solder joint reliability of plastic packages on polymeric boards is typically better than that of their ceramic counterparts. This trend was verified during our investigation. The current status of thermal cycles for the two CCGA package assemblies is as follows.

- Plastic package assemblies did not show failures to 2000 cycles whereas CCGA 560 I/O assemblies showed the first failure at 1075 cycles when they were subjected to –50/75°C cycle. The first failure was from the package site since a relatively high solder paste was used for assembly.
- The CCGA 717 I/O showed a minimal signs of solder joint damage at 500 cycles –55/100°C. These assemblies are being thermal cycled until failure.

Acknowledgements

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Appendix A
Back-up information for IPC-9701A
Discussion on Key Thermal Cycle Parameters and Projection for Lead-Free Vs Lead-Based Solder Joints

The appendix B of IPC-9701A establishes guidelines for modifications required to IPC-9701 for lead-free solder joints. Currently, there are only limited data and insight to determine acceleration factors and acceleration models for lead-free solders [1-13]. Data on the impact of various thermal cycle profiles on the results of accelerated testing in comparison to eutectic tin-lead solder are still being gathered by industry.

Acceleration thermal cycle test results especially when are compared to lead-free solder alloys are sometimes inaccurately assumed to be the same as product reliability. Correlations between acceleration test and product reliability for tin-lead are somewhat have been established during many years of investigation and product use whereas that is not true for less understood lead-free solder attachment. Reliability is the ability of a product, here surface mount solder attachments, to function under given conditions and for a specified period of time without exceeding acceptable failure levels. Therefore, comments such as lead-free solder joint is more or less reliable than standard tin-lead solder joint based on only laboratory test results are unsubstantiated Such general statements are incomplete when the lead-free alloy composition or/and when product information and use conditions are not specified. Product reliability needs to be estimated for solder joint under relevant use conditions.

Modification of IPC-9701 to include requirement for lead-free solder attachment thought to be an easy task at start since most information on thermal cycling for tin-lead were already well established. However, soon it became obvious that even a trend can not be established for acceleration thermal cycle based on literature data summarized by this author and are shown in Figure A1. Relative cycles to failures may be better or worse than tin-lead depending on package type, thermal cycle range, cycle profile, and dwell times at temperatures. For example, cycles to failures for lead-free PBGA 256 I/Os (plastic ball grid array) assemblies are about twice whereas for LCC (leadless ceramic chip carrier) are about half of tin-lead, respectively, when they were subjected to an accelerated thermal cycle in the range of -40 to 125°C. Temperature range and dwell time also affect relative accelerated failure cycles as apparent from test data generated for CBGA 625 I/Os under 0 to 100°C and -40 to 100°C.

Figures A2 to A7 were selected from a large number of plots in literature to demonstrate as how various authors have attempted to theoretically explain apparent contradiction on accelerated test results. Figures A2 to A4 show that projections can be made by using creep hysteresis loops (energy) as baseline for modeling. Figure A2 emphasizes that projection based on number of cycles are significantly different than those projected based on time. The effect of dwell time depends on temperature range and max temperature and such effect can be low to high as predicted by modeling in Figure A3. In Figure 5A, Dr. Jean-Paul Clech shows theoretically that the most efficient dwell times are 10 minutes and 3 minutes for SAC and SnPb solder joints, respectively. Based on a very limited test data, contrary to conventional understanding, he also postulates that thermal cycling at higher mean temperature may show improved cycles-to-failures when compared to a lower mean temperature (see Figure A6). The projections of accelerated test results from two conditions (-40/125°C and 0/100°C) to a use condition (30/80°C) is shown in Figure A7. Again, please remember that all these are based on accelerated thermal cycles in laboratory and are yet to be validated for product reliability based on field data.

Figure A8, provides additional interesting cycles-to-failure data generated under different thermal profiles for LCC84 I/Os ceramic package assembly. The effects of maximum dwell temperature as well as mean temperature are also investigated. Since this package induces high strain, the results even though interesting, it may not be representative of field application and should not extrapolated to other conditions without further verifications. Dr. Greg Henshall utilizes these and other test results to demonstrate his point of view on the effect of temperature as shown in Figures A9 and A10. Figure A11, shows another projection for a specific package configuration. It should be noted again that these acceleration factors (AFs) are developed for a specific package configuration and should not be used blindly.

Extensive discussions were made within the IPC-9701 committee team members as how to best capture the apparent conflicting accelerated test data and generate them into requirements. Initially, these figures were included in the Appendix B1 of IPC9701A to show different point of views within team members for specifying the dwell time requirement. However, based on comments received after its wider distribution to industry, these figures were removed from the specification and it was decided to include them in this Appendix as back up information. In addition, the Appendix B of IPC-9701A title was changed

to "*guideline*" rather its previous version as "requirement" since no industry-wide agreement could be reached on even the definition of thermal cycle profile. Based on numerous discussions within two years, two thermal cycle profiles were recommended for tin-silver-copper (SAC) solder attachment depending on the reliability approach and use conditions. These are:

- Condition D10 (10 minute dwell)- This condition requires 10-minute dwells at the hot/cold temperature extremes.
- Condition D30$^+$ (30-minutes or higher dwell)- This condition requires dwells of 30 minutes and higher (60 minutes) at the hot/cold temperature extremes.

Because of rapid implementation of lead-free solder alloys for electronic products and extensive knowledge-base on tin-lead, the IPC 6-10d committee members may be able to come to an industry-wide agreement on requirements. In the mean time, IPC 9706, guideline on lead-free implementation, is being generated to have more comprehensive guidelines on this highly demanded subject.
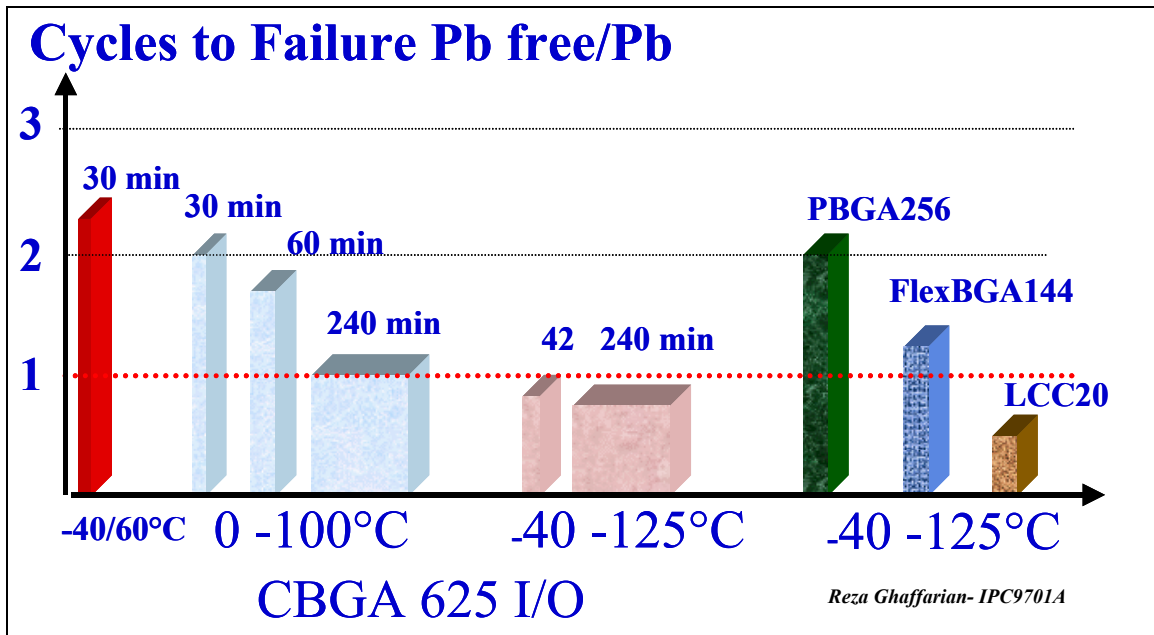
Figure A1 Cycles-to-failures for SAC (Sn-Ag-Cu) solder attachment depend on thermal cycle range and state of stress/strain (Courtesy Reza Ghaffarian, NASA-JPL, CIT), different source of data including [11].
Note: When comparing cycles-to-failure data for lead-free and lead-based solders, it should be noted that such comparison may not be valid since failures depend not only on the temperature cycle profile but also on the type of package and assembly configuration.
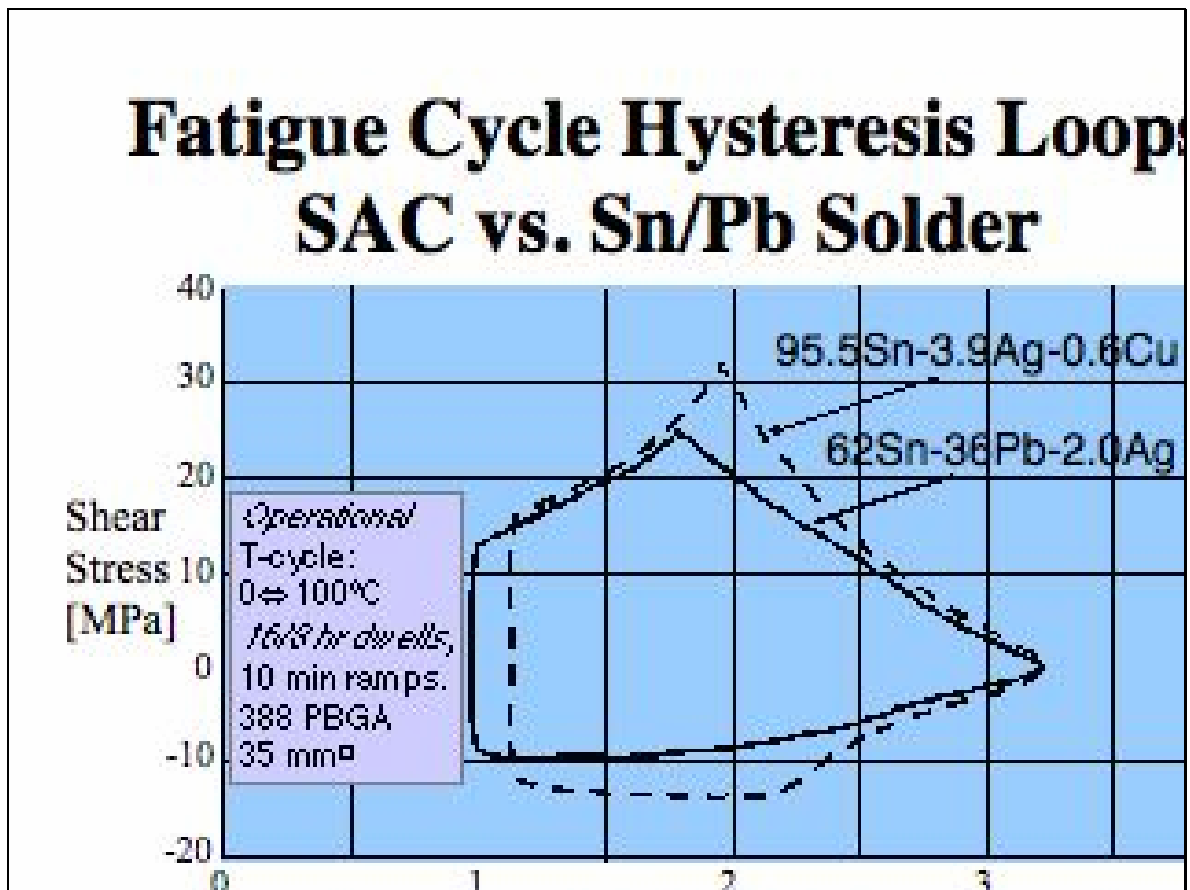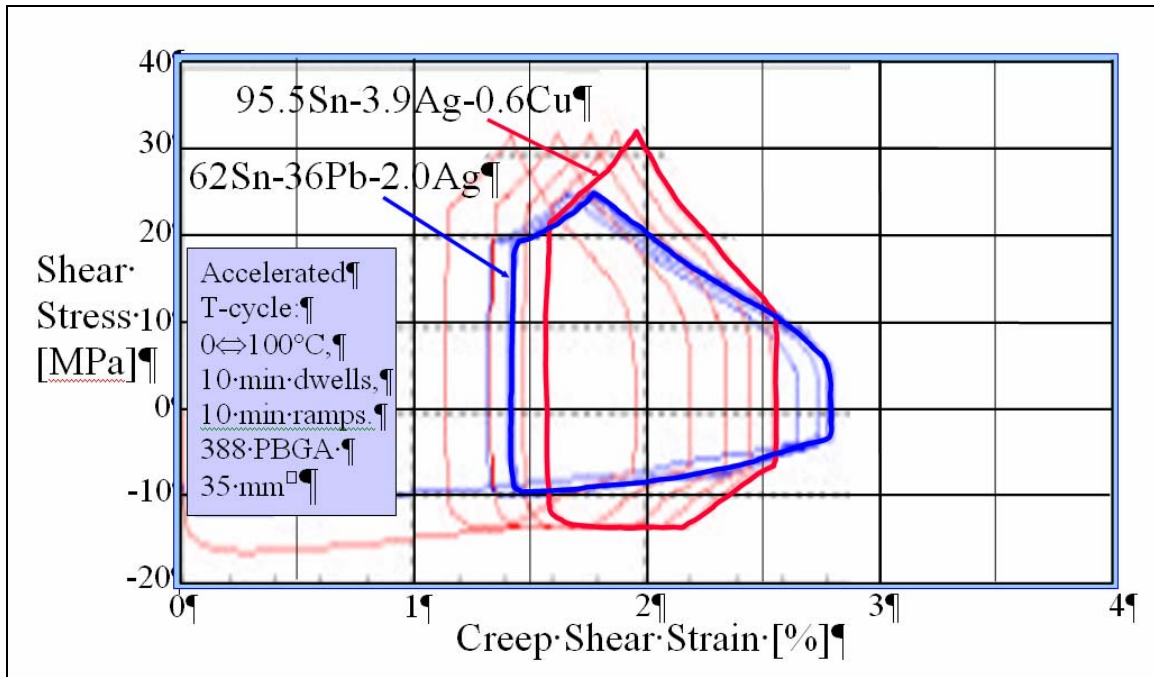
Figure A2 Fatigue cycle hysteresis comparison for lead-based and lead-free solder alloys at 10-minute dwells in accelerated reliability testing and operational environment dwells of 16 hours at hours at 0°C and 8 hours at 100°C for PBGA assembly. (Sources: ATC hysteresis loops--J. Lau, et al., and operating environment hysteresis loops--Werner Engelmaier)

Note: Acceleration thermal cycle and Operational cycle assumed to have the same temperature range of 0°C/100°C. The Acceleration Factors (AFs) are less than 1 (AF(N) <1) for both SnPb and SAC solder alloys; however, the much more important is that the AF for time is much larger than 1 (AF(t) ~ 20).
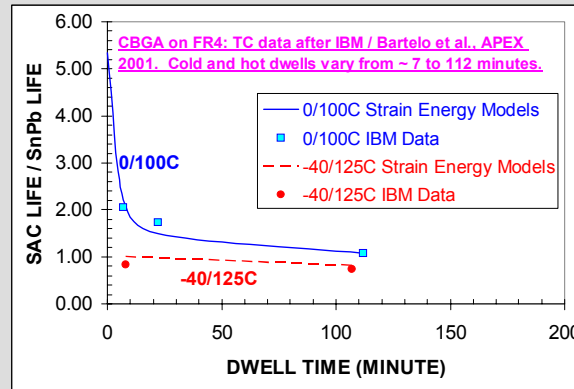
Figure A3 Effect of dwell time using CBGA data (Courtesy of Jean-Paul Clech)

Note: This clearly shows that for CBGAs, the effect of longer dwell time is of less importance for -40/125°C whereas it is significant for 0/100°C between 0-30 minutes and become of less significant beyond the 30 minute dwell.
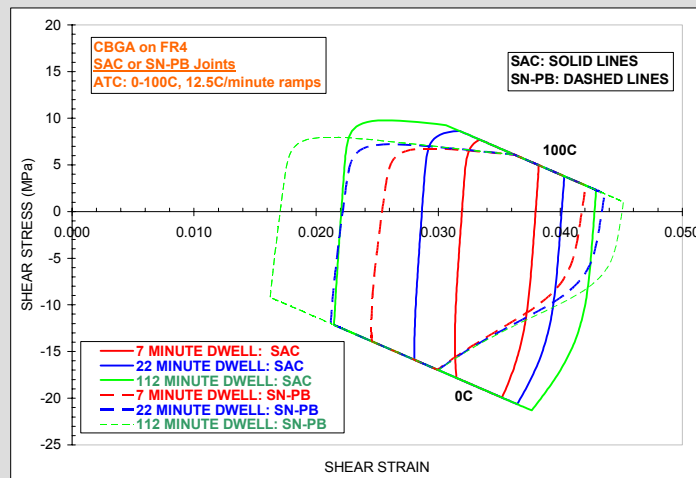
Figure A4 Effect of time on hysteresis loop for lead-free and lead-based solders (Courtesy of Jean-Paul Clech)

Note: Effect of time and temperature on cyclic hysteresis loops (the area represents the damage for each cycle) is different for lead-free and lead-based solders. Cycles-to-failure data for the two solder systems can be directly compared when damage for each cycle is understood and could be projected for use environment.
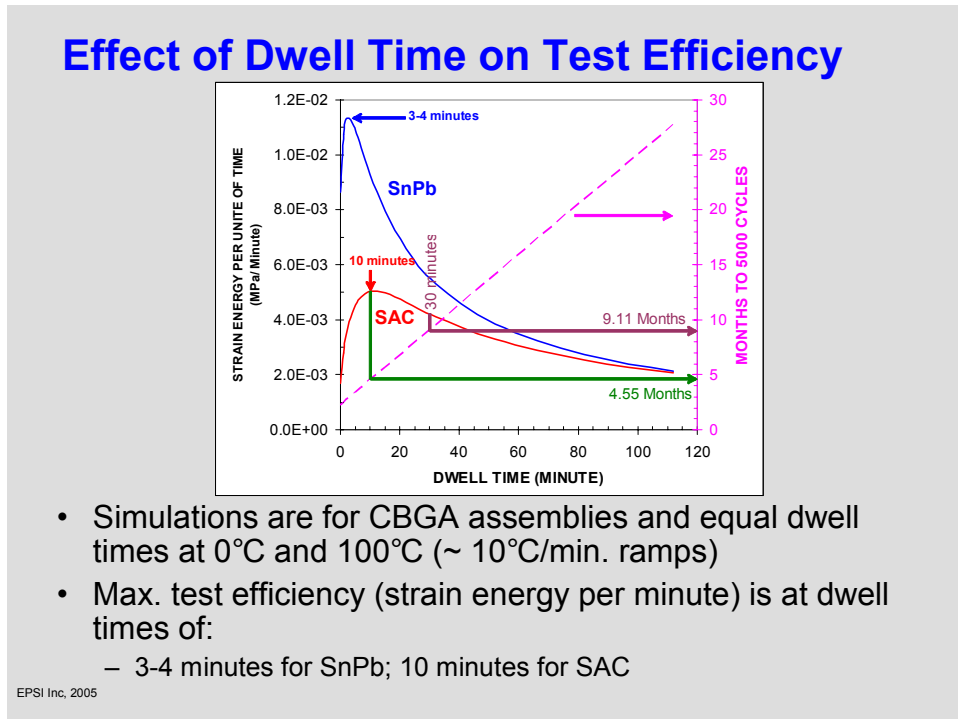

Effect of Dwell Time on Test Efficiency

- Simulations are for CBGA assemblies and equal dwell times at 0°C and 100°C (~ 10°C/min. ramps)
- Max. test efficiency (strain energy per minute) is at dwell times of:
  - 3-4 minutes for SnPb; 10 minutes for SAC

EPSI Inc, 2005

Figure A5 Effect of dwell time on thermal cycle test efficiency for CBGA(Courtesy of Jean-Paul Clech)

Note: For CBGA and lead-free solder, the strain energy per unit of dwell time shows that the 10 minute dwell provides the most damage density for this specific package and the specific thermal cycle range (0/100°C). Again, this efficiency will not be valid for other thermal cycle ranges and package types (see Figure A1).
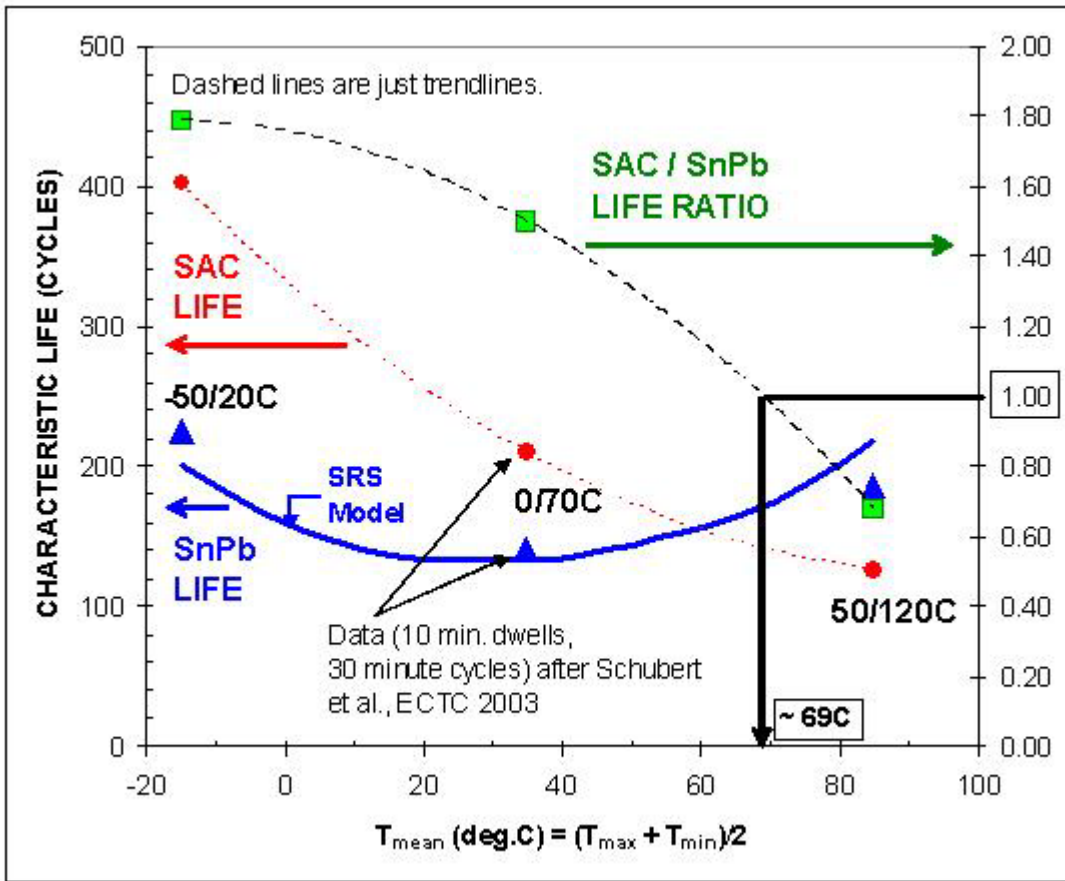
Figure A6 Characteristic life projection versus mean thermal cycle temperature for lead-free and lead-based solders (Courtesy of Jean-Paul Clech)

Note: Characteristic life projection dependency on the mean cycle temperature and dwell time
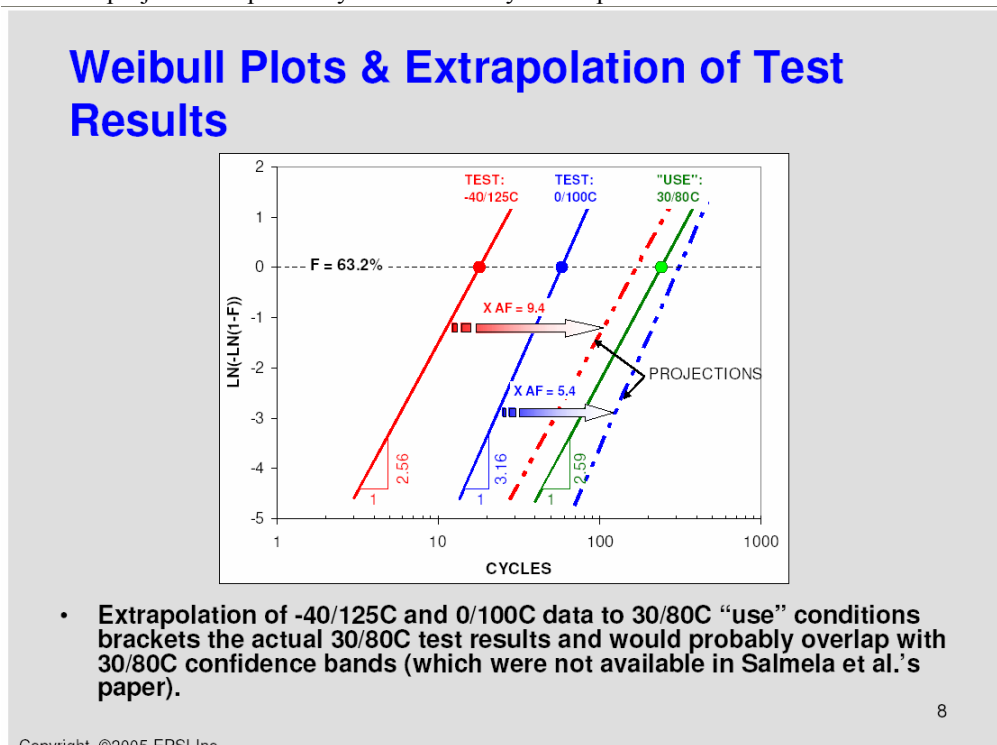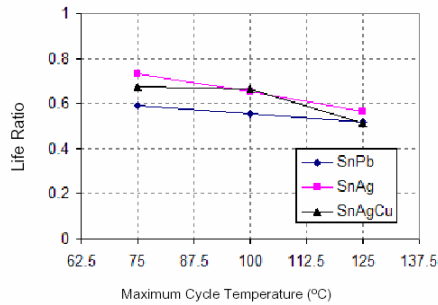

Figure A7 Extrapolation to use condition from two different sets of cycles-to-failure test data based on strain energy calculation for ceramic package (Courtesy of Jean-Paul Clech)

Note: The data are specific to the one type of ceramic package assembly only

Figure A8 Cycles-to-failure test results for 64 and 84 lead less package showing the effect of package, dwell time, and max temperature for a fix thermal cycle range of 100°C (Courtesy of CALCE EPSC, University of Maryland).

Note: It is interesting to note that for the temperature of above the 105°C, the 84 I/O package with longer 75 minute dwell time accumulated higher cycles before failure compared to a 15 minute dwell time. Solder joint for this package is under extremely high strain and its condition does not represent a typical solder joint assembly.
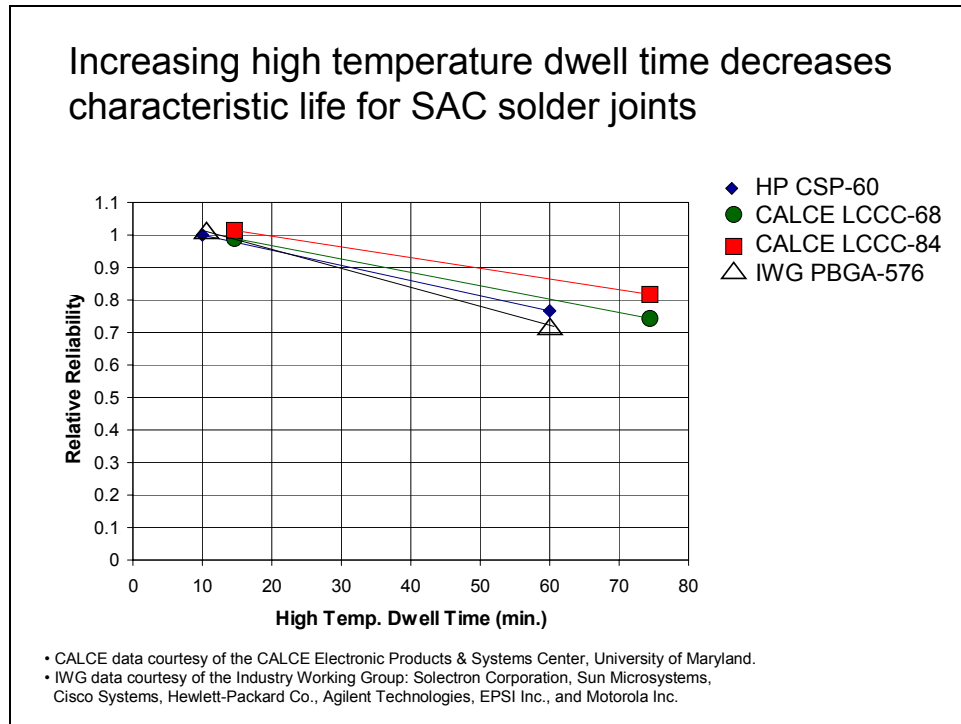
Figure A9 Relative cycles-to-failure for 100°C maximum temperature and various dwell times for different package styles (plot Courtesy of Gregory Henshall, HP) .

Note: For this specific maximum thermal cycle temperature, cycles-to-failures decrease as dwell time increases. As shown previously, this trend may not be always true for other temperatures and package types.
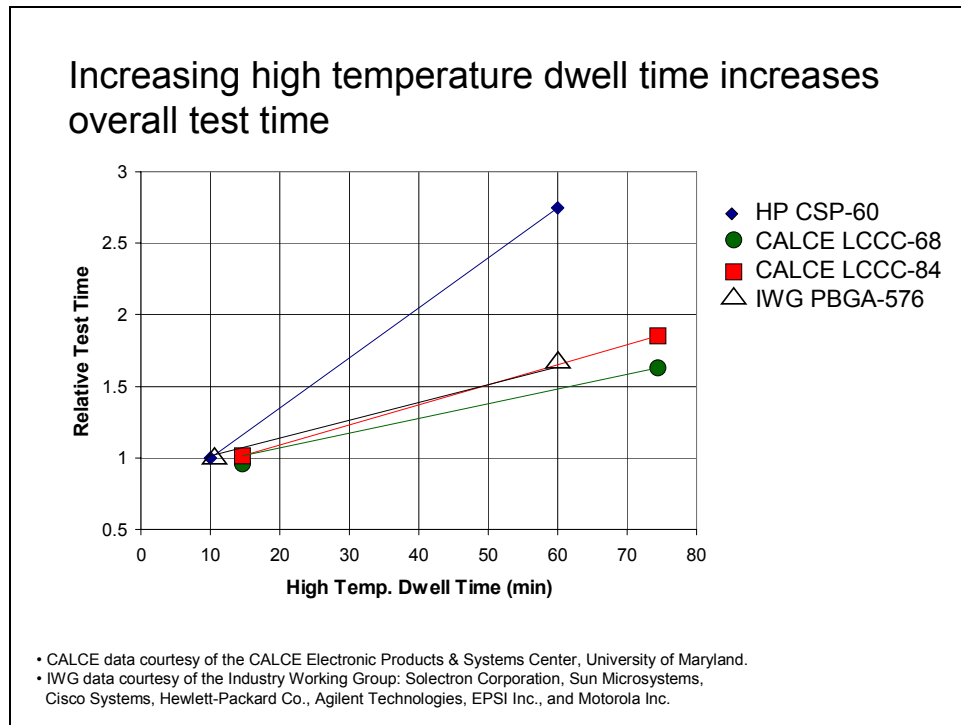

Figure A10 Relative thermal cycle test time versus dwell time at maximum temperature for different package styles (plot Courtesy of Gregory Henshall, HP) .

Note: Increase in time-to-failure increases as dwell time increases, longer dwell time is not the most efficient test, but may be a better representative of real environment

Model	Cycle	Solder	Mean number of cycles to gap cracking	Acceleration factor cycle 85 to -40	Acceleration factor cycle 85 to -40
			FEA		**Analytical (1)**
unsymmetrical, uncracked	25...-7 C	SnAgCu	16,200	16.2	
	20...45 C	SnAgCu	22,700	22.7	
	20...60 C	SnAgCu	8,300	8.3	
	25...+7 C	SnAgCu	56,000	56	
	-23...25 C	SnAgCu	7,100	7.1	
	Composed	*SnAgCu*	*20,500*		
unsymmetrical, uncracked	25...-7 C	SnPb	12,700	12.7	19
	20...45 C	SnPb	19,000	19	23
	20...60 C	SnPb	7,200	7.2	7.5
	25...+7 C	SnPb	32,700	32.7	58
	-23...25 C	SnPb	7,200	7.2	8.8
	Composed	*SnPb*	*17,000*		

Figure A11 Estimates of mean cycles to cracking for different use conditions and relative acceleration factor to control test cycle in the range of -40°C to 85°C (Courtesy of Rainer Dudek, et el, Franhofer IZM, Germany and Jabil Circuit, France).

Note: This table gives acceleration factors (AFs) for the given type of ceramic components discussed in the paper. These AFs and others reported in literature are developed for specific package configurations and they should not be used blindly for different types of packages and assemblies.

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