Front-End Architectures for CMOS Radio Receivers

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Abstract

This paper addresses some of the architectural limitations and concerns in the development of CMOS high frequency front-ends for wireless communication applications. Different architectures are evaluated as to how well their characteristics suite an all CMOS integrated solution. Also, the comparison aims at important parameters such as low cost, low power, and small feature size. Important receiver architecture characteristics are summarized and compared. It is argued that digital generation of I/Q signal paths provides for a possible performance improvement. To accomplish the IF digitizing a bandpass Delta-Sigma Converter is suggested as a potential solution.

I INTRODUCTION

WITHIN the last decade or so CMOS (*Complementary Metal Oxide Semiconductor*) has seen a renewed interest in terms of integrated analog circuit design, see e.g. [19, 31, 32, 40]. This is partly due to mixed-signal designs where production cost reduction and circuit minimization is potential. Mixed-signal is a term used to identify chip designs where both analog and digital circuitry are combined on a single chip. Mixed-signal technology has brought with it a new design term – *system-on-a-chip* – that illustrates the degree of circuit minimization expected from CMOS integrated design.

In today's electronic industry, a variety of applications already require mixed-mode circuit designs in order to be competitive in price and performance [20]. These applications range from hard-disk drives [31, 40] to medium frequency communication chips [18] and high frequency radio modules [8, 10, 17, 19, 27, 32, 35]. This development is also foreseen within the mobile radio communication industry [3] where production price is a main competition parameter. In fact, in modern wireless communications systems a given performance at a low cost is almost always prefered to improved performance at a greater cost [6].

The use of CMOS is in most wireless equipment limited to DSP (*Digital Signal Processing*) applications and low frequency analog designs [36]. The potential of CMOS for high frequency applications motivates much of todays research in integrated circuit design. As a result designs presenting high frequency CMOS applications are starting to surface [2, 8, 10, 17, 49].

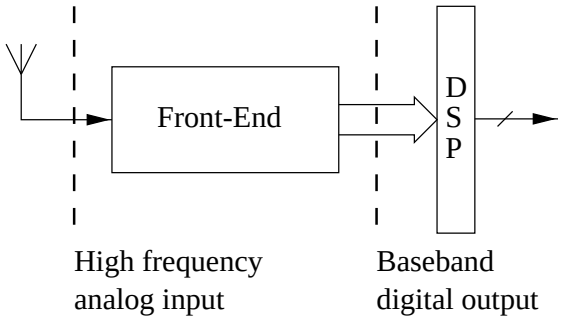

Figure 1: Front-End interface definition. The front-end accepts a high frequency antenna signal and delivers a Nyquist rate digital baseband output to a subsequent DSP unit.

High frequency front-end applications (see Figure 1) such as LNAs (*Low Noise Amplifiers*) and frequency translating devices are typically implemented using one of the more sophisticated and also more expensive technologies such as Bipolar, GaAs (*Gallium-Arsenide*) or BiCMOS (*Bipolar CMOS*) [6, 37]. To reduce cost and to fully exploit the potential of mixed-signal designs more analog signal processing applications thus need to be implemented in CMOS. This basically implies taking CMOS to higher frequencies.

At higher frequencies the analog signal processing capability limitations of CMOS are more apparent [32]. The main problem is the semi-conducting property of the silicon substrate. This constitutes a significant capacitive load resulting in large signal losses in especially transmission lines [33]. This combined with a limited ability to drive the undesired capacitive loads makes high frequency CMOS design a non-trivial task. An equally important effect of the substrate loss is the reduced performance of passive and especially reactive components. High quality inductors, which are extensively used in high frequency analog circuits, are not easily manufactured in any IC technology [28]. In a standard silicon technology, quality factors of passive spiral inductors are limited to approximately 3 – 8 within the frequency range 0.5 – 2GHz which is rather poor [2, 29]. In comparison, off-chip high-Q resonators can provide quality factors better than 10,000 for the same frequency range. One way to circumvent the limited quality factor problem is to use active approaches where the quality factors can be increased significantly. On-chip bandpass filters based on active Q-enhancement have been reported with quality factors as high as 100 – 360 [22, 23, 42]. Passive filters are, however, almost always preferable rather than active ones with respect to dynamic range and IMD (*Inter-Modulation Distortion*) [2, 3]. IMD performance is especially important in the design of early stage filters such as antenna filters. The small signal handling of active filters is limited by a fundamentally higher noise level, and large signals suffer from nonlinearities in the active devices resulting in signal distortion [1]. Also, signal swings above the supply voltage, as used in many tuned amplifiers, are not possible with active inductors [25]. The extensive use of high quality inductors in RF designs does therefore not match with the fact than silicon technologies only provide poor quality inductors. Therefore, new transceiver architectures need to be designed with the

limitations of CMOS in mind [21]. This is mandatory if a single mixed-signal chip transceiver is to be made potential. Also, with the newest trend in mobile communication being dual- or even multi-standard designs a degree of flexibility is required that calls for controllability of system blocks. Besides complying with the limitations of CMOS the receiver design also needs to fulfill the given system specifications.

The purpose of this document is to evaluate different receiver architectures aiming for an all CMOS-RF solution. The architectures to be mentioned are all included in Figure 2.

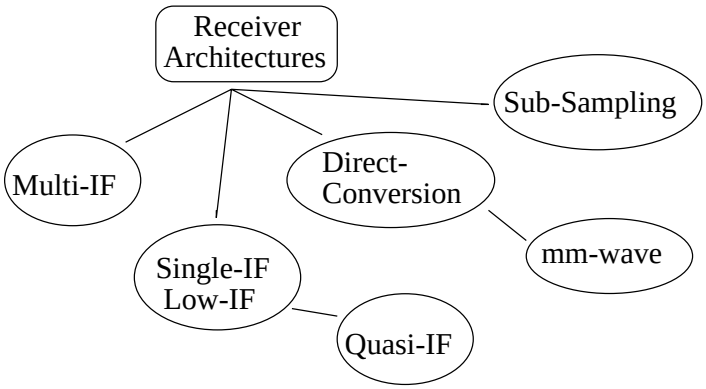

Figure 2: Architecture relation diagram presenting the most common architectures, their relations, and also a few novel architectures.

Sections II, III, and IV address todays receiver architectures, i.e. heterodyne, direct-conversion, and low-IF receiver, respectively. In the latter, an ADC (*Analog-to-Digital Converter*) based on a bandpass delta-sigma analog-to-digital conversion is presented.

Section V present an alternative architecture developed at the UCLA (*University of California, Los Angeles*). This architecture, designed for DECT-like specifications, makes use of sub-sampling in an attempt to provide increased integration and flexibility. The combined use of sub-sampling and delta-sigma conversion is addressed in Section VI. In Section VII the mm-wave receiver is briefly introduced. Section VIII compares the architectures with respect to some key receiver parameters.

II HETERODYNE RECEIVER ARCHITECTURE

THE traditional receiver architecture for wireless communication, the heterodyne receiver, as illustrated in Figure 3 was introduced in 1918 [1]. Here the translation from a high frequency signal to a low frequency baseband signal is spread over two or more conversion stages, thus the label *multi-IF* in Figure 2. The architecture of Figure 3 exploits high quality filters to provide the desired performance. The first filter , the duplex filter, separates the receiver from the transmitter. The second, the image rejection filter, suppresses the image signal while

the third provides for channel selection filtering. Generally, the image rejection and the channel selection filters are implemented using expensive SAW (*Surface Acoustic Wave*) filters. This adds significantly to the end price of the handset.

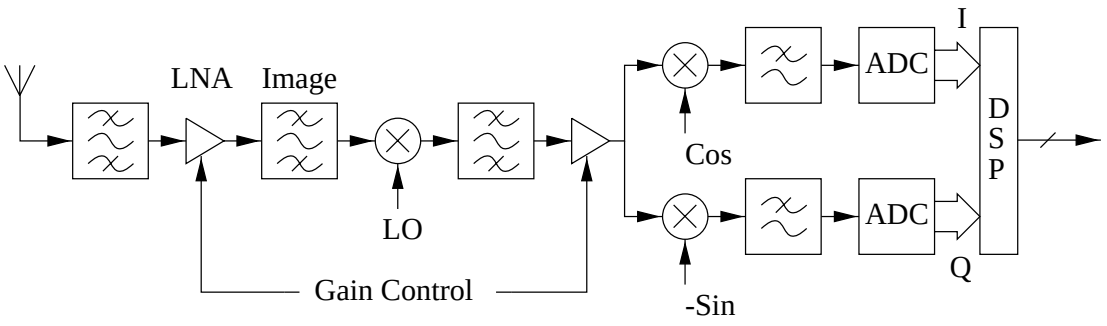

Figure 3: Traditional heterodyne receiver architecture based on the parallel data detector concept.

For reasons of image rejection the first intermediate frequency needs to be kept fairly large, usually on the order of 10% of the RF carrier frequency [15]. This implies that at least one filter stage and one amplifier stage need to be implemented at a high intermediate frequency. Thus, while a large IF reduces the requirements for preceding filtering, high frequency signal processing is required.

The architecture of Figure 3 differs from that indicated in Figure 1 by having dual signal paths delivered to the subsequent DSP. Figure 3 makes use of a parallel data detector concept while the simpler serial data detector is assumed in Figure 1. Both detector concepts are generally applicable for demodulation. The main difference is that the serial detector makes use of real signal representation whereas the parallel detector uses complex signal representation. As a result the serial detector is generally less complicated and a lower power consumption is potential. However, the parallel detector generally provides for better performance in fading environments than does the serial detector [5] and as a result the parallel detector is the most widely used. Also, the use of the parallel data detector concept of Figure 3 generally improves on the image rejection [9, 11]. Ideally, the complex signal representation provided by the parallel detector allows for complete separation of the desired signal and the corresponding image signal. By prober combining of the I and Q signals it is possible to relocate the desired and the image signal to positive and negative frequencies, respectively. This, however, requires exact matching of the I and Q signal branches which is not possible in a practical implementation. One way of illustrating the effect of I/Q mismatch is to consider a complex input signal consisting of unmodulated single tone signals,

$$\begin{aligned} s(t) &= \cos(2\pi f_{IM} t) + j \cdot \alpha \cdot \sin(2\pi f_{IM} t + \theta) \\ &= 1/2 \cdot \left[e^{j2\pi f_{IM} t} \left(1 + \alpha \cdot e^{j\theta} \right) \right] + 1/2 \cdot \left[e^{-j2\pi f_{IM} t} \left(1 - \alpha \cdot e^{j\theta} \right) \right] \end{aligned} \quad (1)$$

As the amplitude, α, and phase, θ, errors are relative values these can be assigned to just one of the signal branches without loss of generality [43]. The terms $e^{j2\pi f_{IM} t}$ and $e^{-j2\pi f_{IM} t}$ can

be viewed as the desired and the image signal, respectively. Hence, from Equation (1) it is seen that in case of ideal matching, i.e. $(\alpha, \theta) = (1, 0)$, the image signal component is cancelled. By comparison of the amplitude terms of the desired and the image signal components he approximate amount of I/Q image discrimination, ID, is found as [43]

$$\begin{aligned} ID &= 10 \cdot \log\left(\frac{A_d}{A_i}\right)^2 = 10 \cdot \log\left(\frac{1+\alpha \cdot e^{j\theta}}{1-\alpha \cdot e^{j\theta}}\right)^2 \\ &= 10 \cdot \log\left(\frac{1+\alpha^2+2\alpha\cos(\theta)}{1+\alpha^2-2\alpha\cos(\theta)}\right), \end{aligned} \tag{2}$$

where A_d and A_i are the amplitudes of the desired and the image signal, respectively. Thus, to achieve for instance 40 dB of I/Q discrimination Equation (2) reveals that the local oscillators are required to be orthogonal within 0.5° under all circumstances including temperature drift and processing tolerances [41]. Also, to preserve the I/Q discrimination the amplitude response of the two signal paths must be matched to better than 0.1 dB including any gain mismatch in the ADCs [41]. Obtaining such an accuracy is not easily done in any IC implementation [39]. Thus, due to phase and amplitude mismatch between the signal paths the IF still needs to be fairly large if image rejection is to be preserved without the use of expensive ceramic filters [15]. Also, the dynamic range of a down-converter is limited by the I/Q imbalance [3]. As a result of these matching limitations digital generation of the I and Q signal branches could offer improved performance for some applications.

Designing high performance low noise amplifiers [22] and mixers [10] in pure CMOS is a great challenge at higher frequencies. Amplification and filtering at tens to hundreds of MHz come at the expense of increased power dissipation. For the active devices to drive the large parasitic capacitances they need to operate at high bias currents [1]. As a result, high frequency amplifiers are not as power efficient as equivalent amplifiers designed for lower frequencies [3]. Besides, a vast number of circuit components are required making the design rather area consuming and thus also costly. This makes the receiver unsuited for an immediate CMOS IC implementation.

The high degree of filtering in the heterodyne receiver allows for a final down-conversion to a low IF frequency. This way the low-IF signal may be converted to the digital domain whereby the problem of DC-offset, as described in the following section, may be avoided.

III DIRECT-CONVERSION RECEIVER ARCHITECTURE

The direct-conversion receiver architecture represents a less complicated design by having a reduced number of circuit blocks as shown in Figure 4.

A fundamental advantage of the direct-converter is that most amplification and filtering is performed at baseband rather than at RF. This implies lower current drain in amplifiers and active filters and also a simpler task of image-rejection [1] as the image ideally is non-existing. Besides eliminating the need for high frequency bandpass IF filters and amplification, direct-conversion receivers also provide a wide tuning range and high selectivity [12]. There are, however, several

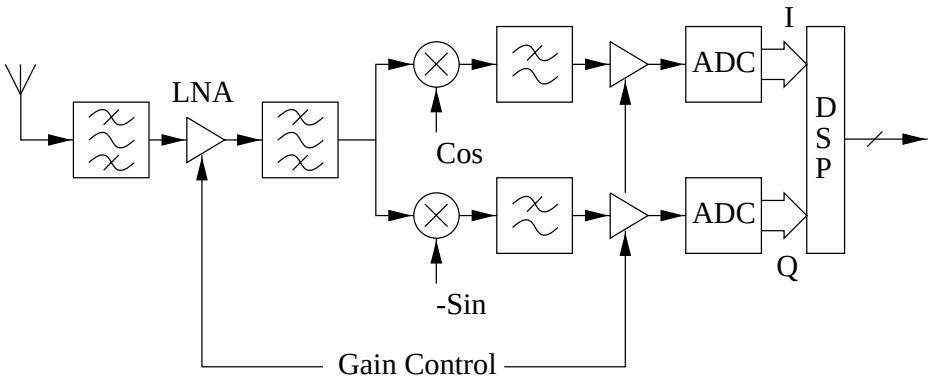

Figure 4: Direct-conversion receiver architecture.

drawbacks such as two high frequency conversion stages in parallel, LO frequency deviation, spurious LO leakage, and DC offset connected to direct-conversion.

In direct-conversion of signals containing low frequency and DC information, such as GMSK (*Gaussian Minimum-Shift Keying*), a device capable of delivering I/Q-branch baseband outputs is mandatory [1]. This parallel mixer structure is required to operate at RF frequencies and the power consumption of the combined converter is thus significantly increased. In fact, this receiver operation can increase the overall power consumption to a level comparable with the heterodyne architectures [4].

In a direct-conversion receiver for GMSK signals DC information needs to be carried from the mixers trough all subsequent receiver stages. Hence, DC coupling is generally considered to be mandatory. However, any DC offset adds directly to the information signal resulting in distortion [1]. This problem could be reduced by allowing DC-blocking capacitors to be used. Even though GMSK is characterized by a spectral peak at DC some of the low frequency energy may be removed without significant performance degradation. With maximum cut-off frequencies around 50 Hz unpractical capacitor sizes are called for. This makes DC-blocking unsuited for IC implementations. As a result direct-conversion receivers for GSM cellular radio needs offset canceling algorithms to cope with the DC-offset problem.

Generally three main sources to DC offset are considered [3]. These can be separated as follows:

- Static offset
  - **Transistor mismatch in the receiving path**
    Due to substrate and supply noise considerations signal paths are typically implemented fully differential. Any matching errors in these signal paths generate DC-offset which results in a decreasing SNR. The main contributers are here transistor and resistor mismatch.

- Dynamic offset
  - **Spurious LO leakage to antenna**
    Due to poor isolation through the mixer and LNA the LO signal may leak to the antenna. Impedance mismatch at the antenna can cause the leaked signal to be reflected whereby it self-converts in the mixer. This LO-self mixing also adds to any DC-offset in the signal [3].
  - **Large near channel interferer leaking into the receiver LO port**
    This causes the LO signal to display spectral distortion which also adds DC to the signal.

Furthermore, any low frequency noise originating from the receiver itself adds to the down converted signal resulting in further decrease in SNR [15]. Typical noise characteristics of Bipolar [16] and MOSFET devices, as sketched in Figure 5, illustrate that active devices contribute mostly with low frequency $1/f$ noise. MOSFET mixers add a considerable amount of low frequency noise to its down-converted signal whereby the overall receiver noise figure is degraded [1].

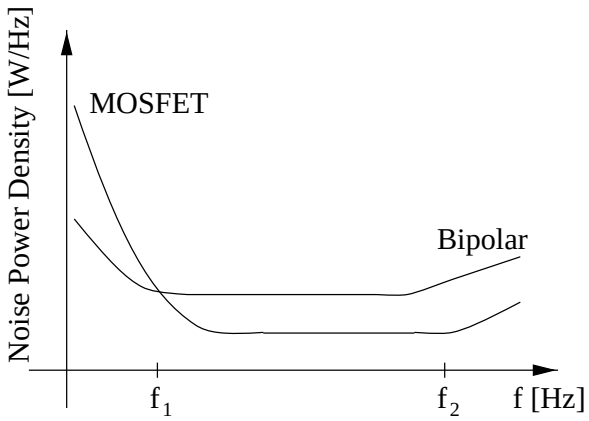

Figure 5: Sketch of Noise Power Spectral Density characteristics of MOSFET and BJT's. The frequencies f_1 and f_2 are typical of the order kHz and several hundreds MHz, respectively [16].

DC-offset represents a major limitation in direct-conversion receiver design. In fact, DC-offset is the single most important reason why only a very limited number of commercial available GSM handsets are based on direct-conversion [47].

The problem concerning DC-offset can be avoided by using a modulation form without any significant information energy at DC – such as binary FSK. On the other hand, an advantage of using GMSK is that a more power efficient non-linear power amplifier may be applied at the transmitter [2], [45, p.178].

Any frequency error between the transmitter and receiver LO causes the signal to down-convert asymmetrically around DC. This is also a concern in heterodyne receivers if the final conversion is to baseband and not a low-IF. Spurious leakage from the receiver LO to the antenna becomes an in-band interferer to other nearby receivers operating at the same frequency [3]. Also, in direct-conversion a mixer with a highly linear RF-to-IF transfer function is required [1] in order to suppress undesired IMD products resulting from interferers [3].

The reduced circuit complexity of direct-conversion receiver architectures generally comes at the expense of reduced performance. Thus for a given application a trade-off exists between complexity and performance.

IV LOW-IF RECEIVER ARCHITECTURE

ONE important operation, the actual demodulation of the information bits, is in most modern receivers implemented digitally whereby some flexibility is provided. This way different modulation forms, in theory, can be accommodated by changing the software performing the actual task. Having the channel filtering done digitally provides superior performance and a degree of flexibility otherwise not provided by an analog implementation [41]. To accomplish this either an extremely high-speed ADC is required or the information signal needs to be down-converted to a low-IF frequency. For reasons of power consumption the low-IF approach, as illustrated in Figure 6, appears to be the most promising.

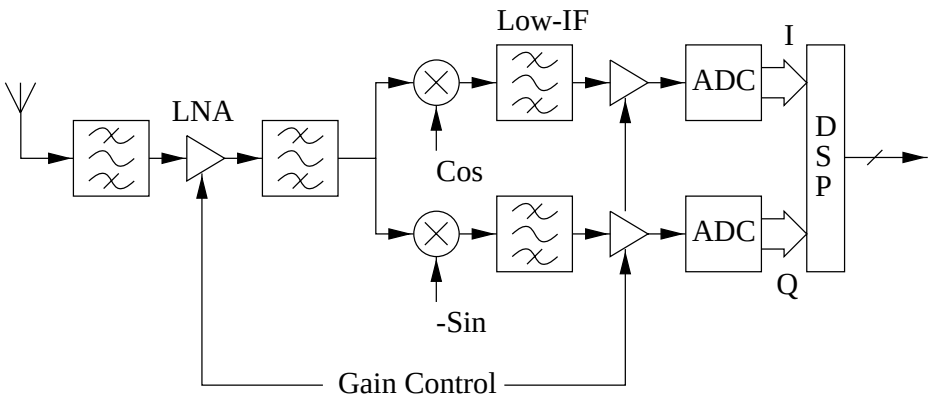

Figure 6: Low-IF receiver architecture.

The architecture presented in Figure 6 also makes use of I/Q-demodulation. A number of commercial available low-IF chip-sets – many aiming at DECT (*Digital European Cordless Telephony*) – make use of single-ended demodulation based on a highly selective IF SAW filter, a limiting amplifier, and a RSSI (*Received Signal Strength Indication*) demodulator. This makes for a simpler demodulator implementation whereby integration is eased. However, the I/Q-demodulation provides for 20 – 40 dB's of image rejection [9] whereby a less selective filter

may be used for image rejection. The use of a image rejection mixer may improve even further on the inherent architectural degree of image rejection [11].

By combining a non-tunable I/Q down-conversion mixer and a tunable image rejection mixer for down-conversion to baseband and channel selection an architecture known as a Quasi-IF receiver results. The Quasi-IF receiver, illustrated in Figure 7, is a compromise between the traditional heterodyne receiver and the direct-conversion receiver.

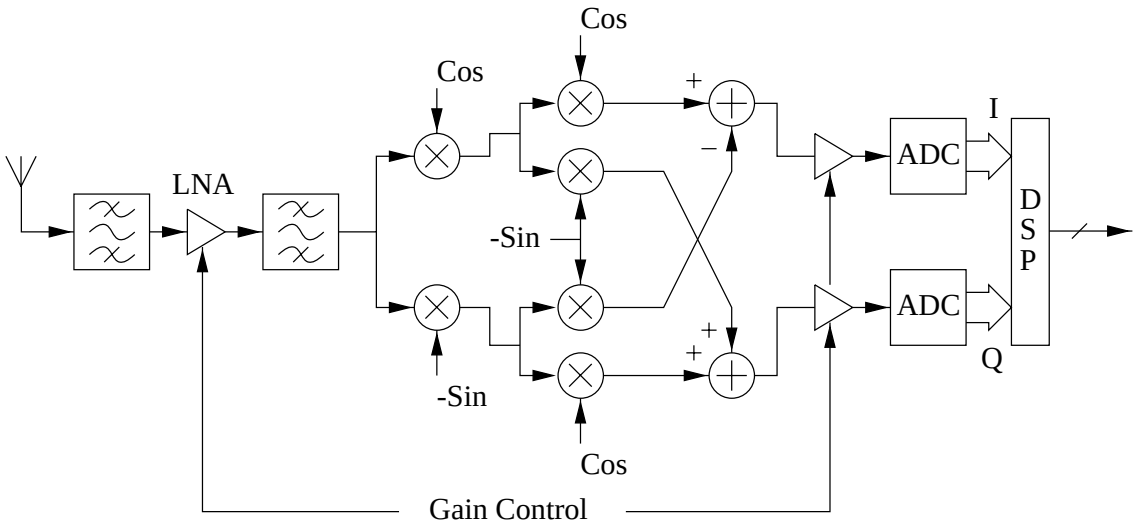

Figure 7: Quasi-IF receiver architecture.

The information signal is here down-converted – in quadrature – to a complex low-IF representation. Without any IF filtering the signal is further down-converted whereby a quadrature baseband signal results. Using this approach 40 – 50 dB image rejection is possible without any filtering at IF [9]. Besides using no IF filtering the quasi-IF receiver has several advantages [9, 15]:

- By allowing the first LO to be fixed this may be optimized with respect to phase noise as no switching requirements are now present
- The tunable second LO operates at low frequencies whereby phase noise and undesired non-linearities may be minimized

While the absence of the IF-filter is a clear advantage the extra mixers required add to the complexity of the receiver and as a result also increases the power consumption of the receiver as a whole. This puts extra focus on low-power mixer implementations.

Another circuit block that has significant importance, especially in a low-IF reduced filtering application, is the ADC. The resolution of the applied ADCs have impact on the preceding

analog circuitry, especially the AGC, as the most significant effect of an ADC is on the dynamic range of the receiver [43]. The dynamic range of analog-to-digital converters is for sinusoidal inputs defined as the ratio of the full scale signal power to the signal power of a small sinusoidal input signal resulting in a SNR of 0 dB [39]. Increasing the resolution of the ADC increases its dynamic range accordingly

$$DR \approx 6.02 \cdot N + 1.76 \quad [\text{dB}], \tag{3}$$

where N is the ADC resolution in bits [7]. Thus, provided sufficient resolution the AGC design requirements can be relaxed inviting to IC implementation. A resolution of 9 – 14 bits, corresponding to a dynamic range of approximately 56 – 76dB, is considered sufficient for implementing cellular systems such as IS-54 and GSM [38]. The specific number of bits required vary depending on the overhead desired. The number of bits, however, cannot be increased at will. Not only is multi-bit accuracy a difficult design problem it is also rather power consuming. In high accuracy converters some means of start-up calibration may be required. This must be kept in mind when wireless applications are the goal. Wireless applications often call for power-down of circuits to save power. Power-down of a high resolution ADC followed by a power-up requires re-calibration making the power-up process sluggish [30]. One way to overcome this is to calibrate only once during operation and then store the calibrated values.

The performance measure of an analog-to-digital converter is typically the product of the bandwidth, i.e. half the sample rate and the resolution [41]. With regards to this measure, early analog-to-digital converters provided poor performance. The conversion speed was the limiting factor. This has changed over the last decade and it is now possible to process at much higher speeds [41]. Sampling frequencies around 40MHz is well within the capability of current IC technology when using a 0.8μm process [24]. In fact, 8 bits of resolution has been demonstrated in a 0.5μm digital CMOS technology using a sample frequency of 80 MHz [44].

This improvement in ADC performance may be utilized to either sample larger signal bands or to reduce noise by oversampling. Oversampling the incoming signal by orders of magnitudes reduces the noise level whereby the resolution can be improved further without the need for increased quantizer accuracy. Oversampled converters are thus extremely feasible in IC implementations where quantizer accuracy is limited. Yet another means of improving on the converter performance is to utilize noise shaping. Noise shaping converters relocate the quantizer noise to frequency bands which are not of interest. The delta-sigma converter is such an oversampled noise shaping converter [7].

As mentioned previously frequency translating a signal to baseband might deteriorate the SNR due to for instance $1/f$ noise. Hence, it may be advantageous to apply analog-to-digital conversion while the signal still is located at some IF frequency [41]. The signals of interest in cellular applications are normally narrow-band and band-limited. Analog-to-digital conversion of IF bandpass signals, using traditional converters, imply wasteful conversion of frequency bands containing only noise and interfering signals. Figure 8 illustrates a receiver architecture where bandpass delta-sigma conversion is utilized. Using this approach the resolution of the converter is concentrated around a certain IF frequency. The incoming high frequency signal is in Figure 8 down-converted to an intermediate frequency using a traditional continuous-time frequency

converter. The information signal is then digitized using a quadrature bandpass delta-sigma converter whereupon the signals are digitally down-converted to baseband. Finally, the signal is decimated and the actual channel select filtering is performed.

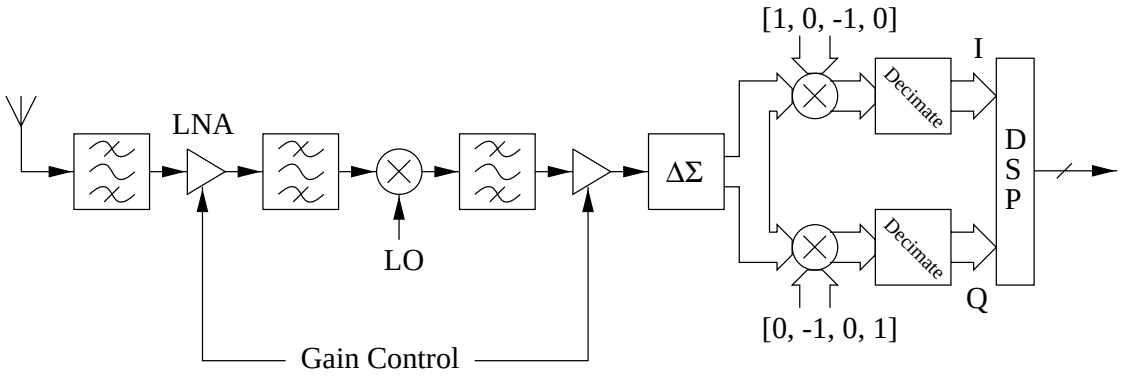

Figure 8: Low-IF receiver architecture based on bandpass delta-sigma conversion.

The output of a delta-sigma converter is a highly oversampled signal contaminated with a high degree of high frequency noise. In order to subsequently reduce the sample-rate to approximately the Nyquist rate, while preserving the resolution, the signal needs filtering and subsequent down sampling.

The use of delta-sigma converters makes it possible to design a very compact transceiver front-end with a reduced number of analog parts. Both the direct-conversion and the heterodyne architectures use analog circuitry to down convert the incoming RF signal to I and Q channel baseband components. Obtaining good matching in analog circuits is not an easy task. One solution to this I/Q signal path matching problem is to perform the A/D conversion at IF instead of baseband. This way the I/Q matching is an all digital task and obtaining sufficient matching accuracy in two digital signal paths is easily accomplished [41]. One means to digitally generate I/Q signals is to use the Hilbert transform [43]. Moreover, pushing the analog-digital interface closer to the antenna provides for increased flexibility. This provides some motivation for IF conversion as illustrated in Figure 8.

Other advantages are inherent to IF conversion. For instance DC-offsets at the converter inputs no longer impose a problem and the same goes for low frequency noise generated from preceding circuit blocks [41]. The use of IF conversion is, however, no trivial task. Removing some of the preceding filter stages requires increased dynamic range and this at a much higher frequency. Also, the problem of IMD becomes more severe as the filtering is relaxed. The increased sample rate results in increased power consumption in the subsequent decimation filters. A trade-off thus remains to be decided for any give application. The designs presented in [12, 13, 34, 38] represent state-of-the-art bandpass delta-sigma converter designs with performance as listed in Table 1. With conversion performances as stated in Table 1 delta-sigma converter based receivers appear promising in implementing low cost digital receiver. They

Bandwidth@f_c	**Resolution**	**Sampling rate**	**Max. SNR**	**Dynamic range**	**Ref.**
n/a@50MHz	n/a	200MHz	n/a	n/a	[12]
200kHz@2.5MHz	n/a	10MHz	52dB	58dB	[13]
>80kHz@2.5MHz	16 bit	10MHz	94dB	94dB	[34]
200kHz@10.7MHz	n/a	42.8MHz	57dB	n/a	[38]

Table 1: State-of-the-art bandpass delta-sigma converter performance.

offer a means to reduce the amount of analog circuit whereby an integrated solution is eased.

V SUB-SAMPLING RECEIVER ARCHITECTURE

AS mentioned above, direct-conversion provides for receiver implementations well suited for IC implementation. However, a number of disadvantages are as mentioned inherent to direct-conversion. A mixer with a highly linear RF-to-IF transfer function is required [1] to suppress unwanted IMD products resulting from interferes [3] and low frequency noise from the continuous-time mixer adds to the signal and degrades the receiver noise figure. A solution to a number of these direct-converter problems may be sub-sampling [1]. Traditional architectures solely operate the MOSFETs as active analog devices despite the fact that they are excellent switches [1]. At UCLA a considerably effort is devoted to the development of a sub-sampling transceiver architecture [3]. The actual sub-sampling device, as illustrated in Figure 9, tracks the input carrier and takes samples at a much lower rate.

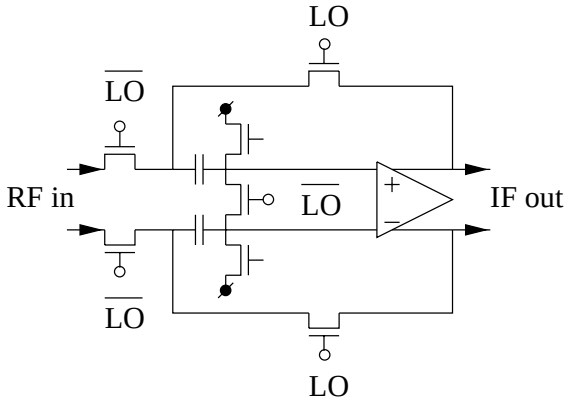

Figure 9: UCLA sub-sampling track-and-hold mixer implementation [3].

The operation of a track-and-hold circuit as that of Figure 9 is ideally that of a low-pass filter followed by an ideal sampling device [46]. The cut-off frequency of this low-pass filter, also know as the track-mode bandwidth of the sampler, effects the performance of the circuit significantly. The track-mode bandwidth thus needs to be greater than the highest input frequency

component while the sample-rate needs to be larger than at least twice the information signal bandwidth [1]. If the track-mode bandwidth is large enough to accommodate the changes in the input signal exact sample values are, in theory, obtained. As the track-mode bandwidth is reduced the filtering effect of the sub-sampling mixer ceases to provide exact sample values as the signal spectrum is shaped and thus signal distortion results.

Besides speed limitations other concerns need to be considered. For instance, to ensure that no spectrum overlap occurs when the sample rates are between the minimum two times the signal bandwidth $(f_h - f_l)$ and two times the highest frequency component f_h of the bandpass signal the sampling frequency f_s must satisfy [48]

$$\frac{2f_h}{k} \leq f_s \leq \frac{2f_l}{k-1} \quad \text{,with} \begin{cases} 2 \leq k \leq \dfrac{f_h}{f_h - f_l} \\ \\ f_h - f_l \leq f_l \end{cases} \tag{4}$$

where k is an integer value. Presumed that the sample-rate further more is an exact sub-harmonic the circuit of Figure 9 results in a direct down-conversion [1]. As with the continuous-time direct down-conversion the sub-sampling direct down-conversion is influenced by the inherent $1/f$ noise of active devices. Provided a high gain LNA precedes, a sub-sampling mixer tends to be more linear, in terms of RF-to-IF magnitude transfer, than traditional analog multipliers and its dynamic range is also large [3]. The discrete-time IF output readily provides an interface to subsequent wide dynamic range switched-capacitor or switched-current CMOS channel select filters operating at a low clock rate.

The sub-sampling approach is bandwidth limited as only narrow band signals may feasibly be down-converted using this approach [10]. This results in the need for high-quality RF filtering which is not easily implemented in an integrated way. Another more severe disadvantage connected to sub-sampling is noise [1]. The problem is that the sub-sampling mixer also acquires wide-band noise which then folds into the frequency band of the down converted signal [25]. The noise in question results both from the input signal and from the preceding receiver stages. The baseband noise spectral density is raised by the ratio of the track bandwidth to the sample-rate [3]. The UCLA sub-sampling receiver structure acquires samples of a 900MHz carrier at a 50MHz rate while displaying an 18dB noise figure [3].

VI SUB-SAMPLING DSC RECEIVER ARCHITECTURE

As a final sub-sampling scheme sub-sampled delta-sigma conversion is addressed. The delta-sigma converter is here operated at a sample frequency f_s much larger than the signal bandwidth but smaller than the signal carrier. This way down conversion is obtained as well as noise shaped analog-to-digital conversion. One concern to this combined approach is that the circuit blocks have to be able to operate at the highest frequency component in the signal [48] if distortion is to be minimized. Also, the combined approach results in a reduced dynamic range of the converter [14]. To circumvent this a mixer stage is included in the delta-sigma converter feedback loop as illustrated in Figure 10.

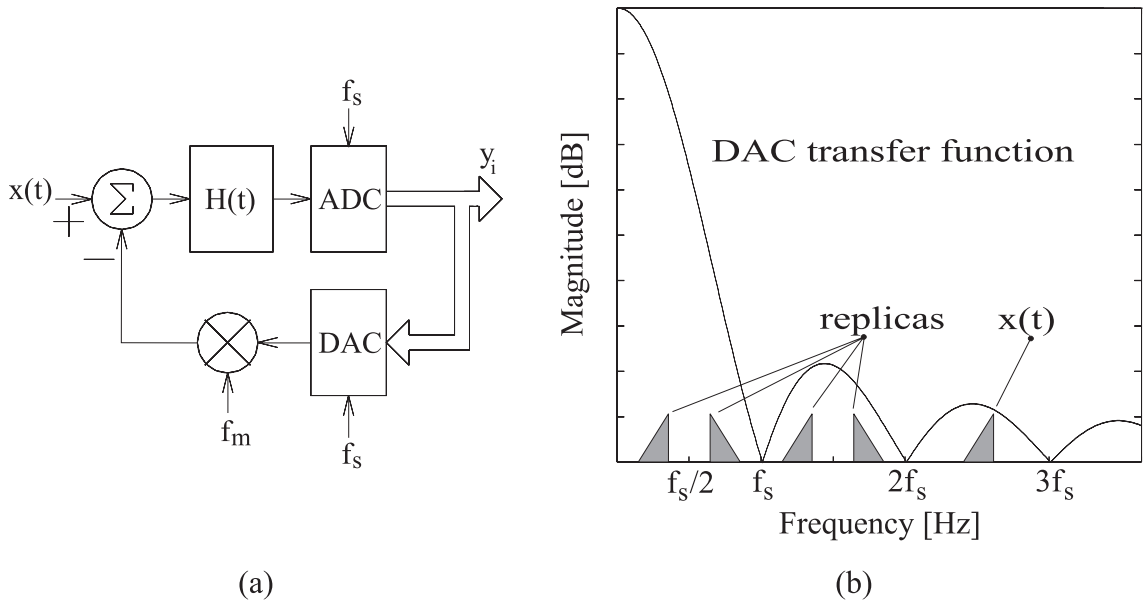

Figure 10: Sub-Sampling bandpass delta-sigma converter [14]. (a) Structure of the circuit. (b) Frequency domain signal representation.

By proper choice of the f_m frequency the zero-order hold effect of the DAC is minimized and the dynamic range is restored. Thus, f_m is chosen such that the $x(t)$ sub-sampling replica falling within $[-f_s/2; f_s/2]$ is translated back to the original $x(t)$ frequency. However, this implies adding a non-linear stage in the feedback loop. Any errors and distortion resulting from these blocks are not suppressed by the delta-sigma operation. Simulations have shown that the structure of Figure 10 is capable of providing approximately 13 bits of resolution at an input frequency of 10.7MHz [14]. However, due to the above this may be rather optimistic with the practical limitations of CMOS.

VII MILLIMETER-WAVE RECEIVER ARCHITECTURE

Traditional receivers, such as the heterodyne and direct-conversion receivers, make use of some sort of quadrature hybrid network to generate the required I/Q signals. Obtaining good accuracy in the complex signal path is difficult in integrated circuit technology, even at moderate frequencies. As the frequency is increased the wave lengths of the signals in question decrease accordingly. It therefore becomes more difficult to obtain acceptable phase and amplitude accuracy.

The mm-wave receiver is a digital receiver operating directly at millimeter-wave frequencies, i.e. approximately at 30 GHz and higher. Through the use of six-port technology a very simple and robust receiver is possible [26]. The architecture of the mm-wave receiver is illustrated in Figure 11.

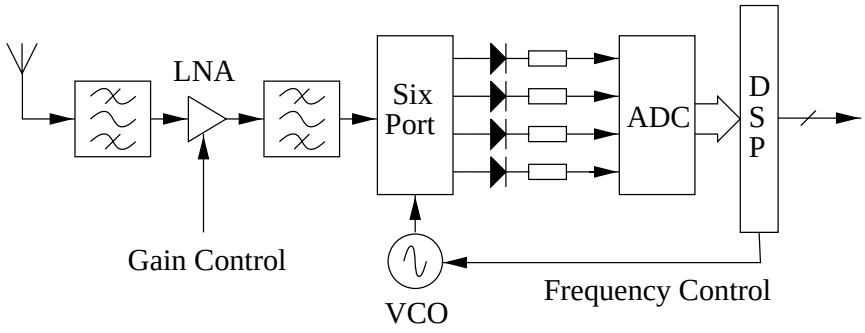

Figure 11: Millimeter-wave receiver architecture [26].

This architecture presents an interesting and novel approach to high frequency receiver design. The above receiver is developed for an operation frequency of 26.5 GHz [26]. Its usability and performance at lower frequencies – todays commercial radio systems all operate below 5 GHz – still needs to be evaluated.

VIII COMPARISON

In order to evaluate the different receiver architectures a few of the key receiver parameters are considered. The performance of the architectures are listed in Table 2.

Parameter	**Heterodyne**	**Direct-Conversion**	**Sub-Sampler**	**Low-IF**
Selectivity	High	High	High	High
Analog Requirements	High	Moderate	Moderate	Low
Flexibility	Low	Low	High	High
CMOS Compatibility	Low	Moderate	Moderate	High
Noise	Low	Moderate	High	Low
Dynamic Range	High	High	High	High

Table 2: Comparison of various receiver architecture key parameters.

The ratings of Table 2 may not be obvious. For instance, even though sub-sampling exploits the excellent switching property of CMOS this architecture is still rated moderate with respect to CMOS Compatibility. This is due to the requirement for a high-Q antenna filter. From a CMOS point of view high dynamic range sampled-data circuits are better suited and thus the Delta-Sigma converter based architectures are preferable. The above, however, does not take power consumption into account. As power consumption is extremely important in battery operated hand-portable wireless applications it is deplorable that this parameter is often left out in the publications.

IX CONCLUSION

THE heterodyne receiver architecture has been around since 1918 and a majority of engineers has gotten familiar with this concept. Some reluctance towards new architectures, until these prove themselves worthy, must be expected. However, direct-conversion receivers offer significant power savings by reducing the number of circuit blocks and by amplifying at baseband rather than at some IF frequency of tens or even hundreds of MHz. This is extremely important in wireless communication applications where power consumption is a key parameter. Also, the use of moderate IF frequencies in heterodyne receivers impose almost equivalent noise requirements on the first LO as does the direct-converter. Still, a number of drawbacks is faced by the direct-converter. Since the overall direct-converter performance depends significantly on the rejection achievable in the image-rejection mixer, I/Q-path matching is extremely important. Accurate I/Q-matching is hard to obtain in the analog domain whereas matching in a pair of digital paths is easier. This provides motivation for IF analog-to-digital conversion as possible using bandpass delta-sigma conversion. With the delta-sigma converters inherent robustness towards component tolerances these types of receiver architectures appear promising for integrated solutions. Thus, further research in the area of delta-sigma converter based receiver architectures is considered justified.

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