The Recabling Scheme and the New Algorithms for the EMC Trigger

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The current EMC trigger operates on fixed jet patches. This results in large gaps in the coverage of the detector, both in eta and phi. Carl Gagliardi has proposed modifications to both the internal DSM tree cabling scheme, and the algorithms. His new scheme will nearly eliminate the gaps in the eta coverage, and reduce the gaps in the phi coverage. The increased acceptance will result in a more uniform (x_1-x_2) coverage and a more rapid efficiency rise, as a function of p_T, above threshold.

Eta-Phi Coverage: Problem and Solution

In the current scheme each BEMC layer 0 DSM board receives a 6-bit ADC value from each of 10 trigger patches. Each trigger patch covers a region of eta-phi space measuring (0.2x0.2). The assignment of trigger patches to layer 0 DSM boards is done so that each layer 0 DSM board covers a region measuring (1x0.4). Calculating the energy in a (1x1) jet patch requires summing up the ADC values from the 25 trigger patches within the jet patch. This involves combining data from several layer 0 DSM boards.

For the first few runs it was necessary to have both full resolution and full range for all sums. The sum of ten 6-bit numbers is a 10-bit number. If the data is split into two groups of five trigger patches then the result is two 9-bit numbers. The DSM output cables can carry 16 bits to the next layer so it is only possible to have one full-range-full-resolution sum on each cable. In order to pass two such sums to the next layer it is necessary to have two output cables. The current cabling scheme was set up so that four out of every five layer 0 DSM boards had one output cable, and the fifth layer 0 DSM board had two output cables. This made it possible to calculate the energy in 12 fixed 1x1 jet patches.

In this scheme, each set of 5 layer 0 DSM boards covered an eta-phi region measuring (1x2) and all 6 output cables went to one layer 1 DSM board. The 4 single-output DSM boards summed up all 10 trigger patch ADC values and sent one 10-bit result to the layer 1 board. The 5^{th} layer 0 DSM board, which covered the middle of the phi region, split its trigger patches into two groups of five and sent two 9-bit sums to the layer 1 board. The layer 1 DSM board was then able to reconstruct two fixed (1x1) jet patches by summing together two (1x0.4) patches with one (1x0.2) patch.

This is illustrated in Figure 1, which shows a (2x2) region of eta-phi space. The thin solid lines indicate which areas are connected to each layer 0 DSM board. There are 10 layer 0 DSM boards in this diagram; 5 at negative eta and 5 at positive eta. The thick solid lines indicate which areas are then connected to each layer 1 DSM board. The dashed lines show how the double-output layer 0 DSM boards split their trigger patches into two groups.

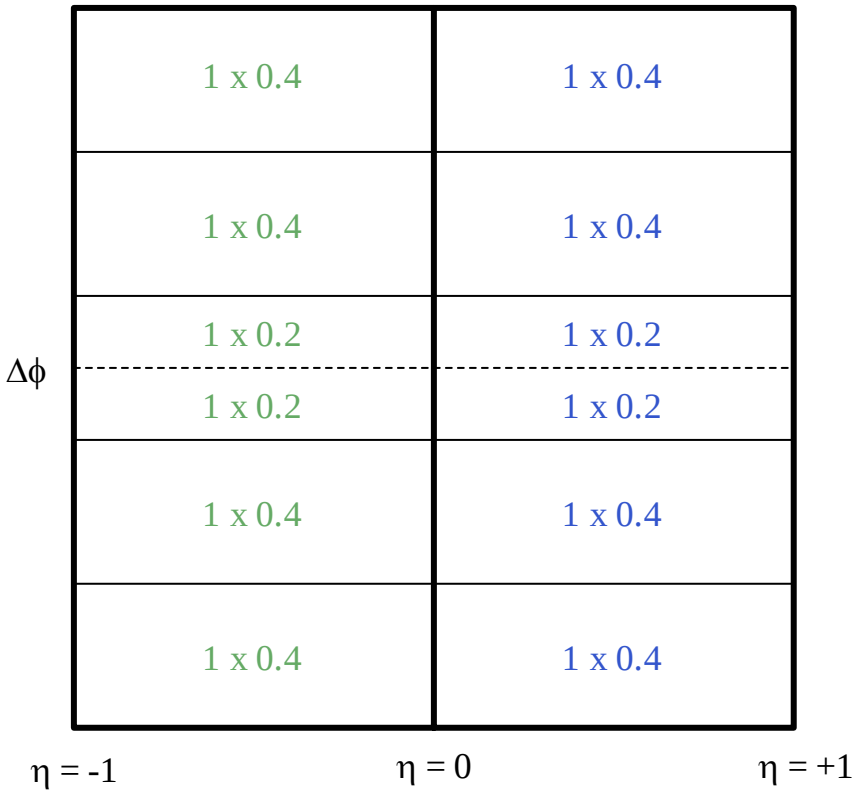

Figure 1: The current BEMC DSM Eta-Phi Scheme

One unfortunate consequence of this scheme is that there are big gaps in the acceptance around the edge of each of these fixed jet patches. Carl Gagliardi pointed out that the experience of the last few years has shown that it is not necessary to pass full-range, full-resolution sums from layer 0 to layer 1. We can select just the lower 6 bits from each sum, with overflow logic to indicate when any higher order bits are set. This makes it possible for even a single-output layer 0 DSM board to pass the sums from two groups of trigger patches to layer 1. As a result, it is possible to calculate the energy for overlapping (1x1) jet patches.

There are two possible ways for each layer 0 DSM to split up its trigger patches:

a) The patches could be split in phi, making two (1x0.2) regions, just like the double-output layer 0 DSM does in the existing scheme. The layer 0 to layer 1 connections would remain as they are now. Every layer 1 DSM would then receive ten sums, each covering an area measuring (1x0.2). That DSM could combine those sums to make six overlapping (1x1) jet patches. This would eliminate the gap in the phi coverage in the middle of this (1x2) region of eta-phi space. However, the gap in eta coverage would remain, and there would still be gaps in the phi coverage in between the regions covered by each layer 1 DSM board.

b) The patches could be split in eta, making a (0.6x0.4) region and a (0.4x0.4) region. The layer 0 to layer 1 connections would be rearranged so that positive and negative eta regions, at a given phi value, would go to the same layer 1 DSM board. Every layer 1 DSM board would then receive 12 input sums covering an area measuring (2x1) in total. It could combine these sums to make three overlapping (1x1) jet patches. It would also make a partial jet patch that would be completed at layer 2 using data from the EEMC DSM tree. This would eliminate the gaps in eta, while leaving the existing gaps in phi unchanged.

Since it is more important for the physics analysis to close the acceptance holes in eta than in phi, option b) has been selected. The layer 0 to layer 1 connections will be rearranged and the algorithms will be changed accordingly. The new scheme is shown in Figure 2. As before, the thin solid lines indicate which areas are connected to each layer 0 DSM board. The thick lines, both solid and dashed, show which areas are connected to each layer 1 DSM board. The dashed lines, both thick and thin, show how every layer 0 DSM board will split its trigger patches into two groups. It can be seen that the double-output layer 0 DSM boards will actually split their trigger patches into 4 groups, and the two output cables will now go to different layer 1 DSM boards.

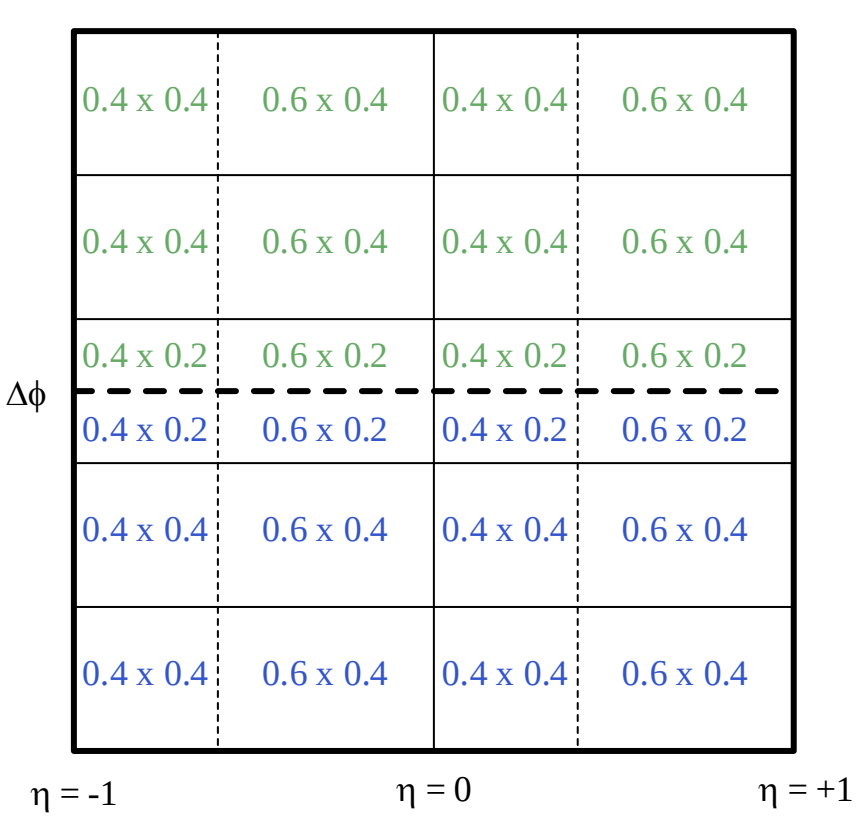

Figure 2: The new BEMC DSM Eta-Phi Scheme

BEMC Re-Cabling Detail

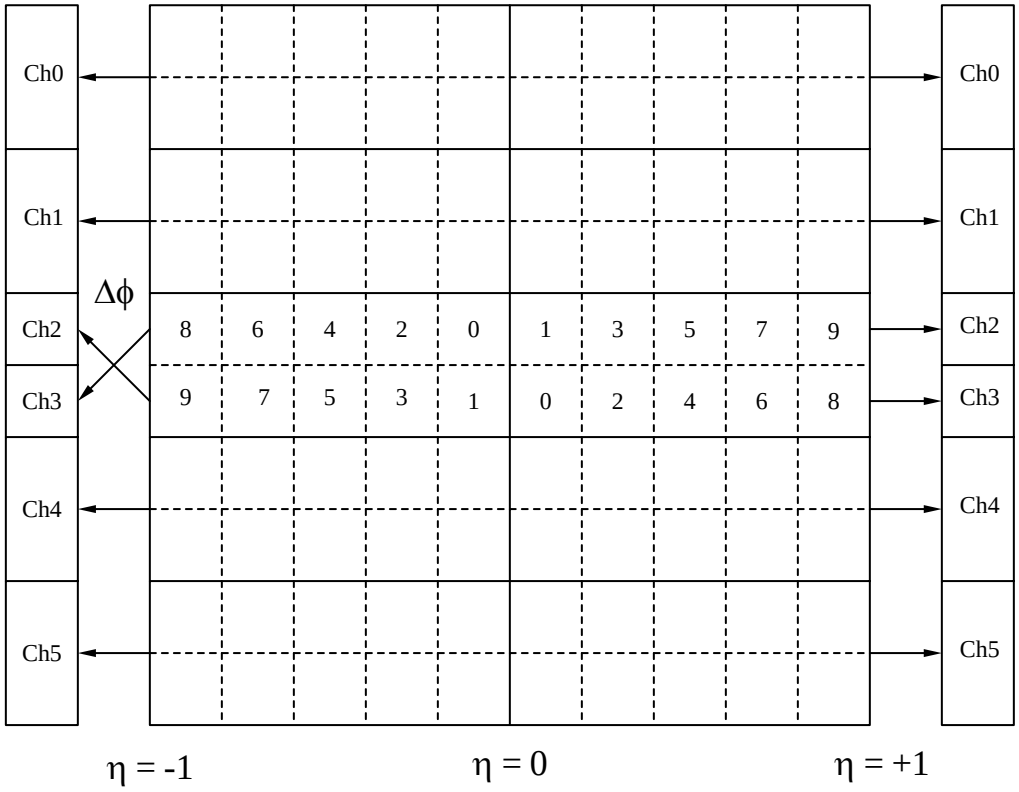

Figure 3: Current BEMC Cabling Scheme

Figure 3 shows more detail of the current cabling scheme. The middle section of the diagram shows the same (2x2) region of eta-phi space that is shown in Figures 1 and 2. As before, the thin solid lines indicate which areas are connected to each layer 0 DSM board. The dashed lines now outline the individual trigger patches. In the central phi region, the numbers show how the trigger patches are connected to the ten input channels of the layer 0 DSM boards. It can be seen that on both the East (negative eta) and West (positive eta) sides of the detector, the small eta trigger patches connect to the low channel numbers, and the large eta trigger patches connect to the high channel numbers. However, the phi-ordering of the channels is switched between East and West. This is irrelevant for the single-output layer 0 DSM boards, because they just sum up all 10 input channels and send one result to layer 1. However, this switch does matter for the double-output layer 0 DSM boards.

The two sidebars show layer 1 DSM boards, and the arrows indicate which layer 0 DSM board connects to each channel of the layer 1 DSM boards. It can be seen that there is a switch on the East side. This is because the double-output layer 0 DSM boards on the East side use the same algorithm as the West side. In this algorithm, the sum of the odd-numbered channels is always driven on the first output channel (JP1) which always connects to input channel 2 of the layer 1 DSM board. The sum of the even-numbered

channels is therefore always driven to channel 3 of the layer 1 DSM board. It can be seen that, in order to correctly reconstruct the (1x1) jet patches, the West-side layer 1 DSM board adds together data received on channels 0, 1 and 2 for one patch, and channels 3, 4 and 5 for the other patch. On the East side, the layer 1 DSM board adds together data from channels 0, 1 and 3 for one patch, and then channels 2, 4 and 5 for the other patch.

The result of all this is that in the current scheme the East and West sides of the BEMC share the single-output and double-output layer 0 algorithms, but they have different layer 1 algorithms. In the new scheme it will be necessary to have different algorithms for the East and West sides at layer 0 anyway, so all mapping issues will be dealt with there. This should make it possible to have one, common, layer 1 algorithm used by all the BEMC layer 1 DSM boards.

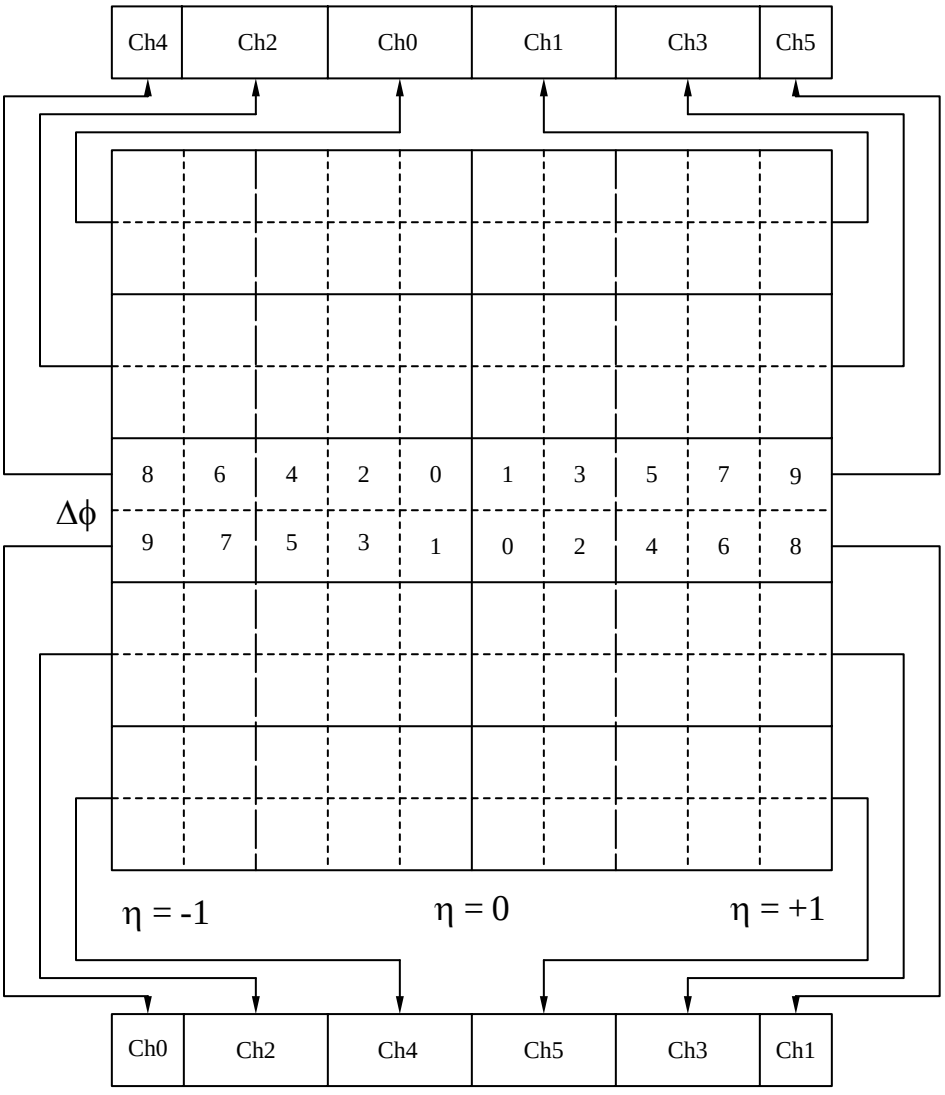

Figure 4: New BEMC Cabling Scheme

Figure 4 shows the detail of the new cabling scheme. As in Figure 3, the middle section of the diagram shows the usual (2x2) region of eta-phi space. The thin solid lines indicate which areas are connected to each layer 0 DSM board and the dashed lines outline the individual trigger patches. The long-dashed lines show how each layer 0 DSM will split its channels into two eta groups. In the central phi region, the numbers show how the trigger patches are connected to the ten input channels of the layer 0 DSM boards. This (including the phi switch) is unchanged from the current cabling scheme, as shown in Figure 3. The sidebars for the layer 1 DSM boards are now oriented horizontally to indicate that each one receives data from both East and West sides of the detector. The East-side layer 0 DSM boards will connect to the even-numbered channels of the layer 1 boards, and the West-side layer 0 boards will connect to the odd-numbered channels. It can be seen that there is a difference in the cabling of the upper (in this diagram) and lower layer 1 DSM boards. The upper layer 1 DSM board receives data from the single–output layer 0 DSM boards on channels 0:3, and the data from the double-output boards on channels 4 and 5. The lower layer 1 DSM board receives the data from the double-output boards on channels 0 and 1, and the single-output boards on the other channels. Since the format of the data will always be the same the cabling difference will not matter, and all of the layer 1 DSMS will be able to use the same algorithm.

BEMC Layer 0 Algorithm Description

From Figure 4 it can be seen that it will be necessary to have four different algorithms for the layer 0 DSM boards: single-output East (negative eta), single-output West (positive eta), double-output East and double-output West. It should be noted that, as well as summing different groups of channels, the double-output layer 0 algorithms also switch their output mapping between the East and West sides. This will take care of the phi switch that is currently dealt with at layer 1.

Single-output East

- RBT File: bemc_be001_2009_a.rbt
- Users: BE001:BE002, BE004:BE007, BE009:BE012, BE014:BE105
- Input: 10 BEMC channels: bits 0:5 = high tower, bits 6:11 = trigger patch
- LUT: Pedestal subtraction and energy calibration is done in the BEMC read-out electronics. Therefore the LUT's are mostly 1-to-1. Missing, dead and non-instrumented channels are zeroed out here.
- Registers: Four registers, each containing one 6-bit threshold value for the high tower comparison. Unlike in the past, these are NOT size ordered.
    - R0: BEMC-HT-th0 (6 bits)
    - R1: BEMC-HT-th1 (6)
    - R2: BEMC-HT-th2 (6)
    - R3: BEMC-HT-th3 (6)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum TP channels 0:5 (low eta) and 6:9 (high eta). In parallel with the sum logic, compare each HT value to 4 thresholds.

- Step 3: Subtract the pedestal from each TP sum. The pedestal is defined as (N-1) where “N” is the number of channels that were added together to make the TP sum. If the initial TP sum is less than N, then the result of the pedestal subtraction process shall be zero. Next, select the lower 6 bits of each pedestal-subtracted TP sum. Set all 6 bits high (63) if any higher-order bits are set in the pedestal-subtracted sum. In parallel with this, combine (OR) the HT bits for each threshold together.
- Step 4: Send the two 6-bit sums (low and high eta) and the 4 HT bits to layer 1 on one output cable.

Single-output West

- RBT File: bemc_bw001_2009_a.rbt
- Users: BW001:BW002, BW004:BW007, BW009:BW012, BW014:BW105
- Input: Same as Single-output East algorithm
- LUT: Same as Single-output East algorithm
- Registers: Same as Single-output East algorithm
- Algorithm: Same as Single-output East algorithm, except the low and high eta TP sums at Step 2 involve channels 0:3 and 4:9 respectively, instead of 0:5 and 6:9.

Double-output East

- RBT File: bemc_be003_2009_a.rbt
- Users: BE003, BE008, BE013
- Input: Same as Single-output East algorithm
- LUT: Same as Single-output East algorithm
- Registers: Same as Single-output East algorithm
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum TP channels in four groups: 0, 2 and 4 (low eta), 6 and 8 (high eta), 1, 3 and 5 (low eta) and 7 and 9 (high eta). In parallel with the sum logic, compare each HT value to 4 thresholds.
- Step 3: Subtract the pedestal from each TP sum and then select the lower 6 bits, as in the single-output East algorithm. In parallel with this, combine (OR) the HT bits from the even-numbered input channels and the odd-numbered input channels separately.
- Step 4: Send the two 6-bit sums (low and high eta) and the 4 HT bits from the even-numbered channels to the upper (in Figure 4) layer 1 DSM board on the first output cable. Send the data from the odd-numbered channels to the lower DSM board on the second output cable.

Double-output West

- RBT File: bemc_bw003_2009_a.rbt
- Users: BW003, BW008, BW013
- Input: Same as Single-output East algorithm
- LUT: Same as Single-output East algorithm
- Registers: Same as Single-output East algorithm
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.

- Step 2: Sum TP channels in four groups: 0 and 2 (low eta), 4, 6 and 8 (high eta), 1 and 3 (low eta) and 5, 7 and 9 (high eta). In parallel with the sum logic, compare each HT value to 4 thresholds.
- Step 3: Subtract the pedestal from each TP sum and then select the lower 6 bits, as in the single-output East algorithm. In parallel with this, combine (OR) the HT bits from the even-numbered input channels and the odd-numbered input channels separately.
- Step 4: Send the two 6-bit sums (low and high eta) and the 4 HT bits from the even-numbered channels to the ***lower*** layer 1 DSM board on the ***second*** output cable. Send the data from the odd-numbered channels to the ***upper*** DSM board on the ***first*** output cable. (NOTE: Bold italics indicate the difference in output mapping between this algorithm and the East-side algorithm).

In all four algorithms the output data on each cable will therefore have the same format, which is shown in Table 1:

Table 1: Output of Layer 0 BEMC DSM Boards

Data	Bit Range	Bit Count	Bit Total
TP sum for low-eta group	0:5	6	16
TP sum for high-eta group	6:11	6	
HT bits	12:15	4	

<u>BEMC Layer 1 Algorithm Description</u>

There will be just one layer-1 algorithm for the BEMC, which will be used by all 6 DSM boards:

- RBT File: bemc_bc101_2009_a.rbt
- Users: BC101:BC106
- Input: 6 channels, each with the format given in Table 1
- LUT: 1-to-1 mapping
- Registers: Three registers, each containing one 9-bit threshold value for the jet patch comparison. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2
    - R0: BEMC-JP-th0 (9 bits)
    - R1: BEMC-JP-th1 (9)
    - R2: BEMC-JP-th2 (9)
- Step 1: Receive two 6-bit TP sums (low and high eta) and 4 HT bits on each of 6 cables. Four of the cables come from single-output layer 0 DSM boards. The other two cables come from two different double-output layer 0 DSM boards. The low and high eta sums will be referred to as ChX_{LO} and ChX_{HI} to indicate which channel, and which eta range, are being selected.
- Step 2: Calculate 3 jet patches sums as follows:
    - JPX ($-1 < \eta < 0$) = $Ch0_{LO} + Ch0_{HI} + Ch2_{LO} + Ch2_{HI} + Ch4_{LO} + Ch4_{HI}$
    - JPY ($-0.6 < \eta < 0.4$) = $Ch0_{LO} + Ch1_{LO} + Ch2_{LO} + Ch3_{LO} + Ch4_{LO} + Ch5_{LO}$

- JPZ ($0 < \eta < 1$) = $Ch1_{LO} + Ch1_{HI} + Ch3_{LO} + Ch3_{HI} + Ch5_{LO} + Ch5_{HI}$

In parallel, calculate the partial jet patch sum to be combined with the EEMC data at layer 2:

- JPpartial ($0.4 < \eta < 1$) = $Ch1_{HI} + Ch3_{HI} + Ch5_{HI}$

Also, in parallel, combine (OR) the HT bits from input channels 0:2 and 3:5 separately.

- Step 3: Compare each of JPX, JPY and JPZ to three thresholds and then pack the results for each jet patch into a 2-bit integer (this is the same logic as has been used for many years now). Select the lower 6 bits of JPpartial, and set all bits high (63) if any of the higher order bits of JPpartial are set. Combine (OR) the two intermediate groups of HT bits together.
- Step 4: Send, to layer 2, the 2-bit integer for each of the three completed jet patches, along with the 4 HT bits and 6 bits of JPpartial. The output data format is shown in Table 2.

Table 2: Output of Layer 1 BEMC DSM Boards

Data	Bit Range	Bit Count	Total
JPX threshold bits	0:1	2	16
JPY threshold bits	2:3	2	
JPZ threshold bits	4:5	2	
JPpartial sum	6:11	6	
HT bits	12:15	4	

EEMC Cabling Detail

Figure 5 shows the current scheme for connecting the EEMC trigger patches to the layer 0 DSM boards, as seen from the West looking towards the center of STAR. The thick solid lines indicate which areas are connected to each layer 0 DSM board. The thin dashed lines outline the individual trigger patches. A pair of adjacent jet patches is highlighted. The numbers indicate which layer 0 DSM board channel is connected to each trigger patch.

It can be seen that every EEMC (1x1) jet patch is split between two layer 0 DSM boards. In each case, the 10 outer trigger patches (lowest eta) are connected one layer 0 DSM board, and the 5 inner trigger patches (highest eta) are connected to another layer 0 DSM board. That second board also contains the five inner trigger patches for the adjacent jet patch. In the current cabling scheme the boards that cover the outer trigger patches each have one output cable. The boards that cover the inner trigger patches of two jet patches have two output cables. The result is twelve cables which are split between two layer 1 DSM boards in such a way that each of the layer 1 DSM boards covers half of the EEMC.

The aim of the new cabling and algorithm scheme is to make jet patches that overlap in eta and fill the acceptance gaps caused by having fixed jet patches. The EEMC only covers one unit of eta so it is not possible to make multiple (1x1) jet patches that overlap

in eta and are totally internal to the EEMC. All that is possible is to make the original internal (1x1) jet patch and a partial (0.4x1) jet patch on the EEMC-BEMC boundary that can be combined with the partial jet patch (JPpartial) from the BEMC side of the boundary. The current EEMC cabling scheme is already set up to construct (1x1) jet patches with the same phi range as in the BEMC. The partial (0.4x1) jet patch can be constructed by summing together the even numbered channels of the single-output layer 0 DSMS (which cover the low eta part of the EEMC). As a result, there is no need to make any cabling changes within the EEMC system, and the EEMC layer 0 algorithms will be minor variations of the BEMC algorithms.

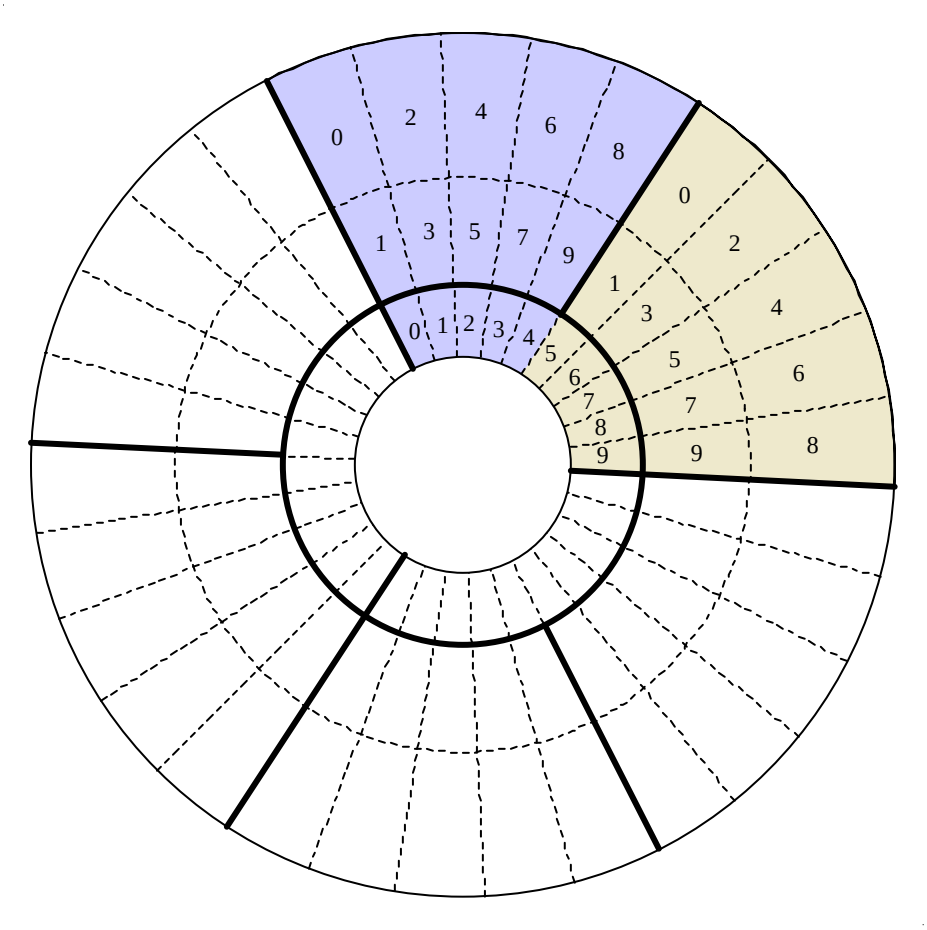

Figure 5: EEMC DSM Eta-Phi Scheme, seen from the West looking towards the center of STAR

The EEMC layer 0 algorithms will differ from the BEMC algorithms primarily in the definition of which groups of channels are added together to make the TP sums. The single-output EEMC layer 0 DSM boards will add together the even-numbered (low eta) channels in one group, and the odd-numbered (high-eta) channels in another group. The low eta group forms the partial jet patch that can be combined with the BEMC partial jet patch at layer 2. The double-output EEMC layer 0 DSM boards will add together channels 0:4 in one group, and channels 5:9 in the other (as indicated in Figure 5).

However, there will be an additional difference associated with the pedestal subtraction. The BEMC layer 0 algorithms do the pedestal subtraction such that each TP sum is left with a residual pedestal of 1. Six TP sums are added together to make a jet patch, so the BEMC jet patch pedestal value is 6. Only three TP sums are added together to make the partial jet patch (JPpartial), so it's pedestal value is 3. In order to simplify later analysis it would be useful to ensure that all jet patches, including those that come from the EEMC and the BEMC-EEMC boundary, also have a pedestal value of 6. To this end, the pedestal subtraction in the EEMC layer 0 algorithms will be done as shown in Table 3. Note that "N" is still the number of channels that are added together to make the TP sum, just like in the BEMC logic. In the case of the EEMC algorithms, "N" is always 5.

Table 3: TP sum Pedestal Calculations in the EEMC Layer 0 Algorithms

TP Sum	Pedestal Subtraction Equation	Residual Pedestal
Low eta sum from single-output DSM	TPsum = TPsum-(N-3)	3
High eta sum from single-output DSM	TPsum = TPsum-(N-2)	2
Sum from double-output DSM	TPsum = TPsum-(N-1)	1

When the three sums listed in Table 3 are added together to make an internal EEMC jet patch the total pedestal value of the jet patch is 6, which matches the BEMC. When the low eta sum from the single-output DSM is added to JPpartial, from the BEMC, to complete the boundary-spanning jet patch, the total pedestal for that jet patch also comes to 6, again matching the BEMC.

EEMC Layer 0 Algorithm Description

Single-output (Low Eta)

- RBT File: eemc_ee001_2009_a.rbt
- Users: EE001, EE003, EE004, EE006, EE007, EE009
- Input: 10 EEMC channels: bits 0:5 = high tower, bits 6:11 = trigger patch
- LUT: Pedestal subtraction and energy calibration is done in the EEMC read-out electronics. Therefore the LUT's are mostly 1-to-1. Missing, dead and non-instrumented channels are zeroed out here.
- Registers: Two registers, each containing one 6-bit threshold value for the high tower comparison. Unlike in the past, these are NOT size ordered.
    - R0: EEMC-HT-th0 (6 bits)
    - R1: EEMC-HT-th1 (6)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum the five even numbered (low eta) TP channels and the five odd numbered (high eta) channels separately. In parallel with the sum logic, compare each HT value to 2 thresholds.
- Step 3: Subtract the pedestal from each TP sum. The pedestal subtraction equations are described in Table 3. If the initial TP sum is less than N (5), then the result of the pedestal subtraction process shall be zero. Next, select the lower 6

bits of each pedestal-subtracted TP sum. Set all 6 bits high (63) if any higher-order bits are set in the pedestal-subtracted sum. In parallel with this, combine (OR) the HT bits together.

- Step 4: Send the two 6-bit TP sums (low and high eta) and the 2 HT bits to layer 1 on one output cable.

Double-output (High Eta)

- RBT File: eemc_ee002_2009_a.rbt
- Users: EE002, EE005, EE008
- Input: Same as Single-output (Low Eta)
- LUT: Same as Single-output (Low Eta)
- Registers: Same as Single-output (Low Eta)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Step 2: Sum the TP channels in two groups: (0:4) and (5:9). In parallel with the sum logic, compare each HT value to 2 thresholds.
- Step 3: Subtract the pedestal from each TP sum using the equation from Table 3, and then select the lower 6 bits, as in the single-output (low eta) algorithm. In parallel with this, combine (OR) the HT bits from channels (0:4) and (5:9) separately.
- Step 4: Send the 6-bit sum and the 2 HT bits from channels (0:4) to layer 1 on the first output cable. On the cable, the sum will be in the bit range used by the low-eta sum in the single-output algorithm. The bits assigned to the high-eta sum will be set to zero. Send the data from channels (5:9) to layer 1 on the second output cable.

In both algorithms the output data on each cable will therefore have the similar formats, as shown in Table 4:

Table 4: Output of Layer 0 EEMC DSM Boards

Data	Bit Range	Bit Count	Bit Total
TP sum for low-eta group	0:5	6	16
TP sum for high-eta group (N/A, set to zero, for the double-output algorithm)	6:11	6	
HT bits	12:13	2	
Unused	14:15	2	

EEMC Layer 1 Algorithm Descriptions

One aspect of the new EEMC layer 1 algorithms will be different from the past: there will be separate algorithms for the two DSM boards. This is due to a feature of the layer 0 to layer 1 connection that was not relevant to past algorithms, but is important now. These connections are shown in Figure 6. As in Figure 5, the thick solid lines indicate which areas are connected to each layer 0 DSM board. The dashed lines show how the inner

regions are split by the layer 0 DSM boards to make pieces of two adjacent jet patches. The arrows show how the outputs of the layer 0 DSM boards (including both outputs from the double-output boards) connect to the input channels of the two layer 1 DSM boards.

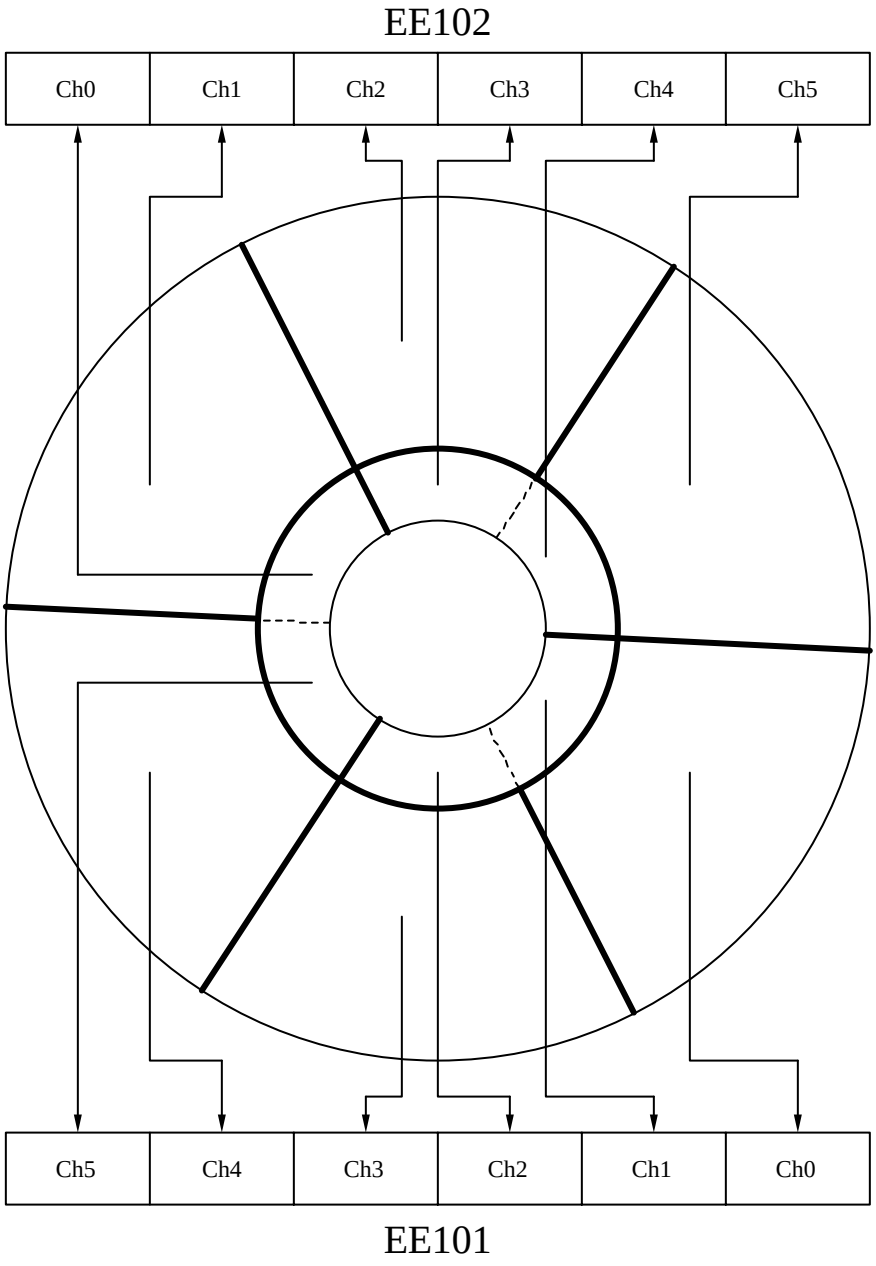

Figure 6: The EEMC Cabling Scheme, with the Endcap seen from the West looking toward the center of STAR.

It can be seen that the layer 1 DSM board covering the bottom half of the EEMC (EE101) receives data from the outer (low eta) parts of its jet patches on input channels 0, 3 and 4. It is therefore these channels that will provide the partial jet patch information that needs

to be passed up to layer 2. However, the layer 1 DSM board covering the upper half of the EEMC (EE102) receives data from the outer parts of its jet patches on input channels 1, 2 and 5, so it is these channels that will provide the partial jet patch information. The two layer 1 DSM boards will therefore need to be slightly different, to account for this difference in the input mapping.

Lower Half (EE101)

- RBT File: eemc_ee101_2009_a.rbt
- User: EE101
- Input: 6 channels, each with the format given in Table 4 (see Page 12)
- LUT: 1-to-1 mapping
- Registers: Three registers, each containing one 8-bit threshold value for the jet patch comparison. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2
    - R0: EEMC-JP-th0 (8 bits)
    - R1: EEMC-JP-th1 (8)
    - R2: EEMC-JP-th2 (8)
- Step 1: Receive two 6-bit TP sums (low and high eta) and 2 HT bits on each of six cables. Three of these cables (channels 0, 3 and 4) come from single-output layer 0 DSM boards. The other three cables (channels 1, 2 and 5) come from double-output layer 0 DSM boards, and on those cables the second 6-bit TP sum will always be zero. The sums will be referred to as ChX_{LO} and ChX_{HI} to indicate which channel, and which eta range, are being selected.
- Step 2: Calculate 3 jet patches sums as follows:
    - JPA (4 o'clock) = $Ch0_{LO} + Ch0_{HI} + Ch1_{LO}$
    - JPB (6 o'clock) = $Ch3_{LO} + Ch3_{HI} + Ch2_{LO}$
    - JPC (8 o'clock) = $Ch4_{LO} + Ch4_{HI} + Ch5_{LO}$

  In parallel, compare pairs of the low eta sums arriving from the single-output layer 0 DSM boards (i.e. $Ch0_{LO}$, $Ch3_{LO}$ and $Ch4_{LO}$). Also combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
- Step 3: Combine (OR) the two intermediate groups of HT bits together. Compare each of JPA, JPB and JPC to three thresholds and then pack the results for each jet patch into a 2-bit integer (this is the same logic as has been used for many years now). Combine the results of the 2-channel comparisons (calculated at Step 2) to select the largest low eta sum.
    - A (4 o'clock) = ($Ch0_{LO} > Ch3_{LO}$) and not ($Ch4_{LO} > Ch0_{LO}$)
    - B (6 o'clock) = ($Ch3_{LO} > Ch4_{LO}$) and not ($Ch0_{LO} > Ch3_{LO}$)
    - C (8 o'clock) = ($Ch4_{LO} > Ch0_{LO}$) and not ($Ch3_{LO} > Ch4_{LO}$)

  This is the partial jet patch that will be sent on to layer 2. Note that if all three low eta sums are the same (e.g. in an event where nothing happens) then all three comparisons will be false. In this case, sum A, at 4 o'clock, is selected. Use a 2-bit integer to indicate which of the three sums has been selected.
    - 1 = A (4 o'clock)
    - 2 = B (6 o'clock)
    - 3 = C (8 o'clock)

- Step 4: Send, to layer 2, the 2-bit integer for the three completed jet patches, along with the 6 bits of selected partial jet patch sum, its 2-bit ID and the 2 HT bits. The output data format is shown in Table 5.

Table 5: Output of Layer 1 EEMC DSM Boards

Data	Bit Range	Bit Count	Total
JPA threshold bits	0:1	2	16
JPB threshold bits	2:3	2	
JPC threshold bits	4:5	2	
Selected partial jet patch sum	6:11	6	
Partial jet patch ID	12:13	2	
HT bits	14:15	2	

Upper Half (EE102)

- RBT File: eemc_ee102_2009_a.rbt
- User: EE102
- Input: Same as Lower Half (EE101)
- LUT: Same as Lower Half (EE101)
- Registers: Same as Lower Half (EE101)
- Step 1: Receive two 6-bit TP sums (low and high eta) and 2 HT bits on each of six cables. Three of these cables (channels 1, 2 and 5) come from single-output layer 0 DSM boards. The other three cables (channels 0, 3 and 4) come from double-output layer 0 DSM boards, and on those cables the second 6-bit TP sum will always be zero. Note that this mapping is exactly the opposite of the mapping into the first layer 1 DSM board (EE101).
- Step 2: Calculate 3 jet patches sums as follows:
  - JPA (10 o'clock) = $Ch1_{LO} + Ch1_{HI} + Ch0_{LO}$
  - JPB (12 o'clock) = $Ch2_{LO} + Ch2_{HI} + Ch3_{LO}$
  - JPC (2 o'clock) = $Ch5_{LO} + Ch5_{HI} + Ch4_{LO}$

  In parallel, compare pairs of the low eta sums arriving from the single-output layer 0 DSM boards (i.e. $Ch1_{LO}$, $Ch2_{LO}$ and $Ch5_{LO}$). Also combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
- Step 3: Combine (OR) the two intermediate groups of HT bits together. Compare each of JPA, JPB and JPC to three thresholds and then pack the results for each jet patch into a 2-bit integer (this is the same logic as has been used for many years now). Combine the results of the 2-channel comparisons (calculated at Step 2) to select the largest low eta sum.
  - A (10 o'clock) = ($Ch1_{LO} > Ch2_{LO}$) and not ($Ch5_{LO} > Ch1_{LO}$)
  - B (12 o'clock) = ($Ch2_{LO} > Ch5_{LO}$) and not ($Ch1_{LO} > Ch2_{LO}$)
  - C (2 o'clock) = ($Ch5_{LO} > Ch1_{LO}$) and not ($Ch2_{LO} > Ch5_{LO}$)

This is the partial jet patch that will be sent on to layer 2. Note that if all three low eta sums are the same (e.g. in an event where nothing happens) then all three comparisons will be false. In this case, sum A, at 10 o'clock, is selected. Use a 2-bit integer to indicate which of the three sums has been selected.
    - 1 = A (10 o'clock)
    - 2 = B (12 o'clock)
    - 3 = C (2 o'clock)
- Step 4: Send, to layer 2, the 2-bit integer for the three completed jet patches, along with the 6 bits of selected partial jet patch sum, its 2-bit ID and the 2 HT bits. The output format is the same as shown in Table 5.

EMC Layer 2 Algorithm Description

The final piece of this DSM tree is the DSM board at layer 2, where the BEMC and EEMC data will be combined. The input map to this DSM board is shown in Table 6:

Table 6: Input Map for the EMC Layer 2 DSM Board

Channel	Source	Phi
0	BEMC BC101	10 o'clock
1	BEMC BC102	12 o'clock
2	BEMC BC103	2 o'clock
3	BEMC BC104	4 o'clock
4	BEMC BC105	6 o'clock
5	BEMC BC106	8 o'clock
6	EEMC EE101	4, 6 and 8 o'clock
7	EEMC EE102	10, 12 and 2 o'clock

The task of this algorithm is to complete the jet patches that overlap the BEMC-EEMC boundary, combine the jet patch threshold and high tower bits for each detector and implement the adjacent jet patch logic. This year there is no need for either the J/Psi logic (non-adjacent jet patches) or the back-to-back logic (back-to-back jet patches) so those will not be included.

The data from the BEMC has the format shown in Table 2, and the data from the EEMC has the format shown in Table 5. It can be seen from Table 5 that each EEMC layer 1 DSM deals with 3 jet patches, but there are only enough bits available to pass one partial jet patch sum. The largest partial sum is chosen to be sent. This means the layer 2 DSM board will only be able to complete two of the six jet patches that overlap the BEMC-EEMC boundary. This is not enough to make a useful contribution to the adjacent jet patch logic so they will not be included in that logic.

The layer 2 DSM for the EMC tree will therefore perform the following steps:

- RBT File: l1_em201_2009_a.rbt
- User: EM201

- Input: 6 channels from BEMC, each with the format given in Table 2, and 2 channels from the EEMC, each with the format given in Table 5.
- LUT: 1-to-1 mapping
- Registers: Three registers, each containing one 7-bit threshold value for the jet patch comparison of the boundary-spanning patches. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2
    - R0: BEMC-EEMC-overlap-JP-th0 (7 bits)
    - R1: BEMC-EEMC-overlap-JP-th1 (7)
    - R2: BEMC-EEMC-overlap-JP-th2 (7)
- Step 1: Receive all the information from the six BEMC layer 1 DSMS, and the two EEMC layer 1 DSMS.
- Step 2: Complete all 6 possible boundary-spanning jet patches in parallel by adding the partial jet patch sums received from the EEMC to each of the partial jet patch sums received from the BEMC. Table 7 shows which BEMC JPpartial sums are combined with the JPpartial sum received from each of EE101 and EE102. Note that only two of these six sums are valid at any one time. The selection of the valid sums will be done at Step 3.

Table 7: Boundary-Spanning Jet Patch Completion

DSM	Patch Location	ID	BEMC JPpartial Sum
EE101	4 o'clock	1	Ch3 – BC104
	6 o'clock	2	Ch4 – BC105
	8 o'clock	3	Ch5 – BC106
EE102	10 o'clock	1	Ch0 – BC101
	12 o'clock	2	Ch1 – BC102
	2 o'clock	3	Ch2 – BC103

  Delay the partial-jet-patch ID from EE101 and EE102 to Step 3.
  Combine (OR) the HT bits from the six BEMC layer 1 DSMS.
  Combine (OR) the HT bits from the two EEMC DSMS.
  Unpack the JP bits from the BEMC and EEMC. In each case, JP0 is the lowest threshold bit, JP1 refers to the middle threshold and JP2 is the highest threshold.
- Step 3: Delay all of the HT bits.
  Combine (OR) the JP bits for the BEMC and EEMC separately.
  Compare all six completed boundary jet patches to three thresholds. Then use the partial-jet-patch ID from each of the two EEMC layer 1 DSMS ("ID" column in Table 7) to identify which two of these six sets of threshold bits are valid this time. Combine (OR) those results with the BEMC-only and EEMC-only bits to make a set of JP threshold bits that are unified across the whole calorimeter.
  Search for jet patches that are adjacent in phi. The search will be done independently, and therefore in parallel, in each of the four eta regions covered by the BEMC-only and EEMC-only jet patches, i.e. $-1<\eta<0$, $-0.6<\eta<0.4$, $0<\eta<1$ and $1<\eta<2$. Note that the boundary-spanning patches are ignored by the adjacent jet patch logic. The search will involve all jet patches that exceed the lowest jet patch threshold, so the logic will look for specific combinations of the JP0 threshold

bits. Within any eta region the adjacent jet patch bit (AJP) will be calculated from:

AJP = (2 o'clock and 4 o'clock) or
(4 o'clock and 6 o'clock) or
(6 o'clock and 8 o'clock) or
(8 o'clock and 10 o'clock) or
(10 o'clock and 12 o'clock) or
(12 o'clock and 2 o'clock)

Finally, combine (OR) the AJP bit for the 3 eta regions contained within the BEMC, and separately combine all the AJP bits to make one bit unified over BEMC and EEMC.

- Step 4: Send to the next layer (either the last DSM or the new TCU) the HT bits, some of the JP bits and the adjacent jet patch bits. The output data format is shown in Table 8.

Table 8: Output of Layer 2 EMC DSM Board

Data	Bit Range	Bit Count	Total
Barrel HT bits	0:3	4	15
Endcap HT bits	4:5	2	
JP1, unified over the BEMC+EEMC	6	1	
JP2, unified over the BEMC+EEMC	7	1	
BJP1 for the 18 BEMC-only patches	8	1	
BJP2 for the 18 BEMC-only patches	9	1	
EJP1 for the 6 EEMC-only patches	10	1	
EJP2 for the 6 EEMC-only patches	11	1	
AJP for BEMC and EEMC but NOT the boundary	12	1	
BAJP for the BEMC-only patches	13	1	
EAJP for the EEMC-only patches	14	1	