The National Technology Roadmap for Semiconductors

Technology Needs

1997 Edition

SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

SIA **SEMICONDUCTOR INDUSTRY ASSOCIATION**

THE NATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

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FOREWORD

The semiconductor industry is unique in having sustained such rapid technology development over so long a period. This has enabled the industry to provide electronic products with substantially lower cost per function as well as higher performance each year. As a result, the semiconductor market has grown at an average rate of approximately 15% annually over the past three and a half decades. Maintaining this growth for as long as possible is a primary goal of the member companies of the Semiconductor Industry Association (SIA), and it is also highly important to their suppliers, customers, the overall U.S. economy, and national defense.

However, it now appears that the industry is rapidly approaching a formidable "100 nm barrier," consisting of an unprecedented number of distinct technical challenges which threaten continuation of its historical success formula. Hopefully, this Roadmap can be used as a focal point for reaching agreement on what needs to be addressed and as a guide to marshall adequate resources required to support the research and development needed to overcome this "barrier."

Since 1992, the SIA has coordinated a process for building consensus on the future technology requirements for maintaining the historical rate of advancement out to a 15-year horizon. The resulting vision is documented as *The National Technology Roadmap for Semiconductors* (NTRS), of which this is the third edition. As in the previous two editions (1992 and 1994), the focus of the 1997 Roadmap remains on the technology needs for mainstream, leading-edge, silicon technology. The Roadmap provides a snapshot of the current thinking of technologists and exposes opportunities for inventing new solutions, especially as they might have applicability to the longer-range needs expressed in the Roadmap. The NTRS is intended to be a Roadmap of technology needs, not solutions.

It is for this reason that the SIA Roadmap Coordinating Group (RCG) has put greater emphasis on quantitative expression of requirements in the 1997 edition—numbers are less likely to be confused with "suggested solutions." Of course, some potential solutions have been included to inform the reader of the current approaches to develop the technology needed—but technologists must always remain open to better ideas! The RCG is particularly concerned about the amount of "red" in the 1997 Roadmap, indicating that the industry is considerably more "idea limited" about potential solutions to many of the technical challenges within the 15-year horizon than it was in the previous editions.

The National Technology Roadmap for Semiconductors has always been much more than just a document. It is the result of a consensus-building process that has become more thorough with each succeeding edition. This 1997 version is the result of greater participation in Technology Working Groups (TWGs), more discussion, and more coordination than ever before. For example, four distinct teams, with separate tasks/perspectives, were involved just in the creation of the Overall Roadmap Technology Characteristics (ORTC). The Roadmap ORTC information is the main coordinating guideline for the more detailed work in each technology area by the corresponding TWGs.

The RCG trusts that this 1997 edition of the NTRS provides an appropriate level of detail to guide the semiconductor research and development investments of industry, government, and universities. The RCG thanks the many technologists from all three sectors who worked so hard on the TWGs to combine their best estimates into this document. It is hoped that this consensus will serve the needs of those making decisions about funding and/or participating in the research and development required to continue the rapid progress of the semiconductor industry.

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INTRODUCTION

OVERVIEW

The National Technology Roadmap for Semiconductors is a 15-year projection of the integrated circuit technology characteristics required to maintain the historical rate of performance and cost improvements. It documents the consensus designed to guide the efforts of research organizations, and research sponsors within industry, government, and universities. Most importantly, the Roadmap identifies the research needs that must be fulfilled to realize the required technology advancements. The technology and research requirements were established by extending historic trends for dynamic random access memory (DRAM) bit count, logic performance, and mixed signal integration over the next 15 years (to 2012). The Roadmap continues to call for reduction in geometric dimensions in accordance with Moore's Law, but allows for short-term adjustments based on current practices.

The primary focus of this Roadmap is on technology required for silicon complementary metal-oxide semiconductor (CMOS) integrated circuits, including mixed signal products. This group constitutes over 75% of the world's semiconductor consumption and therefore requires the core technology competencies used for designing and manufacturing semiconductors. These same competencies provide many of the primary advancements for other semiconductor products such as compound semiconductor, microwave, and discrete devices. To a large extent the Roadmap therefore serves as a technology guide for all semiconductor products.

A concerted effort has been made to estimate in a coherent, self-consistent manner the Roadmap "target" values of the many parameters that characterize the advancement in each technology area for each succeeding technology generation or "node." The high-level targets, as expressed in the Overall Roadmap Technology Characteristics table, are based on the compelling economic and competitive necessity to maintain the current high rate of advancement in integrated circuit technologies.

With these high-level targets as a coordinating guide, the more detailed future technology requirements in each area have been derived by the Technology Working Groups. The TWGs have also made assessments of the industry's ability to meet these requirements on schedule with continuation of present levels of research effort. The culmination of this assessment is a time-phased list of the most critical requirements in each area that need special attention from the R&D performers and their supporters to ensure that the overall goals of the Roadmap are realized. These requirements are generally expressed as "quantitative targets," in part to facilitate the distinction between the estimated needs and potential solutions.

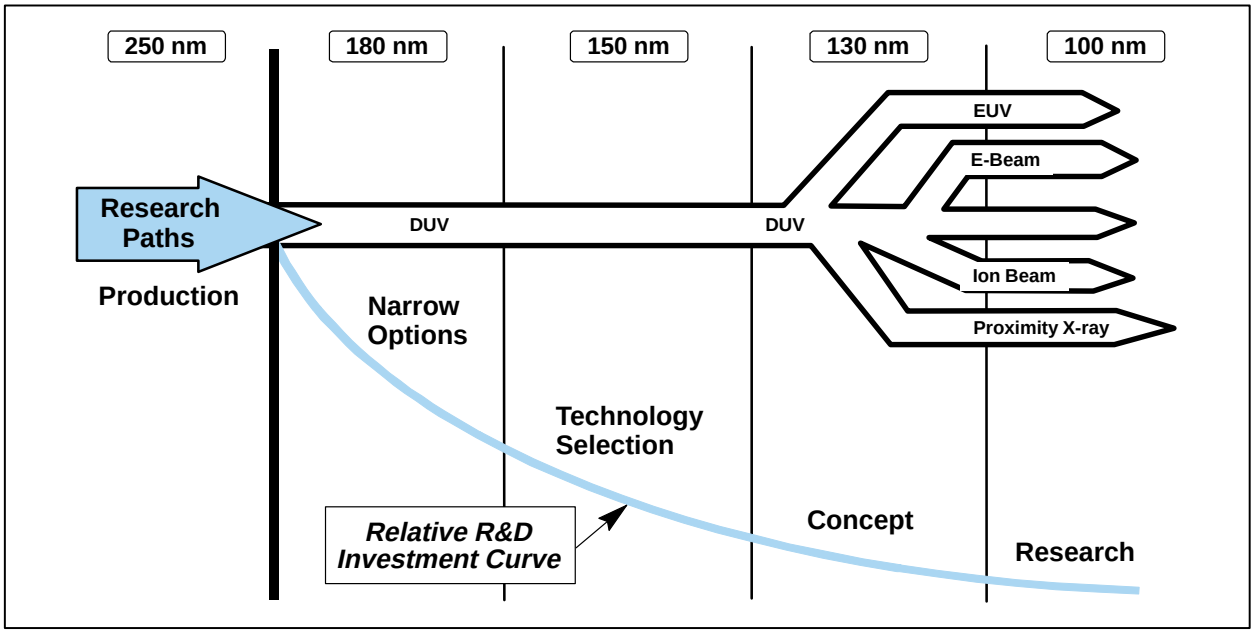
It is *not* the intent of this document to convey or to be interpreted as portraying the most likely solutions to be adopted, nor to focus attention on those potential solutions currently known at the expense of other innovative concepts. Also, this document should *not* be interpreted as having solved all problems or even as identifying the solutions to all problems. In fact, it is eagerly hoped that this Roadmap will inspire additional innovative concepts for consideration. Future success depends on new concepts.

In the description of the research needs, some of the potential technical solutions are listed, where known, to convey current thinking and efforts. Furthermore, the listing of a particular potential solution does not constitute an endorsement by the Roadmap process. On the contrary, it is a strong intent of this Roadmap to enhance communication and stimulate creative, innovative solutions to the many critical issues and research needs identified herein.

THE ROADMAP STRUCTURE

This 1997 revision extends the time line one more generation beyond that of the 1994 Roadmap to 50 nm technology requirements in 2012. The Overall Roadmap Technology Characteristics chart (Table B1 in Appendix B) sets the high-level projections for the Roadmap. (It is important to understand the assumptions and limitations upon which Table B1 is based. These assumptions are also defined in Appendix B.) The six generations of future semiconductor technology requirements and research needs addressed in the Roadmap are categorized by minimum geometric feature sizes and the year in which products incorporating these feature sizes will be available commercially. These six generations encompass a spectrum of technologies, each of which may require the investigation of multiple alternative solutions.

Figure 1 is a conceptual illustration showing the spectrum of technology covered by the first four generations of the Roadmap using lithography as an example. It illustrates uncertainties in the research and development options or approaches to be pursued. However, no matter what direction the industry takes, the general performance requirements outlined as the Technology Characteristics must be met.



DUV—deep ultraviolet
EUV—extreme ultraviolet
E-beam—electron beam

Figure 1 Conceptual Illustration of Today's Research and Development Investments for Future Production Technologies

As depicted in Figure 1, 250 nm integrated circuits are now in production. The technology choices for the 180 nm generation of integrated circuits have been narrowed and solutions have been chosen. However, large investments for 180 nm generation are required to make the selected solutions production ready and to integrate them into effective design and manufacturing processes. It should be noted that the equipment, materials, and unit processes must be proven prior to technology integration and hardening. During this phase, large capital investments will also be made in production facilities. The combined technology investment and capital investment represent a large risk, making it imperative that the technology work flawlessly upon the start of production. Semiconductor manufacturers and equipment/material suppliers are the primary participants in this area.

The focus of activities changes for the 150 nm generation. These efforts focus on finalizing the selection of a deep ultraviolet (DUV) solution that will meet the technology requirements in 2001. There are more choices to be made and therefore the available research funding is shared by all possible solutions.

For 130 nm, researchers are performing "proof of concept" for an even larger number of techniques and methods to fulfill the requirements in 2003. Prior to making large investments in any one technology alternative, efforts must focus on proof of concept for those critical but unproved elements. All sectors of the semiconductor R&D community participate in research for these technologies.

For the 100 nm generation and smaller, a vigorous creative research activity is required. There are many areas of technology for which no potential solutions are known. The research that addresses this area of the Roadmap is focused on identifying, evaluating, and developing new concepts, methods, and techniques that might enable the fulfillment of the requirements in the year 2006 and beyond. This area requires the most innovative research, including serious consideration of paradigm changes. All possible approaches should be considered "on the Roadmap" for this area.

Because of the risk associated with large investments, the first two generations receive the most attention and consume the larger portion of the available research and development funds. Beyond the 180 nm and 150 nm generations, the focus is divided among many alternatives. Without additional funding, research on these alternatives may have to share a smaller amount of funding; therefore, awards for this area of research may be spread thin.

In the past, for the out-years of the Roadmap, only a small amount of funding has been available, requiring researchers who work in this area to manage on their determination and salesmanship abilities. However, there is a much greater appreciation of the magnitude of the critical problems beyond 130 nm. *Availability of adequate funding for innovative research targeted at generations beyond 130 nm is a compelling issue that must be addressed.*

In recent years the research challenges have exploded while funding has remained, at best, constant. The SIA has recognized the need to apply additional funding to technology activities at 100 nm and beyond to allow efforts to be directed toward paradigm changes. Since the government has played a key role in the past in funding basic research, increased industry investment does not diminish the need for continued government-supported research. *In addition to the SIA's effort, a coordinated and largely increased resource allocation for the full range of the Roadmap is required. The current rate of advancement in integrated circuit technology must continue well into the future, a critical factor in maintaining the competitiveness of the U.S. semiconductor industry.*

TECHNOLOGY WORKING GROUP SUMMARY

The 1994 Roadmap was developed with eight Technology Working Groups, most of which represented the mainstream business activities, or focused "natural workgroups" that occur in typical semiconductor manufacturing businesses. An outcome of the Focus TWG roadmap development was a number of crosscut issues that were handled within and across the Focus TWGs. The crosscut activities' main attribute is that they are required as a portion of most, if not all, of the Focus TWG agendas and have key activities that are supplied to the semiconductor manufacturers.

As a result of the 1994 NTRS experience, the 1997 NTRS was organized with seven Focus Technology Working Groups and four Crosscut Technology Working Groups. The Focus TWGs are Design & Test; Process Integration, Devices, & Structures; Front End Processes; Lithography; Interconnect; Factory Integration; and Assembly & Packaging. These categories of activities are required for semiconductor manufacturers to design and manufacture integrated circuits. The Crosscut TWGs are as follows: Environment, Safety, & Health; Defect Reduction; Metrology; and Modeling & Simulation.

The working group membership was chosen to cover the full spectrum of interests and expertise in each technology area. Participants are representatives from universities, government laboratories, consortia (SEMATECH and Semiconductor Research Corporation [SRC]), industry analysts, equipment and materials suppliers, industry R&D, and the end user—the semiconductor chip makers.

THE FOCUS TECHNOLOGY WORKING GROUPS

Design & Test includes the following focus areas of technologies necessary to comprehend the complexity of advanced integrated circuits:

- Design Environment and Standard Interfaces
- System and IC Verification and Analysis
- Design Techniques and Methodologies
- System-level Design
- Design Syntheses
- Physical Design

The magnitude of the numbers of transistors, the levels of design from accounting for software behavior down to physical circuit behavior, and linking all levels of design hierarchy and achieving an on-chip clock speed of >1 GHz with digital signals is one of the Grand Challenges.

Testing these complex on-chip systems at speed is also a daunting challenge. The Roadmap focus areas for Test are the following:

- Testability
- Testing and Testers
- Known Good Die

Integrated circuits testing is a major product cost factor and must be done in prepackaged and packaged form, including future multiple chip packaging. Design productivity and performance improvement, cost-effective tools covering design verification from system design down to physical transistor, and interconnect design at clock frequencies to >1 GHz and 0.5 volt power supplies is a major challenge.

Front End Processes (formerly Materials and Bulk Processes in the 1994 NTRS) has four primary focus areas, as follows:

- Starting Materials (Wafers)
- Surface Preparation
- Thermal/Thin Films and Doping
- Front End Etch (Plasma etches of the moat, trench isolation, and gate structures)

Major challenges are atomic and molecular scale structures with attendant design, construction, and yield issues. Building affordable integrated transistors and interconnects that achieve clock speeds of >1 GHz at reduced power supply targets (down to 0.5 volts) is also a challenge.

Interconnect focus areas include the following:

- Planarization
- Interconnect Architecture
- Interconnect Reliability
- Metals
- Dielectrics
- Etch

High-speed signal handling requires innovations for on-chip wiring. This is complicated by smaller feature sizes and line widths, thus creating a demand for fine pitch interconnects. Identifying any economically viable alternative to succeed copper and low (κ) dielectrics is a major challenge.

Lithography primary responsibilities are the following focus technologies:

- Exposure Equipment
- Resist Materials and Processing Equipment
- Mask Making, Mask Equipment and Materials

Below 100 nm, the use of conventional "through the lens" optical lithography may not be cost-effective. The technical challenges and complexities of alternative technologies preclude a clear choice of the successor to optical lithography. Regardless of the technology successor choice, it will be expensive to the industry because the entire system of lithography process and tools will need to be developed. An affordable, cost-effective, post-optical lithography system is a critical component of both cost reduction and performance improvement of ICs. This need is a Grand Challenge.

Process Integration, Devices, & Structures (PIDS) includes technology areas for both digital and analog devices. These specific areas are the following:

- Memory and Logic (Memory cells [DRAM, static RAM (SRAM), and nonvolatile] and physical and electrical design rules)
- Analog and Mixed Signal (Unique issues for on-chip structures such as inductors and filters, bilateral capacitors, CMOS bipolar transistors, sensors, micro-electromechanical systems (MEMS), power and high voltage devices, and physical and electrical design rules)
- Process Flow and Short Flow Methodologies, Generic Process Flows
- Reliability (Device reliability modeling, reliability testing [includes wafer level reliability], and burn-in/stress testing)

PIDS is challenged with an increasing set of material choices, materials' limitations at the atomic and molecular level, continuously reducing memory cell sizes, and designing 50 nm gate length transistors. Combining all these technologies to create the optimum, cost-effective IC architecture allowing high clock speeds at reduced power supply voltages and reliable new technologies will be a key to continuing on Moore's Law.

Assembly & Packaging deals with the following focus areas:

- Multi-chip Packaging
- Single-chip Packages
- Bonding Chip/Package/Substrate Design
- Packaging Substrates
- Flip Chip Interconnect (Direct Chip Attach)
- Assembly
- Thermal/Power/Ground Management
- Electrical/Performance Characterization

Assembly and Packaging technologies include the design and the manufacture of the IC packages, but not the printed circuit card manufacture. Major challenges are integrating substrate, packaging, and chip interconnect for increasing chip speeds and thermal dissipation while controlling cost and improving reliability with increasingly complex manufacturing equipment.

Factory Integration focus topics are the following:

- Product and Material Handling
- Process and Equipment Control
- Operational Modeling and Simulation
- Manufacturing Information and Execution Systems
- Productivity Analysis
- Facilities Infrastructure
- Software Improvement
- Human Resources

An enormous part of the manufacturing cost of an IC resides in the semiconductor factory. Controlling factory cost and achieving maximum utilization of precious factory resources is crucial. Yields have improved to the point where little further cost reduction can be achieved, yet maintaining current yields will be increasingly challenging.

Increasing automation and improved system controls both *in situ* in the factory tools as well as information and control systems are key to operational efficiencies. Building factories at forecast wafer sizes of 300 mm and 450 mm and achieving continued product-level cost reduction is the major challenge for Factory Integration.

THE CROSSCUT TECHNOLOGY WORKING GROUPS

Environment, Safety, & Health (ESH) focus topics are as follows:

- Chemical Management
- Natural Resource Management
- Worker Protection Tools
- ESH Design

The ESH technologies ensure the semiconductor industry protects its most valuable resource, the people, as well as the environment itself. The semiconductor industry has an enviable ESH track record and needs to continue to maintain this reputation. Working in concert with government at all levels is an everyday reality. The major challenge is improvement in environmental impact concurrent with manufacturing cost reduction.

Metrology covers the following critical measurement capabilities:

- Critical Dimensions and Overlay
- Physical and Electrical Correlation
- Materials and Contamination Characterization
- Dopant Profile (Dose/Junction Shape)
- *In situ* Sensors for Process Control
- Imaging
- Film Thickness and Profile
- Reference Materials

Process control depends upon measuring critical parameters. An increasing variety of new materials at film thicknesses at atomic and molecular dimensions challenge metrology capability. The major challenge is nondestructive manufacturing capable microscopy for critical dimension measurement, defect detection, and analysis.

Defect Reduction primary technologies cover the following:

- Defect Detection
- Yield Model and Defect Budget
- Defect Sources and Mechanisms
- Defect Prevention and Elimination

Defects are both random (in placement) and systematic (recurring and related to specific materials). Defect reduction cuts across all manufacturing activities. Without defect reduction, yields will suffer and costs will be high. The major challenge for this technology is cost-effective, manufacturing-worthy measurement and analysis of defects extending down to 17 nm.

Modeling & Simulation focus areas are as follows:

- Equipment Modeling
- Feature-Scale Modeling
- Front End Process Modeling
- Lithography Modeling
- Topography Modeling
- Physical Device Modeling
- Circuit Element Modeling
- Packaging Modeling
- Simulation Environments
- Numerical Methods

Device, feature, and process modeling must become hierarchically integrated to empower the engineer using the system to get time- and cost-efficient answers. Modeling and simulation is the only tool available for engineers to design processes, material use, transistors, and structures; there is no viable alternative. The major challenge is getting predictive model results from atomic scale through electrical performance; to accurately model new technologies a priori resulting in development cost reduction; and faster time to market.

RESOURCES FOR ADDRESSING THE ROADMAP

The Roadmap Coordinating Group is hopeful that this 1997 edition of *The National Technology Roadmap for Semiconductors* will serve as a useful guide in the R&D investment decision processes. Ultimately, it is the level and direction of such funding decisions that will determine the future success of the semiconductor industry and, to a considerable extent, its customers in the pervasive range of industries dependent on high-performance, low-cost electronics.

Over the past 15 years, the semiconductor industry has increasingly sought to address its technology needs through precompetitive partnerships with government and academia. This is due in large measure to the increasing cost of developing solutions to the challenges associated with continuing to advance semiconductor technology. Members of the SIA have been instrumental in this process by establishing the Semiconductor Research Corporation (SRC) in 1982, SEMATECH in 1987, *The National Technology Roadmap for Semiconductors* in 1992, the International 300-mm Initiative (I300I) in 1996, and the Microelectronics Advanced Research Corporation (MARCO) in 1997.

Further, government support of research has been a major factor in the birth and rapid growth of the semiconductor industry. As a result, the United States is now a global leader in information technologies. These technologies have become a major component of the U.S. economy and are critical to defense programs. *Sustained government support of semiconductor research is mandatory if this industry is to continue to provide for strong economic growth in the U.S.*

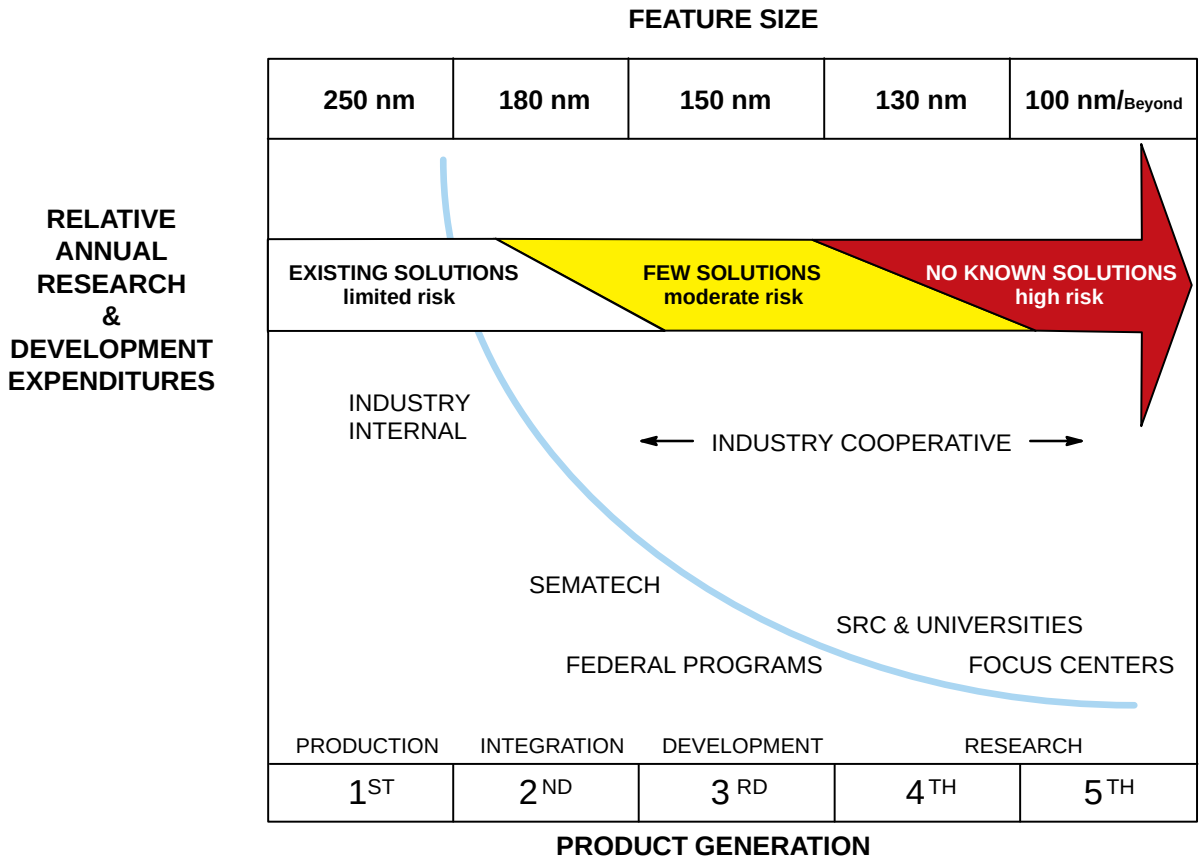


Figure 2 Present Day Commitment of Research and Development Expenditures

Figure 2 illustrates present day commitment of research and development expenditures to ensure future generations of semiconductor devices. The largest investments are made by individual companies as they prepare for their next generation of products. Additionally, significant resources are committed on a cooperative basis to meet the difficult challenges presented by future products two generations and more from present day practice.

As shown in the figure, each product generation represents increasing risk. This risk can be either related to the uncertainty of being able to develop manufacturing and design solutions for increasingly difficult technology nodes, or can result from a delay in technology development. In both cases, missed product opportunities will result in significant financial damage to the semiconductor industry and to the industries, including defense, that depend upon future generations of advanced integrated circuits.

Since the 1992 Roadmap, both the SRC and SEMATECH have aligned their organizations and programs to address the R&D needs of the Roadmap. In addition, some government agencies and laboratories have also used it to guide their research investments.

More recently, the SIA, in collaboration with SEMI/SEMATECH and the Department of Defense, has created a new university-based Focus Center research program to address some of the most difficult technology challenges that will be encountered soon after the turn of the century. This program will be managed by MARCO.

Each of the above organizations plays a unique, but coordinated, role in addressing the precompetitive research and development needs identified in the roadmap. Their activities are tailored to span the entire R&D spectrum ranging from the integration of new tools and processes to advanced exploratory research. Figure 2 illustrates the approximate focal point of their respective efforts in relation to this R&D spectrum.

However, in addition to the above programs, more research and development will be required in the future. A recently conducted analysis by the RCG and the SRC in collaboration with SEMATECH has identified serious gaps in research funding. Moreover, the 1997 Roadmap will highlight further challenges that must be addressed if the semiconductor industry is to remain on the historic productivity path that has contributed to the industry's success and to the security and economic success of the nation.

The SIA Roadmap Coordinating Group and the Technology Working Groups will remain active in identifying and developing the programs necessary for the semiconductor industry's future success. Further, these organizations stand ready to work with others that share their vision and who will benefit from mutual successes.

THE GRAND CHALLENGES

The U.S. semiconductor community faces increasingly difficult challenges as it moves into production at feature sizes approaching 100 nm. Some of these challenges span the entire spectrum of technology and will require major initiatives to develop solutions. Other challenges emerge as the industry is forced to seek solutions using approaches that have no historical precedent. The magnitude of these challenges demand special attention of the leadership from the semiconductor community. For this reason, they are highlighted in this section as Grand Challenges.

THE GRAND CHALLENGES

THE ABILITY TO CONTINUE AFFORDABLE SCALING

AFFORDABLE LITHOGRAPHY AT AND BELOW 100 nm

NEW MATERIALS AND STRUCTURES

GHz FREQUENCY OPERATION ON- AND OFF-CHIP

METROLOGY AND TEST

THE RESEARCH AND DEVELOPMENT CHALLENGE

AFFORDABLE SCALING

The semiconductor industry has maintained its growth by achieving a 25–30% per-year cost reduction per function throughout its history. This productivity growth in integrated circuits came through design innovation, device shrinks, wafer size increases, yield improvement, and equipment utilization improvements. However, some of the historical contributions to increased performance are no longer available. For example, yields today are quite high, precluding appreciable contributions to productivity increases through yield increases. The largest contribution to productivity growth continues to be decreased feature size. This scaling not only increases the number of transistors per square centimeter in an integrated circuit but also increases the speed of the circuits.

A second complicating factor is that the complexity of the circuits, and the resulting manufacturing complexity, is escalating as feature sizes decrease. Today's high-end microprocessors require six levels of interconnect. Continuing to use the materials' technologies and design approaches of the past will increase the number of levels of interconnect from 6 at 250 nm to 14, with some levels at feature sizes of 100 nm. New materials, new technologies, and new approaches *must* be invented. Affordable scaling and these required inventions constitute the Grand Challenges.

AFFORDABLE LITHOGRAPHY AT AND BELOW 100 nm

Ever since the invention of the integrated circuit, patterning had been achieved by lithographic techniques that use visible light. With the relentless decrease in feature size required for the productivity increases necessary to follow Moore's Law, lithography sources have progressed to ever shorter wavelengths, leading to today's exposure tools based on deep ultraviolet light (193 nm). While innovative technological approaches have enabled the industry to manufacture ICs with feature sizes significantly smaller than the wavelength of the exposure light, 193 nm technology will reach physical limits as feature sizes approach 100 nm.

Since no materials exist that are optically transparent at wavelengths significantly shorter than 193 nm, through-the-lens exposure tools cannot be advanced to shorter wavelengths. A completely different approach will be required for patterning as feature sizes approach 100 nm. Furthermore, the solution will require more than simply developing an exposure tool capable of meeting the industry

requirements; it will require a complete infrastructure of resists; masks; mask writing, inspection, and repair tools; and associated systems. Although various options are being explored, no clear path to the future has been identified.

NEW MATERIALS AND STRUCTURES

Analogous to the breakthroughs required to implement a fundamentally new approach to lithography as feature sizes decrease below 100 nm, the industry must develop new gate dielectric and gate electrode materials and processes to replace thermal SiO_2 and polysilicon as the gate stack, as well as interconnect materials and processes to replace the metal, dielectric, and contact materials. These manufacturing processes have served the industry since its inception. Manufacturing and integrating transistors with sub-100 nm gate lengths will be challenged by issues ranging from transistor physics to the incorporation of analog, memory, and logic within a single device. Copper is being developed for interconnect to replace aluminum, and new low dielectric constant (κ) materials must be developed to replace silicon dioxide in interlayer dielectrics. The use of copper will require the development of diffusion barrier materials and processing approaches.

As the device size continues to shrink, the thickness of the gate oxide must also decrease. Scaling and control of threshold voltage will be difficult due to statistical variation of the dopant atoms in the channel region. New approaches must be developed to ensure threshold voltage control.

Additionally, new higher dielectric constant materials or new approaches to creating the gate dielectric must be developed to reduce the tunneling currents in oxides grown by conventional techniques as the oxide thickness approaches 2 nm and below. Transistor performance requirements will demand replacement of polysilicon gates with high conductivity gates having low or no depletion, such as metal gates. The ultra-shallow source/drain extension affects transistor electrical parameters, such as drain-induced barrier lowering and effective gate length control that also impact threshold voltage and off current.

As currently envisioned, implementation of low κ interlayer insulators and contact materials through the 100 nm technology generation will require introducing groups of new materials with each new technology generation. Introduction of new materials into silicon integrated circuit manufacturing at this rate is unprecedented in the history of the industry. As shown by Figure 3, even though the use of copper and low κ materials reduces the number of levels of interconnect required and thus reduces manufacturing complexity, this approach will extend the improved performance for only a few technology generations. Technology generations beyond 100 nm will either require materials beyond conventional metals and dielectrics or conceptually new approaches to interconnect.

Comparable materials challenges will be faced in assembly and packaging. For continued improvement in off-chip performance, packaging technology must scale with silicon scaling. It does not scale with silicon scaling today, and such scaling will require new packaging materials and fabrication techniques. Low κ materials similar to those used in IC interconnects must be developed for packaging to ensure that performance gains on chip are available in the packaged assembly. Eventually, new interconnect approaches will have to replace the traditional multi-layer metal (MLM) solution.

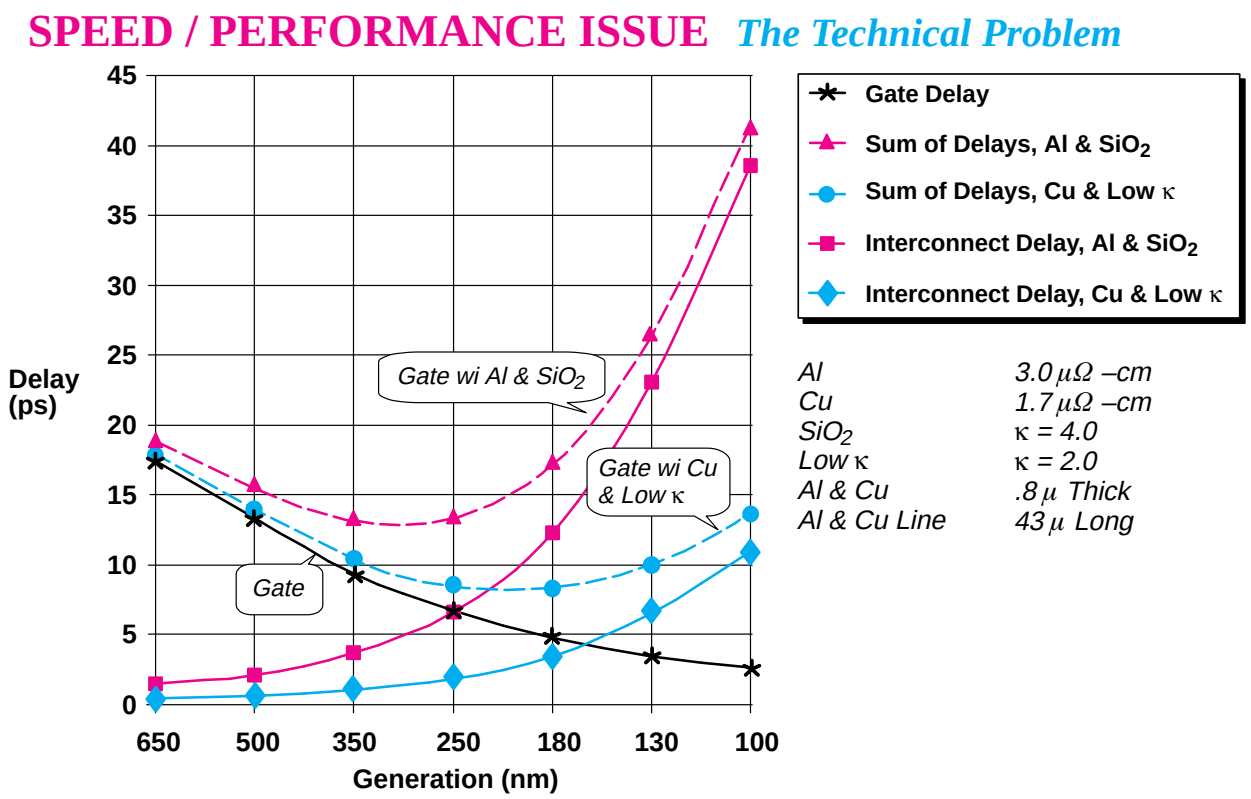


Figure 3 Calculated Gate and Interconnect Delay versus Technology Generation

Calculated gate and interconnect delay versus technology generation illustrating the dominance of interconnect delay over gate delay for aluminum metallization and silicon dioxide dielectrics as feature sizes approach 100 nm. Also shown is the decrease in interconnect delay and improved overall performance expected for copper and low κ dielectric constant insulators. [1]

GHz Frequency Operation on- and off-chip

Device and circuit speeds using extensions of today's chip and system architecture will soon reach fundamental limits. In the GHz frequency regime, circuit elements can no longer be treated as discrete, and transmission line approaches will be increasingly required. For example, electromagnetic signals require 0.1 nanoseconds to travel 3 centimeters (cm) in vacuum and will take longer in any medium with a dielectric constant greater than one. In addition, at frequencies of 10 GHz, the wavelength of 3 cm is comparable to the chip size.

Even for today's high-performance microprocessors, full chip performance cannot be achieved in packaged parts after assembly because of limitations of current packaging technology. The challenge of getting signals in the GHz frequency range off-chip and into the system after packaging is perhaps even greater than the challenge of on-chip performance at this frequency.

New approaches for system and chip architectures will be required. New circuit design and algorithms that circumvent parasitic limitations, along with assembly and packaging approaches, will be needed at these high frequencies. Solutions will require approaching the overall system as a unit rather than treating design, integrated circuit, and packaging as separate entities.

Metrology and Test

With the increasingly smaller dimensions and the need for greater purity, metrology faces major difficulties. Of seven compelling metrology issues, no known solution exists for one need today, for two

1. Bohr, Mark T. "Interconnect Scaling—The Real Limiter to High Performance ULSI." *Proceedings of the 1995 IEEE International Electron Devices Meeting*, 1995, pages 241–242.

starting at the 180 nm node, for three at the 130 nm node, and for six at the 70 nm node. Metrology requirements for lithography are equally forbidding. It may no longer be possible to rely on deterministic measurements virtually across the board. Practical solutions may require the use of statistical metrology (including statistical specifications) instead. If this is the ultimate solution, re-education of the industry to accept and trust such a change will be required.

Scanning probe methods can resolve smaller features, but present-day implementations are not well suited to online use. Much must be done to provide accuracy in scanning probe metrology commensurate with its resolution. Thickness measurements of gate insulators are becoming increasingly uncertain. The composition of real films is graded, with transition regions between film and substrate of a thickness approaching that of the film itself. Solutions to both of these difficulties are not clearly visible.

Detection of surface contaminants, already difficult, will require significant advances. The nature and sources of such improvements are not evident. The size of particles that can cause fatal defects is projected to decrease to 15 nm on patterned wafers. Optical methods cannot find such particles on bare wafers, let alone on patterned ones. Electron beam methods are too slow at present. Tools for detection of metallic impurities on surfaces are pressed to their limits with today's requirements, and further reductions in allowable surface metals are projected.

Product testing has been a concern for several years. Many chips cannot be tested exhaustively now, and it is not clear how the more complex chips of future generations will be tested. Affordable, sensitive, and accurate methods are required; incomplete testing combined with the use of statistical approaches may offer the only cost-effective potential solution known today. Predictive reliability tests are sought, since after-the-fact life testing is not accurate, timely, or affordable.

THE RESEARCH AND DEVELOPMENT CHALLENGE

Throughout the history of the integrated circuit industry, much of the equipment and processing research for future manufacturing technology was performed in large, vertically integrated companies in the semiconductor industry. These companies relied on the revenues from systems sales to fund the basic materials and processing technology research, as well as the device research, required to continue to advance the technology according to Moore's Law. The extensive effort and infrastructure required to reduce research concepts to practice was also frequently provided by these vertically integrated companies. To a large extent, the industry is still living off the benefits of its past research and development.

Intense international competition drove the stratification of the U.S. semiconductor industry into supplier and device manufacturing sectors. This stratification, along with intense competition, resulted in major changes in the nature and focus of the central research labs and a significant decrease in the amount of basic semiconductor research and technology. With the change of the industry in the U.S., approaches must be found to provide adequate, long-term research to replace the loss of the extensive in-house equipment and processing research in those central research labs of large, vertically integrated companies. Also, a new paradigm must be found to provide adequate research and development for new concepts that will be needed as well as the infrastructure to reduce the research concepts to practice.

The research and development needs and manufacturing costs for each technology area appear to increase as feature sizes decrease when each area is addressed independently. If this is the case, stand-alone solutions may neither be affordable nor manageable in the future. A different approach may be required in which the entire process, from design through manufacture, packaging, and test, is treated as a unit to provide a systems solution.

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

OVERVIEW

The Overall Roadmap Technology Characteristics tables provide a concise summary of the key technology metrics. The dates on the tables assume the year of first product shipment of integrated circuits (ICs) from a manufacturing site with a volume exceeding 10,000 units.

The ORTC tables were created early in the process and were used as the basis for the activities of each Technology Working Group in producing the individual roadmaps. The ORTC tables were also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the Technology Working Groups by highlighting any inconsistency among the specific roadmaps. As a result, the ORTC tables went through several revisions until the Roadmap document was completed. The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group section. Appendix B presents the ORTC glossary.

ROADMAP TIMELINE ACCELERATION

The pace at which technology generations are introduced has accelerated since the publication of the 1994 Roadmap. Fueled by the continuing explosive growth of the semiconductor market, the introduction of new technologies has been accelerated by leading semiconductor companies from the traditional 3-year cycle towards an approximate 2-year cycle. On the average, the introduction of each technology generation has been pulled in by one year with respect to the 1994 Roadmap. This is clearly demonstrated by products built with the 250 nm technology generation that are shipping in 1997 as opposed to the previous prediction of first shipments in 1998. In addition, the introduction into the market place of the 180 nm technology generation, which was previously predicted to occur in the year 2001, it is now forecast to occur in the year 1999. To reflect this technology trend, the granularity of the ORTC tables has been increased to reflect a 2-year cycle for the introduction of the next four technology generations (250 nm, 180 nm, 150 nm, and 130 nm).

The ability of optical lithography to lead the industry to and beyond the 100 nm technology generation timeframe is being challenged by a variety of alternative imaging technologies. Consequently, to reflect an increased level of uncertainty that occurs whenever major technology transitions are anticipated, the initial 3-year Roadmap renewal cycle has been reinstated for the introduction of the 100 nm technology generation and beyond.

It should be observed that the ORTC metrics, which guide the Roadmap, are used by the leading semiconductor companies as a set of targets that needs to be achieved ahead of schedule to maintain a position among the industry leaders. As a result, the ORTC metrics need to be realistic but aggressive in nature to provide valuable targets for the semiconductor industry. The above considerations indicate that the intrinsically highly competitive environment of the semiconductor industry will make many portions of the ORTC metrics, and consequently the Roadmap, inaccurate and obsolete within two to three years from its publication. While the fast obsolescence of the Roadmap represents a measure of its success, it also emphasizes the need for more frequent updates.

BACKGROUND

TECHNOLOGY GENERATIONS ROADMAP

Historically DRAM products have been recognized as the technology drivers for the whole semiconductor industry. Prior to the early '90s logic (microprocessor) technology was developed at a slower pace

than DRAM technology. In the last few years, the development rate of new technologies used to manufacture microprocessors (MPUs) has accelerated. Microprocessor products have now closed the technology gap with DRAM. It is now recognized that DRAM and microprocessor products share the technology leadership role.

Several fundamental differences exist between the two families of products. Development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch. Conversely, microprocessor performance is dominated by the length of the transistor gate and by the number of interconnect layers. As a result, Table 1 shows both MPU gate length and DRAM half-pitch features.

Table 1 Technology Generations

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Memory							
Generation @ samples/introduction	256M	1G	*	4G	16G	64G	256G
Generation @ production ramp	64M	256M	1G	1G	4G	16G	64G
Bits/cm^2 @ sample/introduction	96M	270M	380M*	770M	2.2B	6.1B	17B
Logic (high-volume, cost-performance: MPU)†							
Logic transistors/cm^2 (packed, including on-chip SRAM)	3.7M	6.2M	10M	18M	39M	84M	180M
*Logic (low-volume: ASIC)***‡							
Usable transistors/cm^2 (auto layout)	8M	14M	16M	24M	40M	64M	100M

* *Generation is for trend purposes only*
** *ASIC—application-specific integrated circuit*
† *Year 1 data will be less dense than subsequent shrinks*
‡ *Refers to high-performance, leading-edge, embedded-array ASICs*

For each technology generation both the leading-edge and the high-volume DRAM products are indicated. In addition, a new 150 nm technology generation has been introduced. At present exposure tools using 248 nm wavelength are used in the development of 180 nm technology. It is expected that the transition from the 180 nm technology generation to the 150 nm technology generation will occur in 2001. Several companies have stated that the availability in volume of exposure tools using 193 nm exposure wavelength will allow this transition to occur quickly by using the 180 nm technology as a baseline and by replacing 248 nm exposure tools with 193 nm exposure tools on several mask layers. Further improvements in the resolution and alignment capability of these tools will lead to the subsequent transition to 130 nm in 2003. It is anticipated that non-optical exposure techniques may become viable contenders to optical lithography with the advent of the 100 nm technology generation.

In comparing the 1997 Roadmap with the 1994 Roadmap, it should be noted that the average annualized reduction rate in feature size has remained unchanged at approximately 10.5%/year even though this rate has accelerated to 15.5%/year in the time interval 1995–1999. The overall schedule for introduction of a new technology generation has been accelerated by one year.

CHIP SIZE

Despite the continuous reduction in feature size of about 30% every three years, due to advances in patterning technology, the chip size at the time of introduction of DRAM has continued to increase by about 12%/year. This increase in chip area is necessary to accommodate 59% more bits/year in accordance with Moore's Law, as shown in Table 2. However, to maintain the historical trend of reducing

cost/function by 25–30%/year it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, and, most of all, increase the number of chips available on a wafer. The increase in the gross number of chips available on a wafer is primarily obtained by reducing the area of the chip by means of a combination of smaller feature size (shrink) and product redesign (compaction). For instance it is forecast that the chip area of a cost-effective product must be reduced to approximately 50% and 35% of the initial chip area at time of introduction within three years and six years, respectively.

To improve productivity it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is determined by the field size of the lithographic tool. The roadmap for this useful parameter is included in Table 2.

Table 2 Chip Size

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Functions/Chip							
DRAM bits/chip—Years 1–6	267M	1.07G	1.7G*	4.29G	17.2G	68.7G	275G
Microprocessor total transistors/chip—Years 1–6	11M	21M	40M	76M	200M	520M	1.40B
Chip size (mm^2)							
DRAM—Year 1	280	400	445*	560	790	1120	1580
DRAM—Year 3 (2^{nd} shrink)	170	240	270*	340	480	670	950
DRAM—Year 6 (2^{nd} cut-down-next gen.)	100	140	160*	200	280	390	550
MPU—Year 1	300	340	385	430	520	620	750
MPU—Year 3 (2^{nd} shrink)	180	205	230	260	310	370	450
MPU—Year 6 (2^{nd} cut-down-next gen.)	110	125	140	150	180	220	260
ASIC (Max litho field area)	480	800	850	900	1000	1100	1300
Lithographic field size (mm^2)	22 × 22 484	25 × 32 800	25 × 34 850	25 × 36 900	25 × 40 1000	25 × 44 1100	25 × 52 1300
Maximum Substrate Diameter (mm)							
Bulk or epitaxial or SOI** Wafer	200	300	300	300	300	450	450

** Generation is for trend purposes only*
*** SOI—silicon on insulator*

Historically, another major productivity increase has resulted from the conversion to wafer size of progressively larger diameter. It is anticipated that conversion to 300 mm diameter wafers will commence production ramp in 1999. It is projected that the number of available chips will increase by a factor of 2.4–2.5 on a 300 mm wafer compared to the number of chips available on a 200 mm wafer. To realize a similar gain in the number of available chips, it is forecast that the next wafer size will need to be 450 mm in diameter.

PERFORMANCE OF PACKAGED CHIPS

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or memory cells for each technology generation. Consequently, the number of pins/balls necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. Refer to Table 3.

Table 3 Performance of Packaged Chips

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Number of Chip I/Os							
Chip-to-package (pads) high-performance	1450	2000	2400	3000	4000	5400	7300
Chip-to-package (pads) cost-performance	800	975	1195	1460	1970	2655	3585
Number of Package Pins/Balls							
ASIC (high-performance)	1100	1500	1800	2200	3000	4100	5500
MPU/controller, cost-performance	600	810	900	1100	1500	2000	2700
Cost-performance package cost (cents/pin)	1.40–2.80	1.25–2.50	1.15–2.30	1.05–2.05	0.90–1.75	0.75–1.50	0.65–1.30
Chip Frequency (MHz)							
On-chip local clock, high-performance	750	1250	1500	2100	3500	6000	10000
On-chip, across-chip clock, high-performance	750	1200	1400	1600	2000	2500	3000
On-chip, across-chip clock, cost-performance	400	600	700	800	1100	1400	1800
On-chip, across-chip clock, high-performance ASIC	300	500	600	700	900	1200	1500
Chip-to-board (off-chip) speed, high-performance (Reduced-width, multiplexed bus)	750	1200	1400	1600	2000	2500	3000
Chip-to-board (off-chip) peripheral buses	250	480	785	885	1035	1285	1540
Maximum number wiring levels	6	6–7	7	7	7–8	8–9	9

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will grow at an annual rate of approximately 11%. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions. Nevertheless, the cost/pin is forecast to decrease at a rate of 5%/year.

The insatiable market demand for higher performance cost-effective products creates the need for processing electrical signals at a progressively higher rate. The need for a progressively higher operational frequency associated with an increasing average chip size requires the development of novel process, design, and packaging techniques.

These considerations are reflected in the multiple categories in which frequency trends are reported. The highest frequency obtainable in each technology generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between the value of this "local" frequency and the value of the frequency of signals traveling across the chip (across-chip clock) becomes progressively larger due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package.

To optimize signal and power distribution across the chip it is expected that the number of layers of interconnections will continue to increase. As scaling of interconnections will continue, it is projected that use of a lower resistivity metal (copper) and that replacement of silicon dioxide (κ~4) with various insulating materials of progressively lower dielectric constant (κ~2–3) will be adopted in the chip fabrication process. Use of copper will reduce degradation of signal propagation delay time due to voltage drop on power lines. Use of low κ dielectric will decrease the degradation of signal propagation delay time by reducing capacitive coupling. Multiplexing techniques will be used to increase the chip-to-board operating frequency (off-chip).

ELECTRICAL DEFECT DENSITY

The targets for electrical defect density of DRAM, MPU, and ASIC necessary to achieve 60% chip yield in the year of introduction are shown in Table 4.

Table 4 Electrical Defects

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
DRAM first year electrical D_0 * @ 60% yield/3rd year @ 80% yield (d/m^2)	2080/1390	1455/985	1310**/875**	1040/695	735/490	520/350	370/250
MPU First Year Electrical D_0 @ 60% yield/3rd year @ 80% yield (d/m^2)	1940/1310	1710/1150	1510**/1025**	1355/910	1120/760	940/640	775/525
ASIC first year electrical D_0 @ 60% yield (d/m^2)	1210	725	685**	645	580	530	450
Minimum mask count	22	22/24	23	24	24/26	26/28	28

** D_0—electrical defect density*
*** Generation is for trend purposes only*

The allowable number of defects is calculated by taking into account the different chip sizes reported in Table 2 for DRAM and microprocessors. The maximum chip area of ASIC products is assumed equal to the maximum available field size of the exposure tool. In addition, the reduced number of defects required to achieve 80% yield in the third year of manufacturing has been calculated using the corresponding chip sizes. The approximate number of masks for logic devices is reported as an indicator of the ever increasing process complexity.

POWER SUPPLY VOLTAGE AND POWER DISSIPATION

Reduction of power supply voltage is driven by several factors—reliability of gate oxides, reduction of power dissipation, and reduced transistor channel length. The way in which the value of the power supply voltage is represented in the 1997 Roadmap is quite different from the approach taken in the 1994 Roadmap. As seen in Table 5 the value of the power supply voltage is now given as a range.

Table 5 Power Supply and Power Dissipation

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)	1.8–2.5	1.5–1.8	1.2–1.5	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6
Maximum Power							
High-performance with heat sink (W)	70	90	110	130	160	170	175
Battery (W)—(Hand-held)	1.2	1.4	1.7	2	2.4	2.8	3.2

Selection of a specific V_{dd} value has become part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each technology generation. In the 1994 Roadmap edition, the power supply voltage was regarded as a single standard with a limit of 0.9 volts. Values of V_{dd} as low as 0.5 volts are now considered viable.

Maximum power has been divided in the two following categories: 1) high-performance desktop applications, for which a heat sink on the package is permitted and 2) portable battery operations. In both cases, total power consumption will increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher operating frequency, higher overall capacitance, and larger chip size.

COST

Table 6 is dedicated to cost trends. The ability to reduce the cost per function by an average 25–30% each year represents one of the unique features of the semiconductor industry. Despite the continuously increasing amount of investment needed in research and development in conjunction with the escalating cost of building and equipping a manufacturing plant, the ability to deliver four times as many memory cells in approximately three years with only a moderate ($< 1.5\times$) increase in chip size constitutes the foundation on which the growth of the semiconductor industry is built. To continue to support this growth, it is necessary to assess, on the basis of the above boundary conditions, an affordable cost/bit and an affordable cost/transistor for DRAM and microprocessors, respectively. These cost targets, together with the technical targets, must guide the activity of the engineering community in planning and executing each technology program. Table 6 shows that DRAM suppliers, to limit the maximum average selling price (ASP) increase per generation to 41%, must decrease the cost/bit at an average rate of 29%/year.[2]

Extrapolation of historical trend data indicates an introductory affordable cost/bit of approximately 120 microcents for the 256 Mbit DRAM. In addition, the historical trends indicate that within a DRAM generation a 45%/year reduction in cost/bit should be expected.[3] A similar analysis conducted from published data for microprocessors yields similar results.[4] In this case a 24%/year reduction in cost/transistor from generation to generation and a 45%/year reduction rate within the same generation are projected. A somewhat slower cost decline is observed beyond the fourth year (three years) from introduction. The above cost reduction targets for DRAM and microprocessors are consistent with the overall cost reduction trend discussed at the beginning of this paragraph.

As the number of functions/chip continues to increase it becomes increasingly difficult and therefore costly to test the final products. This is reflected in the escalating cost of testers (cost/pin is flat while the number of pins grows at 10.5%/year) indicated in Table 6. It is anticipated that implementation of Built-In-Self-Test (BIST) and Design-For-Testability (DFT) techniques will need to accelerate within the time frame of the 1997 Roadmap.

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2. Staff writer. "Ten Year Commemorative Report: LSI Technology for the Year 2010." *Nikkei Microdevices Magazine*, July 1, 1995, page 115.

3. McClean, William J., ed. Mid-Term 1994: *Status and Forecast of the IC Industry.* Scottsdale: Integrated Circuit Engineering Corporation, 1994.
   McClean, William J., ed. Mid-Term 1995: *Status and Forecast of the IC Industry.* Scottsdale: Integrated Circuit Engineering Corporation, 1995.

4. a) Dataquest Incorporated. *x86 Market: Detailed Forecast, Assumptions, and Trends*. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.
   b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. *Business Week*, December 9, 1996, 148–152.

Table 6 Cost

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF-PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
"Affordable" Packaged Unit Cost/Function (Microcents/Function)							
DRAM packaged unit cost/bit @ (microcents)—Year 1	120	60	30*	15	5.3	1.9	0.66
DRAM packaged unit cost/bit @ (microcents)—Year 3 [2nd shrink]	36	18	9*	4.5	1.6	0.57	0.2
DRAM packaged unit cost/bit @ (microcents)—Year 6 [2nd cut-down—next gen.]	6	3	1.5*	0.76	0.28	0.09	0.03
Microprocessor packaged unit cost/transistor @ (microcents)—Year 1	3000	1735	1000	580	255	110	49
Microprocessor packaged unit cost/transistor @ (microcents)—Year 3 [2nd shrink]	910	525	305	175	75	34	15
Microprocessor packaged unit cost/transistor @ (microcents)—Year 6 [2nd cut-down—next gen.	290	167	97	56	24	11	4.7
Cost-performance package cost (cents/pin)	1.40–2.80	1.25–2.50	1.15–2.30	1.05–2.05	0.90–1.75	0.75–1.50	0.65–1.30
Logic (Low-Volume: ASIC)							
Nonrecurring engineering cost/usable transistor (microcents)	50	25	20	15	10	5	2.5
Design and Test							
Volume tester cost/pin ($K/pin), high-performance	10	10	10	10	10	10	10
Volume tester cost/pin ($K/pin), cost-performance	3	3	3	3	3	3	3

** Generation is for trend purposes only*

The Technology Roadmaps

Focus Technology Working Groups

DESIGN & TEST

SCOPE

Today's integrated circuits are massive arrays of transistors communicating through a complex pattern of interconnects to implement a function of value to some customer. The *Design & Test* section covers designing, verifying, and testing these individual element's patterns using the constraints provided by the individual transistor characteristics and the limitations of the physical wiring. The complexity of these arrays increases exponentially with time because of the underlying wafer technology and historical trends. The difficulty of the design and test tasks is accelerated and represents a limit on the ability to obtain full value from fabrication technology. Additionally, design and test will play an increasingly important role in determining the overall success of the semiconductor industry. Tables 7 and 8 highlight the Difficult Challenges and the Technology Requirements to be addressed to meet continued success.

Table 7 Design & Test Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Design environment and standards, design data models, and access supporting incremental processing	Increased design data Increased design iterations Increased design teams Geographically distributed teams
More accurate interconnect and power models for synthesis/ system level design	Modeling methodology defining guidelines for model development for different system components
Constraint-dominated interconnect synthesis	Gigascale designs will be dominated by interconnect Automatic synthesis and optimization of N-layer interconnects for performance
Verification becomes dominant effort in design	Timing verification System-level formal verification/specification Core-based designs
Eliminate negative yield impact due to tester timing limits	Limitations of test equipment
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Dramatically improved design productivity to deal with increasing complexity	Design effort (transistor/man-year) and design and test cycle times, design quality
Power management impact at all levels	Hard constraint of power dissipation limitations of gigascale ICs
Architectural and other design methods to overcome fatal interconnect performance problems	Limitations of materials (copper/low κ) to overcome interconnect problems associated with high performance ICs
Signal integrity and IC reliability	Noise, interconnect, and reliability related issues
Automated synthesis/layout of analog/mixed signal designs	Difficulties in design and test of analog/mixed signal

DESIGN ROADMAP

TECHNOLOGY STATUS

Leading-edge product design complexity (as defined by number of transistors on a chip) has been increasing at a 58% compound annual growth rate (CAGR), enabled by improving processing and manufacturing technology. However, designer productivity improvement for processors has historically been 21% CAGR, producing a growing gap of designers needed for more complex designs resulting in a 30%/year CAGR.

Table 8 Design and Test Technology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Overall design Productivity	**21% CAGR**	**Improve 1997 CAGR by 5%**	**Improve 1997 CAGR by 10%**	**Improve 1997 CAGR by 15%**	**Improve 1997 CAGR by 20%**	**Improve 1997 CAGR by 2 5%**	**Improve 1997 CAGR by 30%**
Overall design cycle times (includes RF*, analog, mixed signals)	**Measured in months**	**20% reduction over 1997**	**25% reduction over 1997**	**35% reduction over 1997**	**45% reduction over 1997**	**50% reduction over 1997**	**55% reduction over 1997**
Overall ability of test/diagnostic (functional and at speed)	**Increase on chip test BIST/DFT*** **	**Standard test meth-odology for core based designs**	**Timing tests (at speed test) at core level**	**Timing tests (at speed test) at core level**	**Timing tests (at speed test)**	**Timing tests (at speed test)**	**Timing tests (at speed test)**
Enable design reuse methods for systems on a chip	**40% reuse**	**50% reuse**	**55% reuse**	**60% reuse**	**70% reuse**	**80% reuse**	**90% reuse**
Enable near-RF speeds of system on a chip design	**Increase accuracy with models and simulation**	**Couple synthesis and physical design**	**Couple synthesis and physical design**	**Novel architecture: asynchro-nous**	**Novel architec-tures**	**Novel architec-tures**	**Novel architec-tures**

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *RF—radio frequency*
** *BIST—built-in self test*
*** *DFT—design for testability*

The increasing design team size for the leading-edge product is not only costly, but reaches a limit of complexity of team interaction to a point of diminishing return. In addition, increasing globalization leads to the need for collaboration of geographically diverse teams. Teams in excess of 250 to 300 members are becoming inefficient and difficult to manage. Similar team limitations for large software development projects have been reported. The consensus among the semiconductor design technology working group members is that a crisis is approaching.

DESIGN PRODUCTIVITY

Design and test in the semiconductor industry of 1997 has made little substantial progress since the last Roadmap in 1994. It is imperative that research and industry targets be well defined to make the required progress into 2000. In many cases, system-level integration is already limited by existing design methodology and CAD tools because the designer cannot work smoothly up and down the levels of abstraction from device details to product functionality. The lead time for addressing these enormously complex, interdependent issues is long. Failure to quantify and address these issues in the near term will compromise the substantial investments being made in the other areas of the process development technologies. The decrease in design productivity will limit the historical rate of cost per function improvement. Design productivity must be increased significantly or the industry's ability to utilize advancements in manufacturing technology will decrease.

DESIGN AUTOMATION TOOLS

Lack of standards and interoperability greatly complicates design and simulation across the levels of abstraction. Specification of design objectives remains largely informal; performance and system environment parameters are communicated almost entirely on paper rather than through well-defined behavioral and timing models. Synthesis of designs is performed "bottom-up" using a mixture of manual methods, block-level logic synthesis tools, and semiautomatic layout. Verification is achieved by simulating the design at many disconnected levels of abstraction, ranging from behavioral through circuit level. Testability is not explicitly incorporated into most designs although the use of boundary scan and full scan techniques is becoming common in some classes of product. Built-in self-test (BIST) techniques are being investigated, but their actual use in delivered parts other than memory remains rare.

The most successful companies use highly refined design methodologies that depend heavily on vendor-supplied CAD tools, augmented by proprietary tools that provide added value to their product domain. Over the past few years, many of these companies have increased their internal investments in design technology simply because the design technology industry is not able to keep up. Many advanced companies believe that the electronic design automation (EDA) industry continues to fall further behind in understanding the nature of current design problems.

CIRCUIT TECHNOLOGY CHANGES

The dominant circuit design paradigm for mainstream digital very large scale integration (VLSI) is static CMOS logic. However, the growing trend towards system-on-a-chip (SOC) and the explosion of the communications market (especially wireless and data) dictates that an increasing fraction of designs incorporate some analog and perhaps RF functionality to interface to the external world. Even digital designs must often be approached with analog circuit techniques and analysis. Better understanding of the problem, increased investment, and improved coordination between user companies, universities, and the design technology suppliers is essential to provide the new sets of tools and techniques.

Finally, it is important to note a significant difference between the technology described in this section and those covered by the rest of the Roadmap. In the semiconductor manufacturing environment, progress tends to occur in discrete generations where all the technology elements need to be in place before a transition can be made to the next generation. In the design environment, incremental improvements in any part of the process are important and can produce immediate gains in productivity quality and cost independent of improvements in other design or manufacturing areas.

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

DESIGN ENVIRONMENT AND STANDARD INTERFACES

A semiconductor design must be developed, analyzed, and refined by a sequence of several different design tools used across a diverse design team in the shortest possible time and at the lowest possible cost. This requires that design information flow (or be shared) between design tools and individuals in a smooth and efficient manner. As chip density increases the amount of design information and the number of sources and users of that information will increase. This increase affects not only the processing time within a tool, but also the data transition time between tools.

Design needs are generally in the form of improvements to existing tools and techniques. Rapid increases in the complexity of designs (digital and analog/RF) and a collection of deep submicron (DSM) effects have changed the nature of the semiconductor design. These changes will soon require new approaches to the design process. This will result in profound changes in overall design methodology, and these changes will fundamentally alter the needs in design tools as well (Figure 4). Although improved design productivity will come predominantly from continuous improvements in computing platforms, better algorithms in the tools, and improved design methodologies, the design environment must be refined as well. This will require standardized access to design information by CAD tools, and

incremental and concurrent analysis of design changes (whereby processing time is a function of the size of the design change rather than the original design in total).

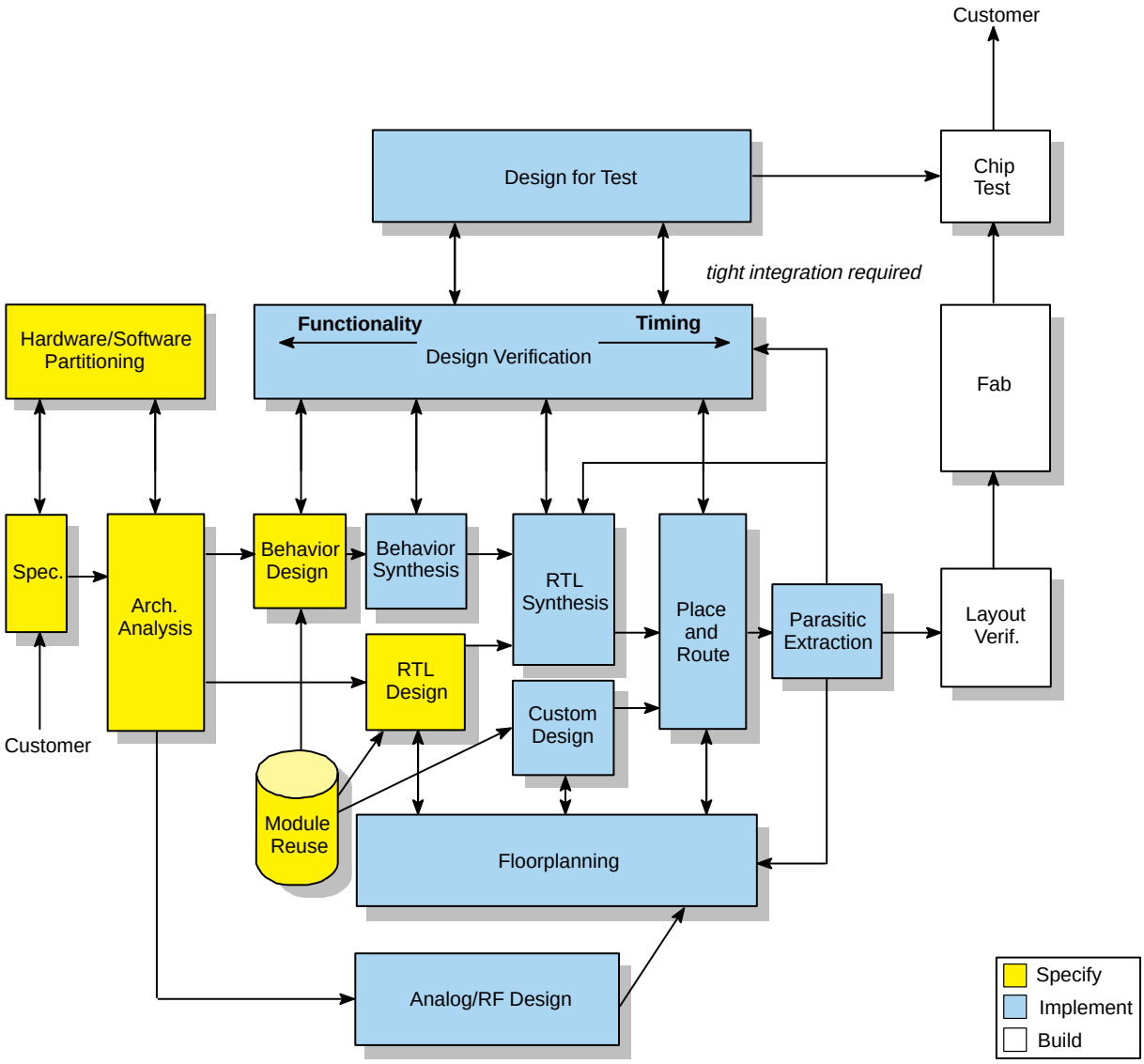


Figure 4 Overall Design and Test Flow

Shared access to design information must be extended to span the entire development process to facilitate concurrent design change and analysis. All levels of the hierarchy must be supported by a standard information model for all design elements.

Visualization and selection of candidate reusable “components” from various sources such as the Internet will also be important as on-chip reuse increases. An industry-wide dictionary of standard terminology for design information must be developed and be extensible for future requirements. Standard mechanisms to distribute designs across the Internet in an efficient and secure manner will be paramount.

The design information environment must include a database utilizing a common programming interface for all design information and usable by all enterprise tools. A solution must evolve starting with common access interfaces and formal approaches for mapping information between different representations and models; continue with research directed at common industry-wide information models; and

include research on large capacity Database Management Systems (DBMS) solutions for this design environment.

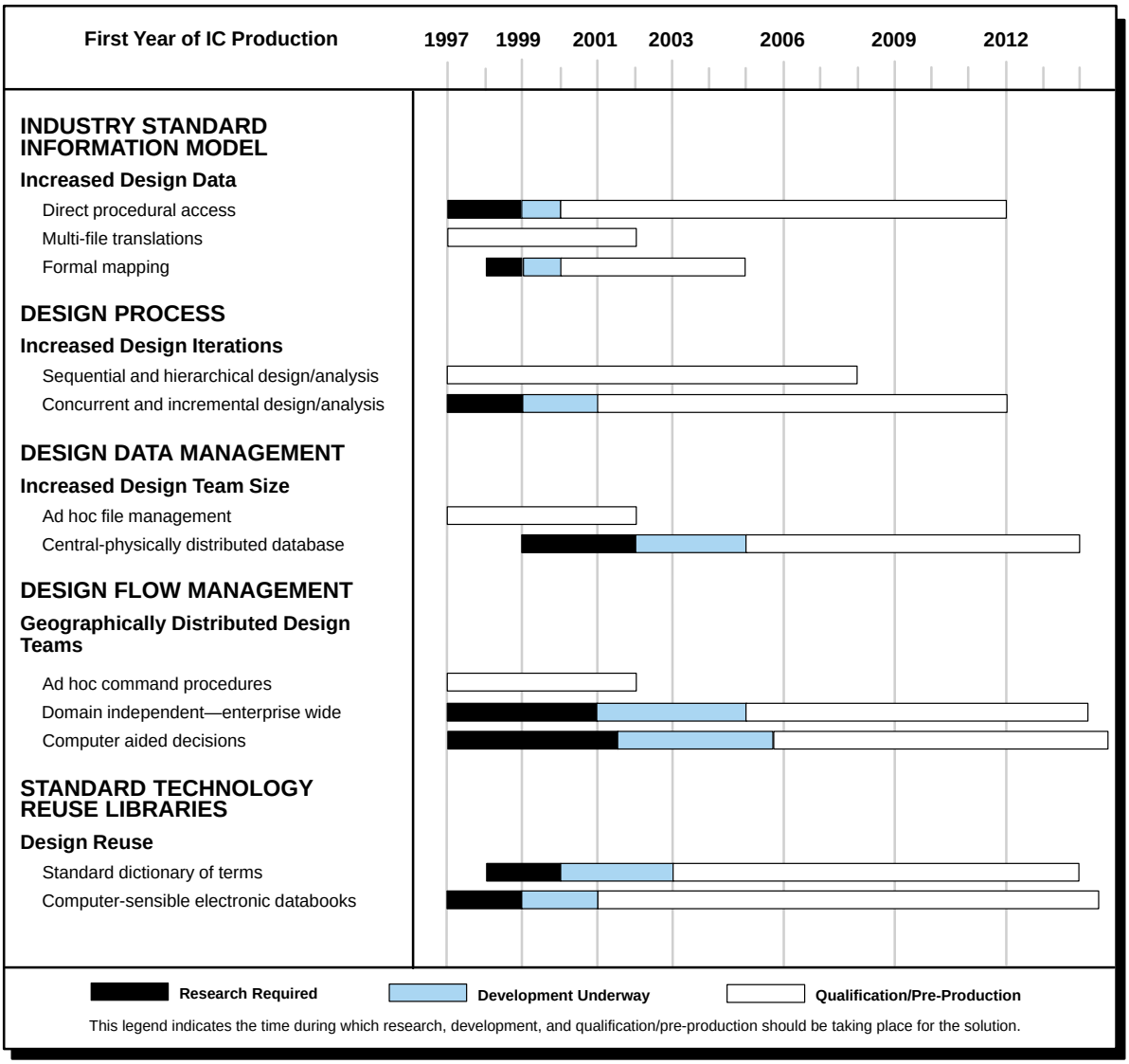


Figure 5 Design Environment and Standard Interfaces Potential Solutions

Larger, geographically distributed design teams who design full SOCs and reuse designs from multiple sources will dictate improvements in design data management and process management. With design complexity growing at its current rate, new solutions must be found to both the capacity and run-time bottlenecks of existing tools and design methodology. Distributing tools among multiple processors on a network can effect some overall performance improvement, but finer-grained approaches to exploiting concurrency in tools and algorithms is also a priority. The thread-based model of concurrency, implemented at the system level in many multiprocessing systems (including networks of workstations) and exported to users naturally in modern programming languages, must also be exploited more effectively by the design technology community to improve overall capacity and throughput.

DESIGN SYNTHESIS AND SYSTEM-LEVEL DESIGN

Improvements in wafer processing will have two different impacts on design synthesis. The exponential growth in the number of devices that can be implemented economically on a single chip will drive a greater integration between synthesis and system level design. The increasing complexity of the behavior of these devices and increasing dominance of circuit delay by interconnect will drive a greater integration between synthesis and physical design. One new important phenomenon in IC design is the appearance of the SOC. Typically, an SOC is not a single chip of application-specific logic but is naturally organized into a number of special purpose modules. These include microprocessors, peripherals, memory, and ASIC portions. The design of integrated circuits such as these requires an integration of system-level design, synthesis, and physical design.

The first requirement for designing an SOC is to have a single design specification that comprehends the entire design. This design specification must be executable and/or emulatable and forms the first functional description of the design against which all subsequent refinements of the design must be verified. Currently, executable system specifications are primarily used for analyzing the system properties of a design. This usage must be extended to link to implementation tools in both the hardware and software domain.

An SOC typically has a memory subsystem that contains compiled software. This reflects the fact that the system designer has made many decisions regarding the partitioning of system functionality into hardware and software. After the initial specification is obtained it is modified during architecture exploration and divided into software and hardware parts. Each partition is then analyzed by estimating critical quality metrics such as performance, power, cost, testability, and others. If the quality metric goals are not satisfied different architectures, partitions, or components may be selected. If no acceptable solution is found, the specification is modified by changing goals, constraints, and features. To aid in this process a number of different estimation tools are needed. The ability to take the system specification and estimate the speed, area, and power dissipation of a portion of the specification in either hardware or software is required. Based on these estimates the designer can then make an intelligent partitioning of the design. To accomplish this will require the development of improved estimation technology.

Once the partition into hardware and software has been made tools must exist that automatically generate both parts of the system. The tools for producing the software, such as C code, from the system specification are currently lacking. There must also be compilers, assemblers, and real time operating systems that enable the final implementation of the software. This technology is currently available but further improvements need to be made before it is applicable to embedded system design. In the case of custom processors improvements include design of instruction sets, custom assemblers and compilers, and possibly a custom real time operating system.

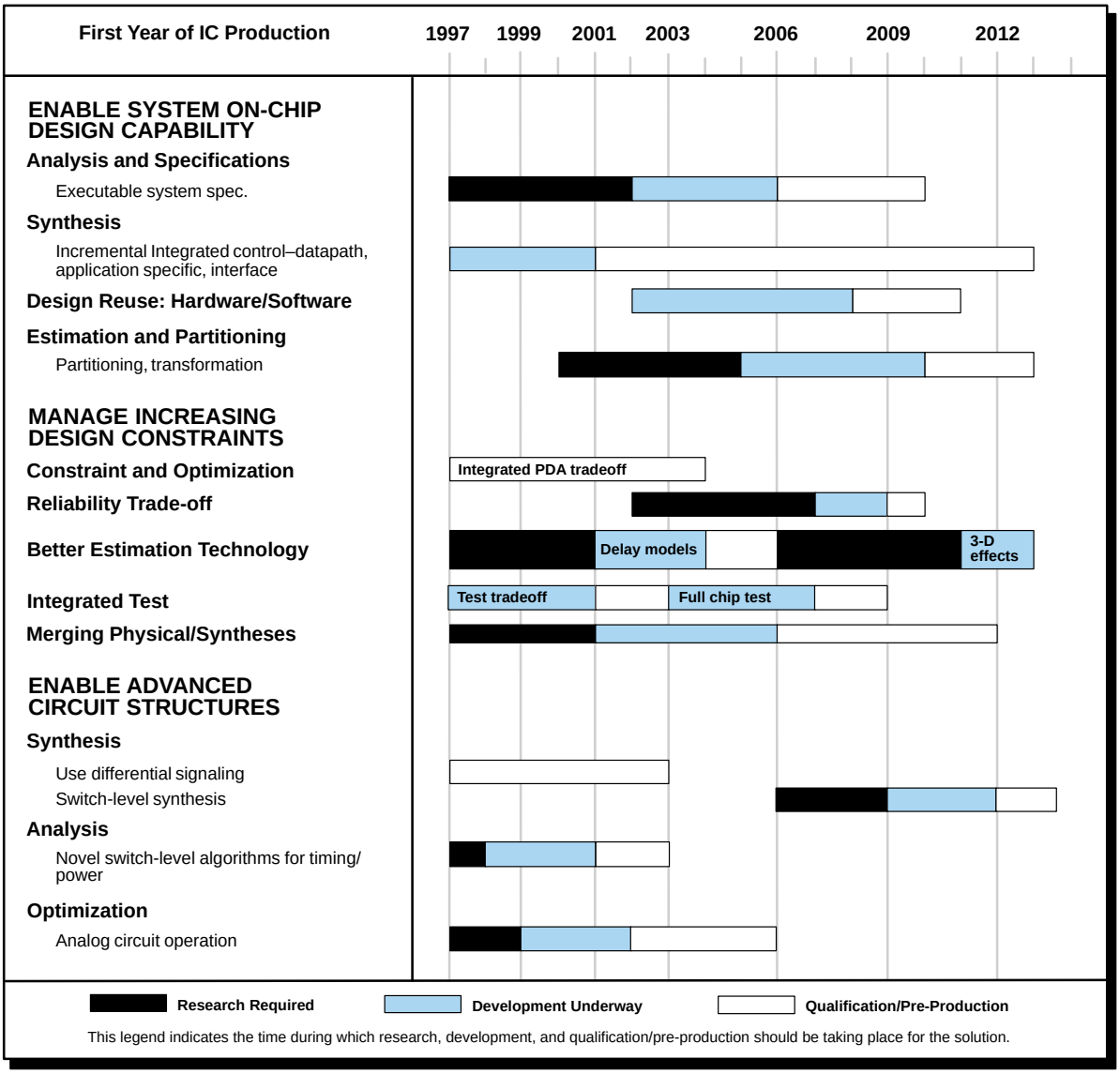


Figure 6 Design Synthesis and System-level Design Potential Solutions

There must also be tools that automatically generate hardware descriptions using languages, such as VHSIC (very high speed IC) hardware description language (VHDL) and Verilog®, from the system specification. Sophisticated design reuse is essential in designing an SOC based on a wide diversity of pre-designed building blocks. To be successful, the design of large blocks, such as microprocessors and microcontrollers, must be made easily portable from one SOC to another and there must be tool support to integrate diverse pre-designed blocks on a single chip. Synthesis plays a central role in re-implementation of design modules, and thus it is also key to design reusability.

Synthesis must evolve to comprehend the reuse of pre-designed blocks, with surrounding synthesized logic. Timing, power, area, test, and reliability tradeoffs must be considered within the context of the reused designs. Since large, pre-designed blocks are not easily portable across SOC designs, it is difficult to share or reuse them. Design reuse will have a major impact on synthesis, most notably new standards for description of systems and standard portable synthesis library formats. To enable new markets, existing techniques must evolve to a new design language environment such that large, portable pre-designed blocks can be developed and shared. These techniques must also support the design and verification of much larger systems (including embedded software). Even in a building

block-based approach, the number of devices expected on silicon within the next few years demands considerable attention for the inter-block communication and wiring expanded to multi-block and multi-chip levels. In a world of packageless chip interconnection schemes, with many thousands of pins per chip, attention to inter-chip partitioning and effective approaches to area-based inter-chip wiring floor planning and optimization are critical.

Having specified the system, partitioned it into hardware and software modules, and implemented such hardware and software, it is necessary to build the interface between the hardware and software. Interface synthesis consists of generating software to interface to hardware, and hardware to interface to software. To interface hardware and software that operate on different abstraction levels, the interface synthesis defines first the bus and communication protocols from which software and hardware components are synthesized.

There are several barriers to productivity gains at the system level that should be addressed, as follows:

- Modeling methodology that defines guidelines for the development of models for different system components and how to integrate them for virtual prototyping or emulation
- Characterization and development of reusable software and hardware components
- Specification and system description languages, methods for capturing requirements and converting these into specifications, and then into simulatable or emulatable models
- Methods for software and hardware synthesis from system level specifications
- System-level modeling tools linked through module generators and synthesis tools to the final implementation.

For hardware these tools must use contemporary module generators, behavioral synthesis, and logic synthesis tools as targets like logic synthesis tools currently use physical design tools as a target. For software these tools must actually use contemporary compiler tools as a target like compiler tools currently use assemblers and linkers as a target.

PHYSICAL DESIGN

Physical design deals with aspects of chip implementation related to the spatial layout of devices and interconnects. In the past, the primary physical design objective was to arrange devices and interconnects to achieve minimum-area layout. In the future, physical design must trade off area against competing measures of design quality—speed, power, signal integrity, and manufacturing yield. This change is ultimately due to the different scaling of devices and interconnects. With successive process generations, devices are smaller; have less drive strength; and are more noise-sensitive. Interconnects are more resistive; have greater coupling capacitance; and traverse larger chip sizes; and thus become the key to chip performance.

As the physical design solution increasingly determines overall design quality, there will be a need for far more accurate models of device/interconnect interactions. For example, for the 250 nm generation, the topology of global interconnects must be modeled accurately during chip planning; for the 180 nm generation, the additional factor of the dynamic capacitive coupling of interconnects must be accurately modeled during performance analysis. The global tradeoff mentioned above, together with the need for better models, will require ever closer unifications of physical design with system-level design, logic-level design, and circuit implementation. Additionally, new design methodologies need to be developed to support tight coupling of analysis, synthesis, and (re)specification activities across multiple levels of representation. These needs apply equally to the design of digital, mixed signal, and analog systems.

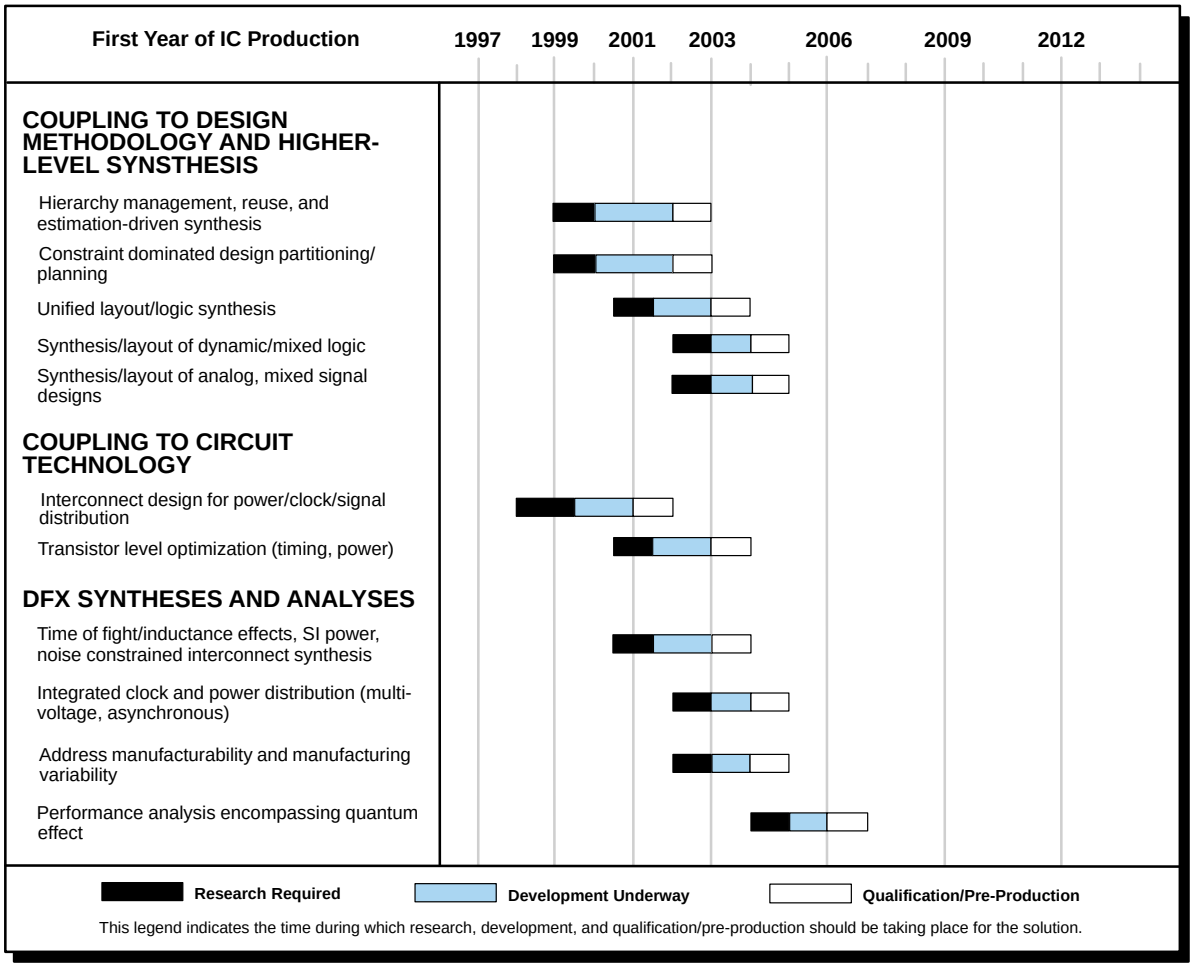
Several new requirements will emerge in the physical design context. Increased design complexity and reuse together imply a need for new block characterization tools, as well as new data management and hierarchy management tools. Increased adoption of area-array I/O implies a need for tools that address associated power/clock/test distribution, reliability, and noise issues. Increased clock frequencies imply

a need for high-frequency and analog/mixed signal design tools. Manufacturing variability implies a need for statistical design and design centering tools. Overall, future physical design tasks will entail interacting multi-level, multi-objective optimizations. Such optimizations will be increasingly constraint-dominated and more degrees of freedom must be considered simultaneously to achieve a feasible solution. (For example, future routers might simultaneously apply wire tapering, shielding, spacing, repeater insertion, and detailed placement). Rethinking sequential algorithms and tool interactions for symmetric multiprocessing will be important.

In summary, future physical design needs can be broadly classified as "unifying physical design" or as "new syntheses and analyses," as shown in Figure 7. Four unifications of design within the design flow are especially critical, as follows:

1. *Analyses and syntheses* must be unified to erase barriers between today's disparate design flow. Constraints must drive synthesis, and estimated parasitics drive analysis, in a closed-loop, "construct by correction" iterative improvement process. An example of a potential solution is a new analysis backplane that enables performance analysis that integrates simulation traces with analyses of hardware description language hierarchy, clock structure, and device noise sensitivities
2. *Layout-level and system-level design* must be unified. Modeling capabilities must be developed to enable forward estimation-driven syntheses and design exploration. New tools will be needed to support hierarchy and reuse across multiple implementation levels, as well as auto-interactive and iterative design paradigms.
3. *Layout-level and logic-level design* must be unified. In particular, system timing management, logic optimization, placement, and routing must coexist in a single environment within the next two process generations.
4. *Layout-level and circuit-level design* must be unified, e.g., for synthesis of dynamic CMOS circuits and for transistor-level layout within cell-based design.

The roadmap of physical design needs also includes "new syntheses and analyses" to achieve acceptable design quality with respect to (a) limited interconnect resources, (b) signal integrity, (c) power and reliability, (d) manufacturability, and (e) other drivers (e.g., transmission-line and quantum effects). In general, as future designs become increasingly interconnect-limited, physical design must carefully balance all of these factors.



DFX—design for manufacturability

Figure 7 Physical Design Potential Solutions

SYSTEM AND IC VERIFICATION AND ANALYSIS

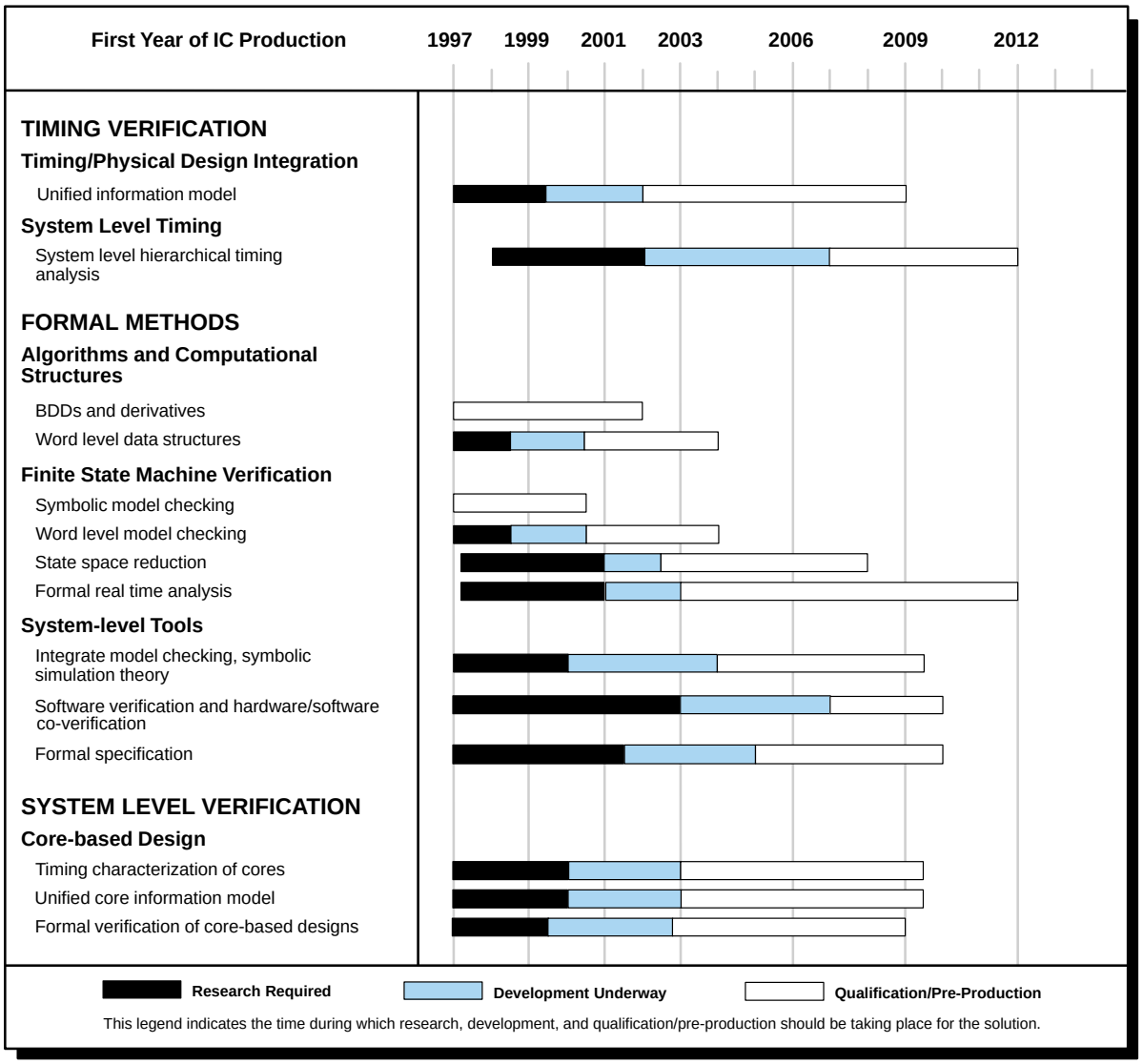
Verification and analysis are serious bottlenecks for the timely design of systems and ICs. It is estimated that verification requires between one third and one half of the total time expended in the design process. Analysis and verification problems in general are exacerbated by the growing number of devices on a chip and by the inclusion of digital and analog devices (perhaps even sensors) on the same chip. For digital designs, the use of in-circuit emulation, improved simulation technologies and formal verification are just barely keeping up with complexity. For mixed signal digital and analog chips, some tools for analysis and verification exist, but major improvements will be required to deal with the greater complexity levels anticipated. For RF chips, only rudimentary tools suitable for small circuits are currently available. Significant research is required to develop tools and methods for designing VLSI systems that include RF circuitry.

Increasing complexity demands more automation of the design process. As the clock speed and performance of integrated circuits continues to increase, chip packaging is limiting system performance. Solutions such as flip chip and chip-on-board will continue to expand. Verification tools that comprehend a signal path from one chip, through the system interconnect, and onto the next chip must be developed. New ideas and automated tools in formal verification, simulation, emulation, and hybrid approaches are needed now to handle the synthesis, analysis, and verification problem.

Typically designs are modeled at many different levels of abstraction, including system, architectural, micro-architectural, RTL, gate, switch, and layout. Extensive verification is required at each level of abstraction in the design flow, but in addition, cross-verification among abstraction levels is a critical need.

Verification and analysis activities fall into the following general categories:

- The semiconductor industry needs mathematically precise system and architectural models, automated analysis tools that handle the complexity now routine on a single chip, and automated verification tools that can guarantee compliance of a higher level model with a lower level model of the same design. System-level design and hardware/software co-design initiatives have not yet produced commercially usable tools that solve these difficult verification and analysis problems.
- For models at the RTL and below, many verification tools and methodologies exist, but they are only marginally adequate, due to reduced device feature size, increased clock speeds of synchronous designs, and increased dominance of interconnect over transistor performance in critical timing nets—not to mention mixed signal design issues. With the advent of designs based on subcircuits (cores) comes increased importance of careful characterization of cores with respect to functionality, timing, and electrical properties to allow cores to be reused and functional models distributed to safeguard intellectual property.
- Functional verification, which abstracts away most timing and implementation details, increasingly exploits emerging formal methods, a family of powerful techniques that use mathematical methods rather than simulation. Formal methods have proven useful in many digital applications to date, but are currently quite limited in terms of problem size. Much research is needed to apply these methods to larger circuits, to applications beyond purely digital, and to full systems. Because the available tools and techniques lag so far behind current and future needs, even research prototypes are often used immediately. Thus in this field, there is an unusual amount of concurrency among research, advanced development, and pre-production.
- As interconnect performance becomes a larger factor in the design problem, physical parameters will need to be expressed in an information model that includes timing methodology. Truly innovative timing analysis and verification methods, comprehending wires, parasitics, and the analog nature of dynamic signals are a critical research need; these new capabilities must be available for development by the 150 nm technology generation.



BDD—binary decision diagram

Figure 8 System and IC Verification and Analysis Potential Solutions

DESIGN TECHNIQUES AND METHODOLOGIES

Design methodology is the sequence of steps that create a system. It is the philosophy and ordering of the steps, including the kind of information that is passed between the tools, that accomplish the steps. Both a top-down and bottom-up approach must be used. A top-down system approach should make tradeoffs across discipline boundaries and give high-level feedback on specifications. The bottom-up approach demonstrates feasibility of critical blocks. This combination of methodologies will become increasingly important to integrate entire systems on a single chip. Increasingly, VLSI design methodologies must include disciplines such as software, user interfaces, and power scaling.

Design techniques are the specifics of implementing the steps that make up a methodology. Often, various design techniques can be used to fulfill each step in a design methodology. The development of innovative design techniques generally requires that research be driven by an application. However, the techniques usually do not emerge in the course of product development, since the time-to-market and risk-management pressures often prohibit the investigation of unproven design approaches. It is imperative that some level of investment be allocated to pre-product design techniques to assure an uninterrupted flow of innovation.

Figure 9 presents the potential solution for design techniques and methodologies. As the level of design complexity increases and the focus changes to system integration, the need for hierarchical design methodologies and higher levels of abstraction will increase. These will break a design down into smaller tasks that can be executed concurrently and allow constraints to be imposed at the highest possible level of abstraction. Some levels of the hierarchy will be fulfilled using previously designed circuits or cores. The change to a clean hierarchical design methodology will require new data models and design techniques. A complete set of tools for all tasks, e.g., timing, clock distribution, signal integrity, test generation, etc., must be created that work together seamlessly in a distributed design environment. This environment must provide for the integration of point tools from multiple vendors, as well as user-written, application-specific tools. Interoperability standards for tools at all levels will be an essential enabler. It will be essential that these standards provide for work across levels of hierarchy and across disciplines. Application-specific CAD providers will become more prevalent as design houses themselves become more specialized.

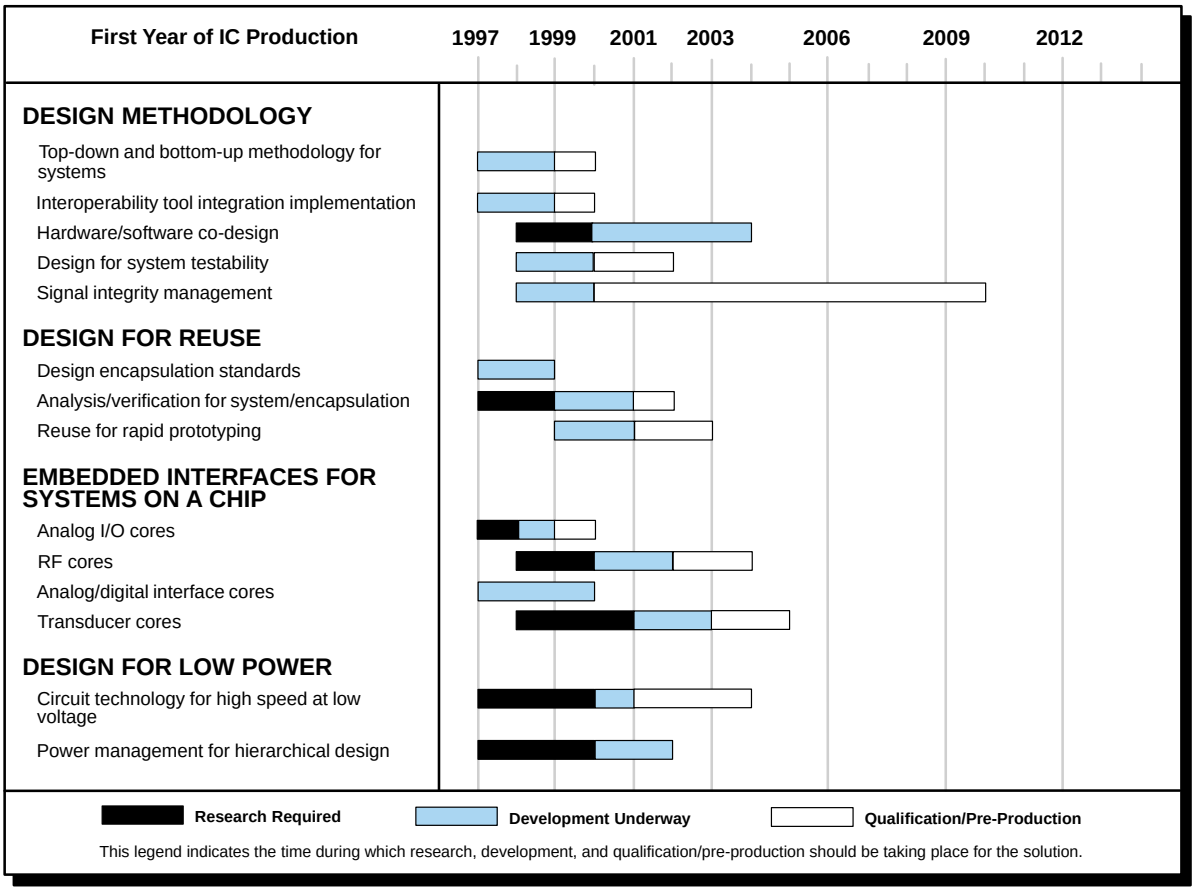


Figure 9 Design Techniques and Methodologies Potential Solutions

Advances in silicon processing technology will enable much higher levels of integration. Design reuse and embedded interfaces will enable the implementation of complex systems on a single chip. The sharing of cores among companies will help fuel design reuse. The encapsulation of complex designs will enable companies to retain their intellectual property while licensing the use of their proprietary digital and analog cores to others. These cores will include not only I/O circuits, analog/digital interfaces, micro-controllers, DSPs and bus interfaces, but also modems, optical transceivers, and RF interfaces. Signal integrity, cost, and performance issues will preclude the integration of some interfaces within large VLSI system chips. Field programmable gate array (FPGA) circuits will play an important role in interfacing between cores on these chips.

Verification and Design For Testability (DFT) will become dominant activities in achieving large systems. Work must start immediately to assure that tools to encapsulate cores are available. Not only will it be necessary to create behavioral simulation models, but timing analysis, formal verification, and DFT models must also be automatically generated for digital cores. Analog cores will need similar tools in the near future.

Power management calls for the emergence of a whole set of circuit techniques that optimize power at the chip and total system level. These must deliver the required performance for digital and analog functions at voltage levels down to 1.8 volts and perhaps lower. Proper interfacing between subsystems operating at different voltage levels, even on the same chip, will be essential. Accurately estimating and effectively managing the power at the system level will require an approach combining several levels of abstraction. New algorithms and approaches will be necessary in this area.

In a hierarchical design, system reliability requirements propagate down to become part of the chip-level design constraints. At the chip/package/system level, signal integrity issues like crosstalk, timing, and degradation must be considered. Extraction and calculation of interconnect parasitics and ultimately the inclusion of the interconnect as a fully modeled circuit element that contributes to interconnect delays and distortion will be required.

TEST METHODOLOGY

Test continues to be a major expense in the IC development and manufacturing chain, with up to 35% of nonrecurring engineering (NRE) costs attributed to test development and debug, and with large testers costing up to $6 million. Changing processes and design methods are pushing testability beyond economic limits. Rapid improvements must be made to improve overall testability and test economics.

- *New divide-and-conquer* techniques must be developed to manage test complexity. Without fragmenting the test problem into manageable pieces using automation and standardization, the task of developing adequate tests will become unacceptably slow.
- *Reuse of cores* requires the encapsulation and reuse of test as well. Interfacing and access methods to get test access for cores are needed, and composition methods to assemble complete chip tests for chips with multiple cores, including analog cores, are needed. Methods to test the interconnect between cores must also be developed, and signal integrity standards developed to assure that cores, when embedded, function as expected within the larger chip, even in the presence of noisy power, grounding, and interconnect. In addition, tests for embedded cores must be more tester-independent than today's typical tests, as different cores with tests targeted at particular (different) testers may not be usable together.
- *Built in self test* needs to be made usable in short-design cycle environments by novice designers. Logic BIST methods must be developed that give fault coverage for hard-to-target faults, and for all fault types required.
- *Fault models'* standards are required for fault models and coverage metrics for these models, so that a common language can be used to describe fault coverage. New fault types must be quickly identified, and test methods developed for them, as net timing and signal integrity problems increase dramatically and introduce additional new modes of chip failure.
- *Synthesis systems* must include automatic test generation with high coverage for all relevant fault types (e.g., stuck-at faults, timing, bridging, signal integrity). Synthesis systems will have to conform to methodologies used for embedding cores and interconnecting test and timing domains in complex ICs. Synthesis systems for memory, datapath, and other circuit types will have to provide full test automation.
- *Signal integrity* and electromagnetic (EM) phenomena will become an increasingly important test issue as chips and test equipment become complex. New fault models (including soft error models) that incorporate the effects of EM fields must be developed. Relationships between design constraints and manufacturability and testability must be developed for different design domains. Test generators must be sensitive to signal integrity issues.

- *Timing tests* are impacted by interconnect delays, slow synthesis system drivers, increased frequencies, and clock skew. Automatic test generation will be necessary to accommodate the large number of near-critical paths, and BIST systems will have to guarantee high coverage of timing faults.
- *Direct drain quiescent current (IDDQ) testing* requires extensions or a replacement technique for failure analysis. New processes may make it difficult or impossible to employ IDDQ test, and the loss of such a tool will place a higher burden on other test methods.
- *Hardware/software codesign* will provide opportunities for system software to be used as an aid for test. All high-level design methodologies must be sensitive to the fact that they may target unknown libraries and processes with special test problems and unknown fault statistics.
- *Analog/RF systems* present continuing challenges for test, primarily because analog signals represent data with highly varied encodings. Also, there is inherent difficulty in presenting any simplification to create a meaningful fault model. As such, none exist or are likely to exist, and so each application type must be considered as unique.
- *Yield improvement and failure analysis* tools must be developed to provide for rapid yield learning with very complex chips containing embedded cores (on the actual chips, not simplified test devices), and for highly automated failure analysis where faults can no longer be visually detected. Design and synthesis for diagnosis must be included if short failure analysis and yield improvement cycles are to be realized.

Other issues include the insertion of testability circuitry in systems limiting the operating speed of the system. Power consumption during test must be carefully considered so test programs don't put the system into modes which consume excessive power. Application of test programs must also not cause excessive noise with the possibility of soft errors.

TEST AND TEST EQUIPMENT ROADMAP

SCOPE

The Test roadmap focuses on two distinct areas 1) equipment characteristics needed to test devices fabricated on a process technology for digital—ASIC and mixed signal ICs (Table 11 presents digital–ASIC; Table 12 presents the mixed signal requirements); and 2) the impact of test in the manufacturing and defect detection processes. The Test roadmap focuses on the trends seen today and the perceived roadblocks in the future. Only a small subset of issues are discussed, those that require paradigm changes, major research, or process and design changes.

The 1994 Roadmap presented BIST and DFT as potential solutions for achieving simpler and affordable test equipment. However, the present test technology being used for automatic test equipment (ATE) will not solve the test problems during the 1997 Roadmap period. Table 9 shows the difficult challenges facing the Test technologies. Fundamental physics problems, timing inaccuracies, noise, along with escalating cost, demand a change in test methods. Currently, there are no clear answers to these problems. Such issues must be addressed to ensure continued progress and to meet the requirements of the Roadmap.

Table 9 Testing Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
BIST and DFT	Test equipment costs will rise toward $20M and wafer yields will fall toward zero unless there is increased use of DFT and BIST.
Probes and test sockets	A major roadblock will be the need for high frequency, high pin count probes and test sockets; research and development is urgently required in this area.
Mixed signal instruments	These will require more bandwidth, higher sample rates, and lower noise. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits.
IDDQ testing	This testing may not be viable when ICs contain tens of millions of transistors; circuit partitioning and built-in current sensors should be studied.
Test development time	Mixed signal test development time must be reduced; analog DFT and BIST are key areas for research.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Fault models	New fault models will be needed for advanced, multi-level metal ICs; the traditional stuck at model is becoming less effective.
Rules to test	Tools and rules to automatically check the correctness of test program and DFT.
Standard test software	Common definition of test tools; nomenclature to make tests portable with minimal efforts are needed.
DFT	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years; breakthrough tools for control and observation are needed.)
Failure Analysis	3-D CAD and FA systems for isolation of defects in multilayer metal processes

FA—failure analysis

TECHNOLOGY REQUIREMENTS

The basic capabilities of the automatic test equipment must keep up with the device scaling trends toward lower voltage, greater transistor and pin count, extended test patterns and improved accuracy along with mixed analog and digital signals. The main issues seen by the test working group are as follows:

- Potential yield losses as the cycle time of manufactured devices becomes comparable to the timing accuracy of the ATE
- Increasing cost of capital equipment, driven by increasing pin count, high frequency, and features
- Requirement of test to support yield learning and defect detection, and failure analysis

POTENTIAL YIELD LOSSES

Most of the technology problems causing major yield losses and cost increases are related to the slower growth of ATE speeds versus the ever improving device speed as shown in the overall Roadmap characteristics charts. For example, microprocessor and ASIC speeds require increasing accuracy for resolution of timing signals. While tester accuracy has improved at a rate of 12% per year, semiconductor speeds have improved at 30% per year. Typical headroom of testers five times faster than device speeds have all but disappeared. If the current trends continue, in less than ten years, tester timing errors will approach the cycle time of the fastest devices. A crossover may occur near 2010, but by 2001, yield losses due to tester inaccuracy will be unacceptable. Table 10 shows the forecast trend for overall timing accuracy as defined by the SEMATECH document, #97013234A–TR.[5] Also shown is the cycle time of high end products over the Roadmap period.

5. SEMATECH. *Automatic Test Equipment (ATE) Specification*, 97013234A–TR. Austin, TX: SEMATECH, May 6, 1997.

Table 10 Yield versus Test Accuracy

Year of First Product Shipment		*1997*	*1999*	*2001*	*2003*	*2006*	*2010*	*2012*
Yield	%	90	87	84	79	75	64	52
Device period	ns	1.3	1.1	0.91	0.77	0.59	0.43	0.33
Test accuracy	ns	0.2	0.2	0.19	0.18	0.175	0.175	0.175

Solutions Exist *Solutions Being Pursued* *No Known Solution*

AUTOMATED TEST EQUIPMENT COST

The ATE cost per pin for high-performance machines has remained essentially flat for the past 20 years at around $10K/pin. The demands of higher speed, greater accuracy, more time sets, and increased vector memory offset all the gains in cost reduction seen for improving ATE cost. That trend is expected to continue toward $20M test systems unless there is a major change in IC device design incorporating more BIST and DFT. By 2012, it may cost more to test a transistor than it costs to manufacture the transistor. The increase in test system cost will be overwhelmed by the losses in profits if ATE accuracy cannot keep up with the device speed.

TEST AND YIELD LEARNING

Although there are test issues related to cost and performance, test provides another major service for the semiconductor industry. Today the best tool for analysis of defects in the manufacturing process is the test equipment. Time-to-yield, time-to-money, time-to-quality, and time-to-market are all gated by test. The feedback loop derived from the test process is the only way to analyze and isolate many of the defects in today's processes. Test must continue to support cost-effective process measurement and defect isolation.

The migration of CMOS technology towards 100 nm feature sizes will severely challenge the device failure analysis process. Improvements are needed in fail verification, fault localization, de-processing, and physical characterization. Two categories of needs are discussed: evolutionary or incremental, and revolutionary or breakthrough. While much will be served by evolutionary solutions, the fault localization challenge is especially acute and in need of major breakthroughs. It represents by far the most critical failure analysis need. Understanding failure mechanisms and providing corrective action cannot occur without the ability to localize faults to an area of the chip that can be inspected in a practical and cost-effective manner. Likewise, tools for yield improvement cannot be developed.

EVOLUTIONARY NEEDS FOR DIAGNOSTICS

Incremental improvements to existing tools and techniques are required to keep pace with technology. Examples include regular increases in scanning electron microscope (SEM) resolution and the development of plasma delayering processes for new films. Many routine developments of this nature are required across the failure analysis process as follows:

- Wet and dry delayering processes for new films
- Focused ion beam cross-sectioning, milling, and deposition
- SEM and acoustic microscope resolution
- Integration of CAD navigation across the FA tool set
- Depackaging processes
- X-ray radiography resolution
- E-beam tester resolution, cross-talk, etc.

REVOLUTIONARY NEEDS FOR DIAGNOSTICS

Revolutionary needs require major shifts in capability, driven by drastic changes in analytical method. Examples include high spatial resolution wafer back-side thermal mapping and back-side waveform acquisition. Developments in this area are the most critical and require major efforts of industry,

academia, the national laboratories, and analytical equipment suppliers. The following is a prioritized list of these needs:

1. Software-based fault localization tools compatible with major test methodologies (e.g., scan, IDDQ, BIST, stuck-fault, AC test, dynamic logic, embedded cores) (An especially important subset of these are tools for localization of AC or performance fails.)
2. Hardware-based fault localization tools to complement and supplement the above as appropriate (e.g., migration of existing capability [waveform acquisition, emission testing, thermal mapping] to the backside of the chip and backside thinning techniques)
3. Inspection techniques beyond optical microscopy that offer high resolution without sacrificing throughput
4. Internal node DC micro-probing capability for characterizing individual circuit or transistor parameters or isolating leakage paths (Existing opto-mechanical systems are inadequate.)
5. Signature analysis techniques to significantly reduce or eliminate the need for physical failure analysis

Table 11 Microprocessor and ASIC Test Equipment Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
High-perf. ASIC and MPU							
On-chip RZ* clock MHz	750	1250	1500	2100	3500	6000	10000
Off-chip NRZ** data MHz	750	1200	1400	1600	2000	2500	3000
Overall Timing Accuracy (% period)	± 5.0	± 5.0	± 5.0	± 5.0	± 5.0	± 5.0	± 5.0
RMS Clock Jitter (% period)	2	2	2	2	2	2	2
External Test Vectors without BIST or DFT (maximum)	64M	126M	240M	456M	1200M	3120M	8400M
Design for diagnosability On-chip test: BIST/DFT (% of average IC tested)			Increasing		Increasing		Increasing
Maximum Signal pk–pk Range (V)	1.8–5.5	1.3–3.3	1.3–3.3	0.9–3.3	0.9–2.5	0.6–2.5	0.6–2.5
Power/Device DC W High-perf.	70	90	110	130	160	170	175
Transient Power W with heatsink	105	135	165	195	240	255	260
Tester Cost $K per High Frequency Digital Pin (Characterization and Production)	5–10	5–10	5–10	5–10	5–10	5–10	5–10
Max Number I/O Pads for Wafer Test							
(MPU)	512	512	640	768	768	1024	1280
(ASIC)	1100	1400	1700	2200	3000	4000	5300
Pad Pitch—Arrays (microns)	250	200	200	200	150	150	150
Pad Pitch—Peripheral (microns)	70	50	50	50	50	50	50
Package Pitch—Arrays (microns)	500	350	250	250	250	250	250
Package Pitch—Peripheral (microns)	400	400	400	300	300	300	300
IDDQ	Test	Test	Test	Analysis	Analysis	Analysis	Analysis
Embedded Memory (Mbits)	32	80	200	500	2000	8000	32000

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *RZ—return to zero waveform*
** *NRZ—nonreturn-to-zero waveform (NRZ data rates are often referred to as Mbits per second)*

MIXED SIGNAL TESTING

The trend of more system functionality on a single piece of silicon will increasingly blur the lines between traditional digital, analog, and mixed signal devices RF/microwave. The digital needs of mixed

signal test equipment will follow the digital roadmap. The trend in test equipment is toward a modular high speed and high pin count digital test platform where high-performance analog/RF/microwave instruments can be added as needed. The analog issues and technology limiters are higher bandwidth, higher direct conversion sampling rates, higher dynamic range, lower noise floors, integration of the digital and analog instruments, and cost.

Table 12 Mixed Signal Test Equipment Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Low Frequency Source & Digitizer							
BW (MHz)*	2	2	2	2	4	4	4
Fs MS/s**	5	5	5	5	10	10	10
Bits	20–23	20–23	20–23	20–23	20–23	20–23	20–23
Noise floor (dB/RT Hz)	–130	–136	–142	–150	–160	–160	–160
High Frequency Waveform Source							
Level V (pk–pk)	4	4	4	4	4	4	4
BW (MHz)	500	666	833	1000	1500	2000	2000
Fs (MS/s)***	1000	1500	2000	2500	3500	4500	4500
Bits AWG/Sine†	10/14	10/14	10/14	10/14	10/14	10/14	10/14
Noise floor (dB/RT Hz)	–80	–86	–92	–100	–100	–100	–100
High Frequency Waveform Digitizer							
Level V (pk–pk)	4	4	4	4	4	4	4
BW (MHz) (undersampled)	750	1000	1250	1500	2000	3000	3000
Fs (MS/s)	1/40	1/40/80	1/40/80	1/40/160	1/40/320	1/40/640	1/40/1280
Bits	16/12	16/12/10	16/12/10	16/12/10	18/14/12	18/14/12	20/16/12
Noise floor (dB/RT Hz)	–80	–86	–92	–100	–120	–120	–120
High Speed Sampler							
BW (GHz)	1	2.3	3.6	5	5	5	5
Resolution (bits)	16	16	16	16	16	16	16
Time Measurement							
Jitter measurement (ps RMS)	30	24	17	10	7	5	4
Frequency measurement (MHz)	250	500	750	1000	2000	3000	3000
Single shot time capability (ps)	100	100	75	50	30	30	30
RF/Microwave Instrumentation							
Source BW (GHz)	6	10	14	18	24	30	36
Source phase noise low frequency (dBc/Hz)	126	130	136	136	136	136	136
Source phase noise high frequency (dBc/Hz)	150	155	160	160	160	160	160
Receive BW (GHz)	6	10	14	18	24	30	36
Receive noise floor (dBm/Hz)	–150	–155	–160	–160	–160	–160	–160
Receive dynamic range SFDR (dB)‡	60	70	80	80	80	90	90
Special Digital Capabilities							
D/A and A/D source/capture rate (Mbits/s)§	100	200	300	400	400	500	600
Serial data rate (Mbits/s)	2000	3000	4000	4000	4000	4000	4000

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *BW—Bandwidth*
** *Fs—Sample rate*
*** *MS/s—Megasamples/second*

† *AWG/Sin—Arbitrary waveform generation/sine wave*
‡ *SFDR—Spurius free dynamic range*
§ *Mbits/s—Megabits/second*

Table 12 focuses on test instruments rather than IC devices. The current analog/RF/microwave testing methodology requires measurement of device performance. Therefore, the test instrument needs reflect the increasing device performance predicted in the process technology roadmaps. This trend of increasing instrument performance is expected to continue and will drive up the cost of test equipment. No proven alternative to performance-based analog testing exists; more research in this area is needed.

MIXED SIGNAL ISSUES

1. The analog/RF/microwave signal environment seriously complicates load board design and test methodology. Noise crosstalk, signal mixing and load board issues will dominate the test development process and schedule.
2. To minimize test time, all analog pins will have to be tested in parallel. This requires multiple instruments with fast and parallel execution of DSP test algorithms (FFT's etc).

Standard software tools are needed. Tools are required for digital and mixed signal vector generation; circuit simulation of the device's analog circuitry along with the load board and the test instruments; and rapid mixed signal test program generation.

PROCESS INTEGRATION, DEVICES, & STRUCTURES

SCOPE

The *Process Integration, Devices, & Structures (PIDS)* section addresses concepts that affect full process flow and the manufacturability and reliability tradeoffs associated with new options. This scope has been broken into four subcategories described below. The overarching theme of this section is the need to include more embedded functions into the design of an IC, with simultaneous satisfaction of constraints of interconnection, power consumption, reliability, and device performance. Table 13 presents the difficult challenges facing the PIDS technologies.

MEMORY AND LOGIC

Process integration optimizes the overall architecture of the full process. This includes the silicon active device as well as the on-chip interconnect hierarchies for power, clock, and signal distribution. The architectural tradeoff between the devices and interconnect structures are driven by performance, density, and reliability requirements. Devices and structures refer to the active transistors, interconnect, and other structures required for logic and memory cell design. Memory cells include DRAM, SRAM, and nonvolatile memory. These memory cells are applied to both commodity and embedded applications. Physical and electrical design rules are also included within PIDS and address physical and electrical parameters. This includes physical dimensions, key active device electrical parameters, passive electrical parameters, and reliability criteria. Nominal targets as well as statistical tolerances are important.

ANALOG, MIXED SIGNAL, AND RADIO FREQUENCY (RF) DEVICES

The commodity driver applications for analog, mixed signal, and RF ICs are projected to remain in personal computing and communications. Analog refers to "pure" analog circuits such as operational amplifiers. Mixed signal includes integrated circuits containing both digital and analog functions, such as analog-to-digital and digital signal processing circuits. RF refers to pure analog and mixed signal integrated circuits operating above 800 MHz, such as for wireless communications and "radio on a chip." Certain analog IC technologies such as high voltage and power ICs are not specifically included, while others, such as microelectro-mechanical devices and structures (MEMS), are included in the out years. Such devices must reuse and leverage the expertise gained from mainstream, digital CMOS technology to remain low cost, and meet the demands for high-performance and reliability.

SHORT-FLOW

Short-flow methodology enables the planning and implementation of rapid process sequences to acquire data from metrology equipment and electrical testers to characterize and validate process modules, equipment, and simulators. The key customers for short-flow methodologies include process and metrology equipment suppliers; process integration, manufacturing, and reliability engineers; technology computer aided design (TCAD)/engineering CAD (ECAD) tool suppliers; and factory/cost modeling engineers.

RELIABILITY

To maintain the current reliability levels, the accelerating use of new materials/processes will need to be introduced without the usual database gathering on new failure regimes and defects. Current prevalent defects (i.e., resistive vias) cannot be allowed to scale with the technology and will require a breakthrough technology. These issues place difficult challenges on testing and wafer level reliability (WLR). Packaging interface reliability is particularly vulnerable because of new materials and processes, form factors, tighter lead and bond spacing, severe environments, adhesion, and customer manufacturing capability issues.

DIFFICULT CHALLENGES

Table 13 Process Integration, Devices, & Structures Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Integration of analog and memory with logic	V_{dd} compatibility, high Q passive elements, and increased process complexity
Management of increasing reliability risks with rapid introduction of new technologies	A cluster of new materials is being aggressively introduced; these typically require 5–10 years of R&D. Higher current densities, scaling, and increased power are not supported by new reliability models, databases, and diagnostic/failure analysis tools.
Maintaining the scaling of functional DRAM density faster than lithography feature size scaling	Current memory cell materials, designs, and architectures do not allow desired increase in memory cell density for scaled technologies.
Cost-effective technology integration using short flow methodology	Scaleable reusable short-flow processes and test designs Rapid statistical data analysis methods Predictive modeling techniques that incorporate cross-module inter-relationships; applicability to commercial equipment and TCAD/ECAD software
Design for manufacturability, reliability, performance (DFX)	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, etc. Validated 2-D/3-D* TCAD simulators for process control, reliability, performance
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Signal isolation and noise reduction technology	Inadequate signal shielding techniques to isolate analog and digital blocks and to protect critical paths Increased sensitivity to noise in scaled circuits
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variation
Integrated management of power, ground, signal, and clock on multilevel coupled interconnect	Interconnect scaling is increasing crosstalk, signal integrity, and parasitic RC delay issues Power, clock, and ground distribution will consume an increasing fraction of available interconnect
Function integration at low V_{dd}	Integration of logic, analog, and flash on a chip at low V_{dd}
Gate stack and source/drain (S/D) integration	Future technology nodes will require the integration of unique process modules that promote high integrity gate dielectrics, high conductivity gate materials, shallow S/D extensions, sidewall control, minimum TED**, and low contact resistance junctions

* *2-D/3-D—2- and 3-dimensional*
** *TED—transient enhanced diffusion*

DESCRIPTION OF PIDS DIFFICULT CHALLENGES

1. *Integration of analog and memory with logic*—Increased complexity includes integration of multi-V_t devices, active devices with high gain and stable saturation characteristics, high κ and high quality dielectrics for DRAM and nonvolatile memory, and high quality passive devices (high Q inductors and capacitors).
2. *Reliability risk management*—The unprecedented number of new materials introduced per generation, coupled with inadequate reliability understanding for each material, presents a significant risk that customer reliability requirements will not be met. The increasing complexity, smaller feature sizes, and move to flip chip is outstripping the capabilities of diagnostics and failure analysis that traditionally predict an increased time to develop new technologies and products.

3. *Functional density scaling*—Self-alignment techniques and improved lithography tolerances will not meet the requirements for rapid DRAM density increase with scaling. Innovations in new memory cell/architecture such as multi-state memory cells will be required.
4. *Cost-effective technology development*—Short-flow methodologies need to be developed based on an improved fundamental understanding of the complex cross-module relationships. Key requirements are the development of critical short-flow measurement metrics and designing reusable/scalable test chip designs. Short-flow methodologies will have a significant impact on TCAD/ECAD models, full-flow process development, application-specific enhancements, commercial equipment development, and future technology selections.
5. *Design for X*—High product yields require tight parametric control, and minimization of statistical variations in mask design, individual tool performance, cross-module variations, etc. A robust methodology is needed to accurately model and incorporate this wide range of statistical variations and process sensitivities into the ECAD tools. This is referred to as Design for "X" (DFX), where X is manufacturability, reliability, etc. DFX requires accurate TCAD models and software tools for all future scaled integration challenges such as process control, proximity effects, reliability, manufacturing capability, and performance. The development of smart ECAD tools with DFX capability will become critical for future technology development and cost-effective manufacture.
6. *Signal isolation and noise reduction*—Noise-sensitive analog circuitry must be protected from noisy digital circuitry. Isolation technology must shield digital switching noise through the substrate, interconnect, and package. Shielding is required on signal paths, circuit blocks, and I/O. Noise reduction techniques in active and passive devices require innovation in structures and modes of operation.
7. *Atomic level fluctuations and increasing process variations*—For advanced device structures/architectures, statistical process and dimensional variations will be a more significant barrier to achieving high-performance and yield. While the absolute control of processes and alignment is improving, the percentage variation must not be allowed to increase. Statistical variation of the dopant atoms in the channel region will limit threshold voltage control. To address these issues, novel device structures such as inherently self-aligned or adaptive transistors, or nonlithographically defined structures, will be required.
8. *Managing power, ground, signal, and clock on multilevel coupled interconnect*—Crosstalk and increased parasitic RC delay are becoming limiting factors in scaled interconnect systems. Incorporating low κ dielectrics will not eliminate these problems. With distribution of power, ground, and clock consuming an increasing fraction of the available interconnect, new interconnect architectures are needed. The interconnect issues are inter-related, and can only be solved by careful integration of new materials, process, architecture, and design tools.
9. *Function integration at low V_{dd}*—Future systems on a chip (SOCs) will require integration of logic, analog, and memory on the same chip at low power supply voltages. Each of these technologies faces its own particular problems at low V_{dd}. In logic technology, the challenge is to balance the competing requirements of high-performance and low standby power. Analog circuits will face major problems of head room and signal-to-noise. Flash memory requires higher programming voltages on-chip. Integration of these technologies will be a major challenge.
10. *Gate stack and source/drain (S/D) integration*—High κ gate dielectrics will be required to avoid the excessive tunneling currents of scaled oxynitrides. High conductivity gates with low/no depletion are needed to meet performance requirements. The ultra-shallow S/D extension affects parameters such as drain induced barrier lowering (DIBL) and L_{eff} control. Cleans, etches, implants, and anneals must be consistent with the reliability, control, and low parasitic requirements.

TECHNOLOGY REQUIREMENTS

Tables 14 through 17 present the technology requirements for the four focus areas. This is followed by discussion of key issues.

Table 14 Memory and Logic Technology Requirements

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*	*2006* / *100 nm*	*2009* / *70 nm*	*2012* / *50 nm*
Min. Logic V_{dd} (V) (desktop)	2.5–1.8	1.8–1.5	1.5–1.2	1.5–1.2	1.2–0.9	0.9–0.6	0.6–0.5
V_{dd} Variation	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
T_{ox} Equivalent (nm)	4–5	3–4	2–3	2–3	1.5–2	< 1.5	< 1.0
Equivalent Maximum E-field (MV/cm)	4–5	5	5	5	> 5	> 5	> 5
Max I_{off} @ 25°C (nA/μm) (For minimum L device)	1	1	3	3	3	10	10
Nominal I_{on} @ 25°C (μA/μm) (NMOS/PMOS)	600/280	600/280	600/280	600/280	600/280	600/280	600/280
*Gate Delay Metric (CV/I) (ps)**	16–17	12–13	10–12	9–10	7	4–5	3–4
V_T 3σ Variation (± mV) (For minimum L device)	60	50	45	40	40	40	40
L_{gate} 3σ Variation (For nominal device)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
L_{eff} 3σ Variation (For nominal device; % of L_{eff})	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%
S/D Extension Junction Depth, Nominal (nm)	50–100	36–72	30–60	26–52	20–40	15–30	10–20
Total Series Resistance of S/D (% of channel resistance)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
Gate Sheet Resistance (Ω/sq)	4–6	4–6	4–6	4–6	4–6	< 5	< 5
Isolation Pitch	Consistent with the linear scaling per generation						
Interconnect Levels	6	6–7	7	7	7–8	8–9	9
Short Wire Pitch (μm)	0.50–0.75	0.36–0.54	0.30–0.45	0.26–0.39	0.2–0.3	0.14–0.21	0.10–0.15
DRAM Cell Size (μm^2)	0.56	0.22	0.14	0.09	0.036	0.014	0.006
Soft Error Rate (FITs)	1000	1000	1000	1000	1000	1000	1000
DRAM Retention Time (ms)	64–128	128–256	–	256–512	512–1024	1024–2048	2048–4096
Flash Data Retention (year)	10	10	10	10	10	10	10
NOR Cell Size (μm^2)	0.6	0.3	0.22	0.15	0.08	0.04	0.02
+/– V_{pp}	8.5	8	8	7.5	7	6.5	6
Tunnel Oxide (nm)	8.5	8	8	7.5	7	6.5	6
Flash Endurance (erase/write cycles)	100K	100K	100K	100K	100K	100K	100K
ESD Protection Voltage (V/μm)	6	7.5	9	10.5	12	13.5	15

Solutions Exist *Solutions Being Pursued* *No Known Solution*

** The CV/I gate delay metric is calculated using the data in this table along with the microprocessor gate length given in the ORTC table (Appendix B). The transistor width is assumed to be 5 mm for NMOS and 10 mm for PMOS at the 250 nm generation. Device width is then scaled consistent with minimum feature size scaling.*

Table 15 Analog, Mixed Signal, and RF Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Minimum Analog Supply Voltage (V)	2.5–1.8	1.8–1.5	1.6–1.3	1.5–1.2	1.2–0.9	0.9–0.6	0.8–0.5
Transmit/Receive Frequency (GHz)	1.8–2.5	2.5–3.5	3.0–4.0	3.5–5	5–6.5	6.5–9.5	9.5–13
*Transistor**							
Current (μA)**	100	75	60	50	40	30	20
f_{max} (GHz)	25	35	40	50	65	90	120
f_t (GHz)	20	30	35	40	55	75	100
Noise figure (db)	2	1.5	1.3	1.2	≤ 1	≤ 1	≤ 1
1/f spectral density (V^2/Hz–μm^2)	5×10^{-12}	2×10^{-12}	5×10^{-13}	5×10^{-13}	5×10^{-14}	2×10^{-14}	2×10^{-15}
Gate oxide leakage (pA/μm^2)***	< 0.01	< 0.01	< 0.01	< 0.01	< 0.01	< 0.01	< 0.01
Current matching§ ($\Delta\% \pm 3\sigma$)	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1
Capacitor[1]							
Density (fF/μm^2)	2.5	3.5	4	5	7	10	14
Linearity (ppm/V)	≤ 200	≤ 200	≤ 200	≤ 200	≤ 200	≤ 200	≤ 200
Leakage (A/F)	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1
Matching ($\Delta\% \pm 3\sigma$)	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1	≤ 0.1
Q	≥ 15	≥ 25	≥ 30	≥ 35	≥ 40	≥ 40	≥ 40
Inductor							
Q	≥ 15	≥ 25	≥ 30	≥ 35	≥ 40	≥ 40	≥ 40
Signal Isolation							
S_{21} (db)[2]	≤ –120	≤ –120	≤ –120	≤ –120	≤ –120	≤ –120	≤ –120
Benchmark Circuits							
Gain (db)[3]	≥ 20	≥ 20	≥ 20	≥ 20	≥ 20	≥ 20	≥ 20
IIP3 (dbm)[3]	–6	–4	–3	–2.5	–1.5	–1	0
Noise (db) (Low noise Amp.)	2	1.5	1.3	1.2	0.9	0.7	0.5
Noise (db) (mixer)	5	4	3.5	3	2.5	2	1.5

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *Transistor type, bipolar or MOS, not explicit (It is expected that speed*power characteristics favor use of bipolar for $w_e \geq$ 180 nm. MOS speed*power may be favorable relative to bipolar at $L_{eff} \leq$ 180 nm.)*

** *Absolute current at which f_{max}, f_t, NF are measured, independent of device geometry*

*** *Maximum leakage for an embedded memory cell pass transistor (e.g., DRAM).*

§ *Matching specification assumes "near neighbor" devices at minimum practical separation.*

[1] *Analog filter implementations will drive density to $7fF/\mu m^2$. As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. MEMS implementation for filter applications may be favorable at density $\leq 7fF/\mu m^2$.*

Linearity, matching, and leakage requirements are driven by switched capacitor applications.

Q requirements are driven by coupling capacitor and voltage-variable capacitor (VVC) applications.

[2] *Signal isolation is best defined as the transmission efficiency (S21 in db) between a noise source and a noise sensor.*

Transient sensitivity (mV peak-to-peak) is also an important measure of signal isolation but is not quantified due to its dependence on layout and package.

[3] *Gain and IIP3 apply to both low noise amplifier and mixer benchmark circuits.*

Table 16 Short-flow Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Percent correlation of short-flow to full-flow process	20–40%	30–50%	40–60%	50–70%	60–80%	70–90%	80–100%
Relative complexity factor of required short-flow electrical parameters (i.e., V_t, I_d, R, C, etc.) (30–60% increase/generation)	1×	1.3–1.6×	1.7–2.6×	2.2–4.1×	2.9–6.6×	3.7–10.5×	4.8–16.8×
Relative complexity factor of required short-flow structural/material parameters (i.e., dimensions, concentrations, etc.) (10–20% increase/generation)	1×	1.1–1.2×	1.2–1.4×	1.3–1.7×	1.5–2.1×	1.6–2.5×	1.8–3.0×
Relative complexity factor of required short-flow yield/reliability parameters (i.e., defectivity, lifetime, etc.) (10–50% increase/generation)	1×	1.1–1.5×	1.2–2.3×	1.3–3.4×	1.5–5.1×	1.6–7.6×	1.8–11.4×
Relative complexity factor of required short-flow economic parameters (i.e., cost of ownership, etc.) (10–20% increase/generation)	1×	1.1–1.2×	1.2–1.4×	1.3–1.7×	1.5–2.1×	1.6–2.5×	1.8–3.0×
Relative % of TCAD/ECAD models calibratable using short-flow experiments	30–50	40–60	50–70	60–80	70–90	80–100	80–100
Linewidth measurement resolution (nm) (1% of minimum feature size)	2.5	1.8	1.5	1.3	1	0.7	0.5
Thin film measurement resolution (% of nominal film thickness)	1%	1%	1%	1%	1%	1%	1%
Defect measurement resolution (#/m^2) (1% of electrical defect density)	19	17	15	14	11	9	8
Reliability lifetime resolution (years)	± 10 yrs	± 10 yrs	10 yrs	± 1 yr	± 1 yr	± 0.1 yr	± 0.1 yr
Average short-flow process turn around time	1–3 days	1–3 days	1–3 days	0–2 days	0–2 days	0–1 day	0–1 day
Average number of required data points per short-flow parameter (4× increase/generation)	100–1000	400–4000	1600–16000	6400–64000	12800–128000	25600–256000	102400–1024000
Average time required for short-flow (4× increase per generation) data analysis and modeling	0–60 minutes	0–60 minutes	0–60 minutes	0–10 minutes	0–10 minutes	0–1 minutes	0–1 minutes
Percent reusability of short-flow experiments and analysis techniques	80%–90%	80%–90%	80%–90%	80%–90%	90%–100%	90%–100%	90%–100%

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Table 17 Reliability Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Quality and Reliability Customer Requirements							
Quality (dpm)	3–500	0.1–500	0.1–500	0.1–500	0.1–500	0.1–500	0.1–500
EL (dpm)*	50–2800	5–2800	5–2800	5–2800	5–2800	5–2800	5–2800
EOL (FITs)**	3–700	1–500	1–500	1–500	1–500	1–500	1–500
EOL (FITs)	1–10	0.1					
Communications Market							
TDDB (FITs)		0.5		0.5	0.5	0.5	0.5
Electromigration (FITs)		0.5–1.0	0.5–1.0	0.5–1.0	0.5–1.0	0.5–1.0	
Product/Process Requirements							
@ 60% yield defect density (d/square m)	1940	1710	1510	1355	1120	940	775
A (square cm)	3	3.4	3.9	4.3	5.2	6.2	7.5
Yield defect/chip	0.58	0.55	0.61	0.58	0.58	0.58	0.58
EL (dpm) (Y.D./100)	5800	5500	6100	5800	5800	5800	5800
EL (dpm) (Y.D./500)	1168	1100	1220	1168	1168	1168	1168
Scaled maximum current density (A/sq.cm.)	6×10^5	9×10^5	1.5×10^6	3×10^6	8×10^6	2×10^7	2×10^7
Al limit	1×10^6	1×10^6	1×10^6	1×10^6	1×10^6	1×10^6	1×10^6
Cu limit	1×10^7	1×10^7	1×10^7	1×10^7	1×10^7	1×10^7	1×10^7
F/A cycle time (days)—outlook	3–20	5–25	7–27	8–30	8–30	8–30	8–30
F/A cycle time (days)—requirement	3–20	2–16	1–12	1–10	1–10	1–10	1–10

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *EL=1 year at 85°C*
** *EOL = 10 years at 85°C*
*** *EOL, Communications = 25 years at 85°C*

MEMORY AND LOGIC

The technology requirements table reflects the needs of high-performance products. Physical gate lengths, gate dielectrics, and junction depths are all being aggressively scaled to meet this requirement. To support the smaller physical gate lengths, power supply voltages are also decreasing. It will be a significant challenge to maintain constant drive current as the power supply voltage is reduced. The off-state leakage current is also increasing to meet the drive current and performance targets. The higher leakage current will present challenges for defect screening. The gate dielectric requirements for these transistors quickly reaches a thickness where tunneling currents will be significant. Gate oxide leakage current is assumed to be less than the transistor off current. Alternate dielectric materials may be required. For the shallow S/D extension junction requirements, the need will depend on the drain engineering that is used. With pocket implants it is possible to use deeper junctions. Short wire pitch requirements depend on the application. Memory cells will need a short wire pitch that is ~2× the minimum feature size whereas logic will require ~3×. The metal system must be optimized to minimize RC delay and meet the electromigration and stress migration requirements. Electrostatic discharge (ESD) protection coupled with high speed, scaled I/O's present a challenge in device optimization.

Projections for DRAM cell size scaling quickly reach the point where current approaches cannot meet the requirements. This will drive a change in material, cell design, and memory architecture. Data retention and soft error specs will be extremely difficult to achieve in these smaller cells.

Future SOCs will require integration of logic, analog, and memory on the same chip at low power supply voltages. Integration of these technologies will be a major challenge to satisfy the requirements of each technology. For these highly integrated systems, new testing methodologies will be needed to overcome the testing complexity. Crosstalk and signal integrity problems have been pushed by scaling

of the metal system into a regime where technology alone cannot provide the solution. Intelligent design of signal routing will be a requirement.

ANALOG, MIXED SIGNAL, AND RF

Analog integration is more easily implemented when there are mutual benefits with logic and memory for all new processes. Some mutually anticipated new processes are: SOI multi-value/multi-V_t devices, nonvolatile memory (NVM), and inherently self–X (ISX), where desirable 'X' includes adaptive matching, for example. Necessary power supply enhancements for logic, memory, and analog are "star" distribution systems with low feeder resistances and high κ bypass capacitors.

Analog and RF circuits for mainstream wireless and computation applications will operate at increasingly higher frequencies, well above today's 900 MHz range. Precision matching of devices, such as current matching and capacitor matching, places stringent requirements on technologies for high-performance analog and mixed signal applications. Gate oxide and capacitor leakage current guidelines for high-performance mixed signal circuits are smaller than the leakage of junctions connected to them. The leakage current guidelines for nonvolatile memories are several orders of magnitude smaller. Enhancement of signal to noise ratio is addressed in the difficult challenges table.

SHORT-FLOW

Short-flow and DFX methodologies address the fundamental problem of how to minimize the growing cost of acquiring the information needed to characterize and model comprehensively a full-flow process. Short-flow experiments are designed to obtain the desired electrical, structural, manufacturing, reliability, or economic information from key process modules. A properly designed short-flow experiment will characterize and model the principal interactions between the selected module and the rest of the full flow.

Successful short-flow experiments must address the following issues:

- The number of short-flow parameters that need to be measured to achieve high correlation with full-flow processes is expected to scale with increasing process complexity and wafer size.
- Along with increased demands on metrological tool resolution that scale with minimum feature size and film thickness, short-flow experiments will require major improvements in metrological tool data volume, feedback time, and cost per measurement.
- Major improvements in the statistical data analysis and modeling techniques as well as in the factory data handling infrastructure will be required to enable the real time processing of the short-flow data.
- Short-flow experiments and analysis techniques must be reusable and scalable with technology.

RELIABILITY

There are a variety of need levels in future reliability requirements. After steadily improving for years, reliability levels, specified as failures in time (FITs) per device, have essentially been flat since 1994. Some market segments can live with flat reliability levels in the near term, while other market segments require continuous improvements. Even to retain, much less improve, the existing level of reliability, the introduction of the new process/material sets will need to be free of unresolved reliability issues and at defect densities capable of supporting yield and reliability objectives. Plan yields and defect densities for first year of production in the 1997 NTRS will cause an increase in failure rates, but will return to the projected customer failure rate requirements by the third year. The electromigration current density limitations of Cu becomes an issue at the 70 nm technology generation. Current estimates of diagnostics and failure analysis turn-around times for future technologies will be longer unless revolutionary new tools and techniques are developed.

POTENTIAL SOLUTIONS

Potential solutions for PIDS are shown in Figures 10 through 13.

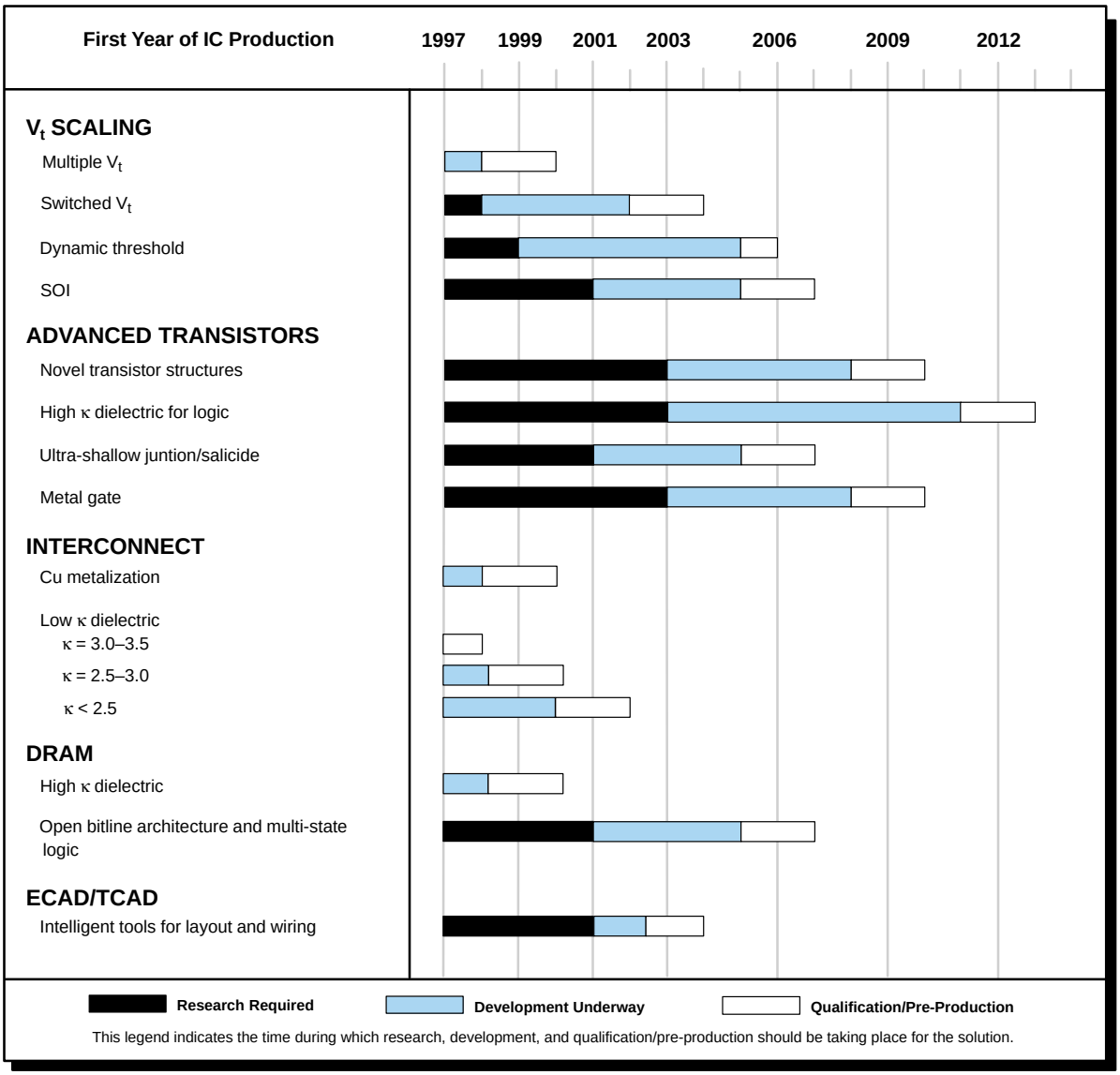


Figure 10 Memory and Logic Potential Solutions

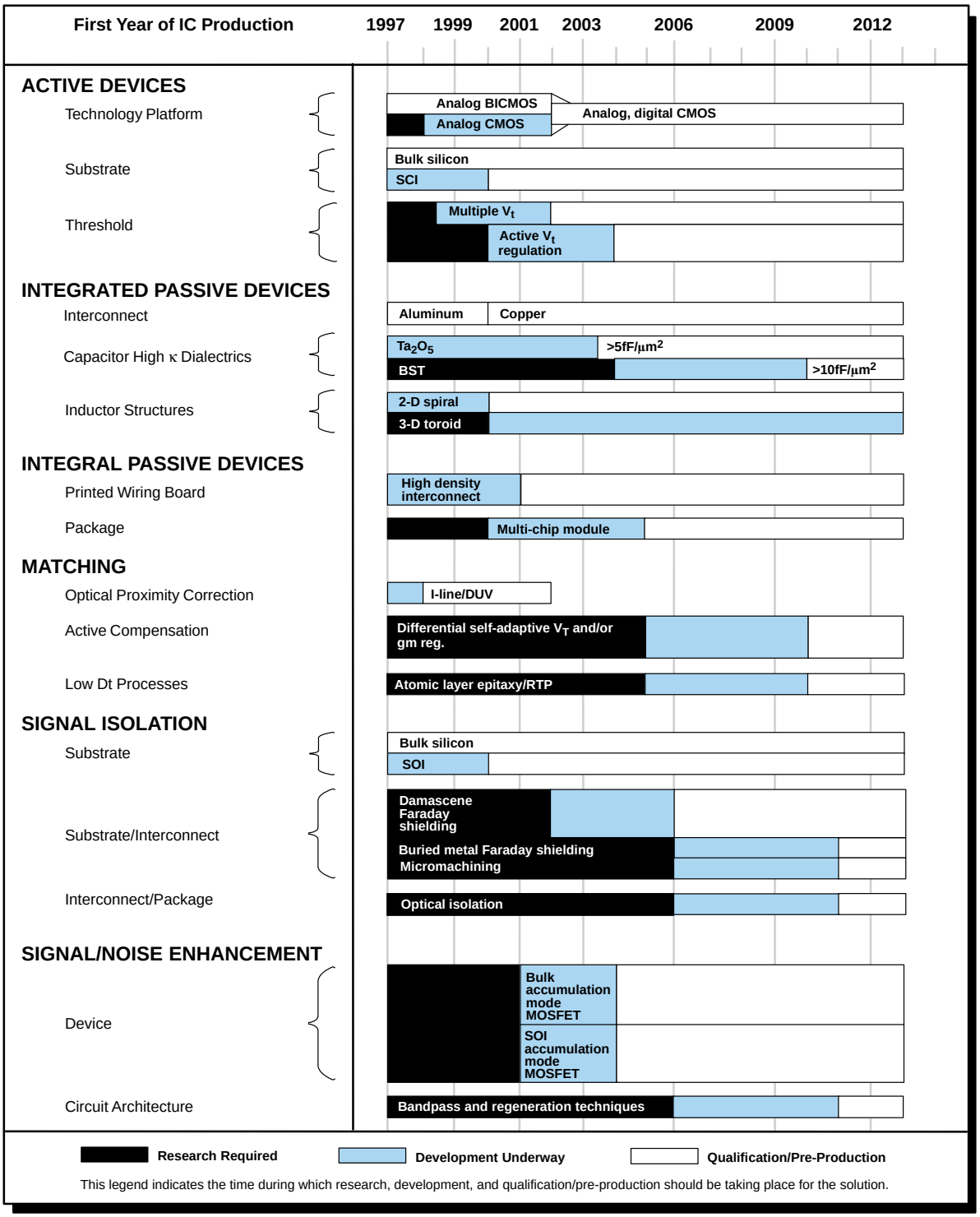


Figure 11 Analog, Mixed Signal, and RF Potential Solutions

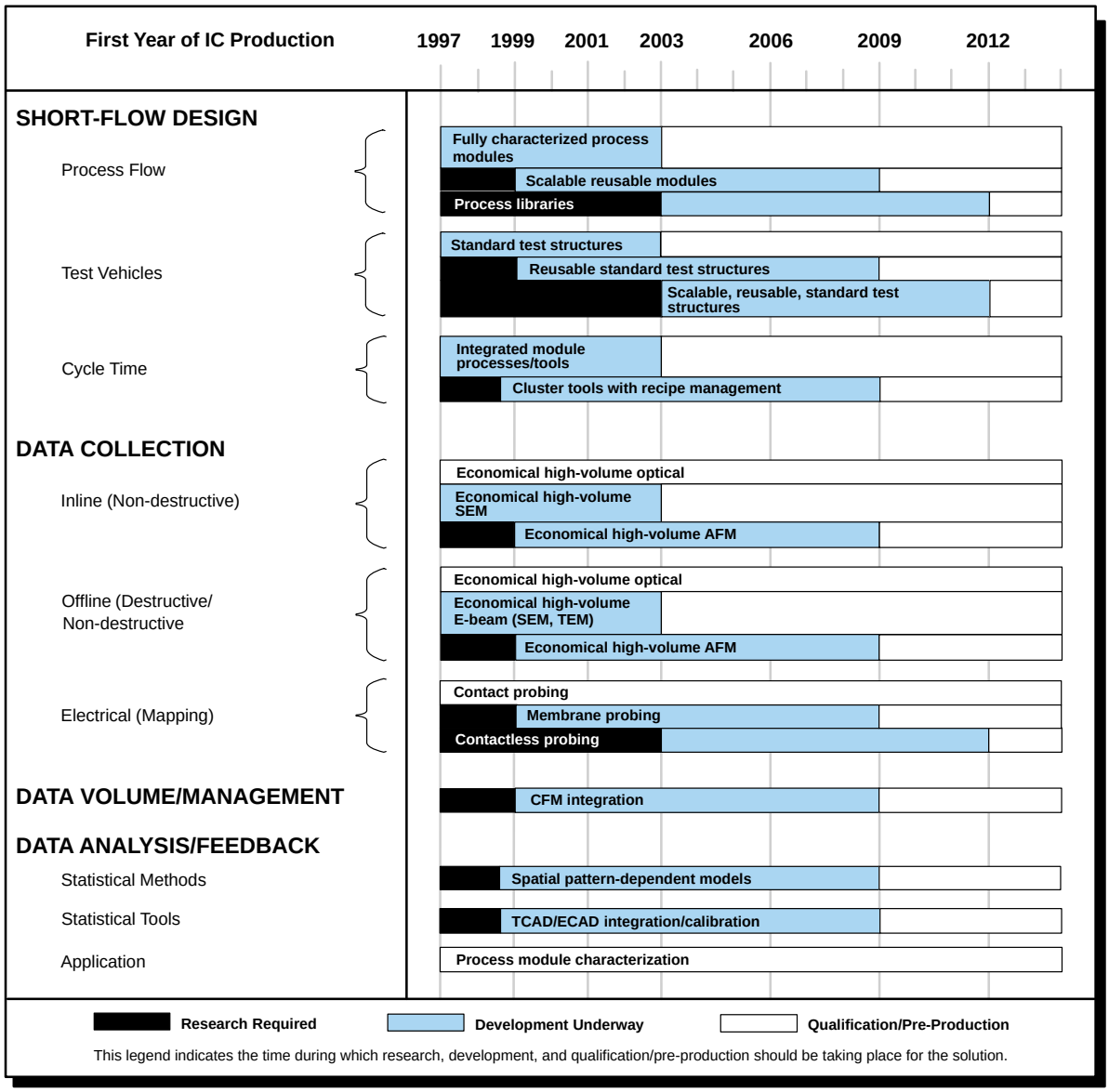
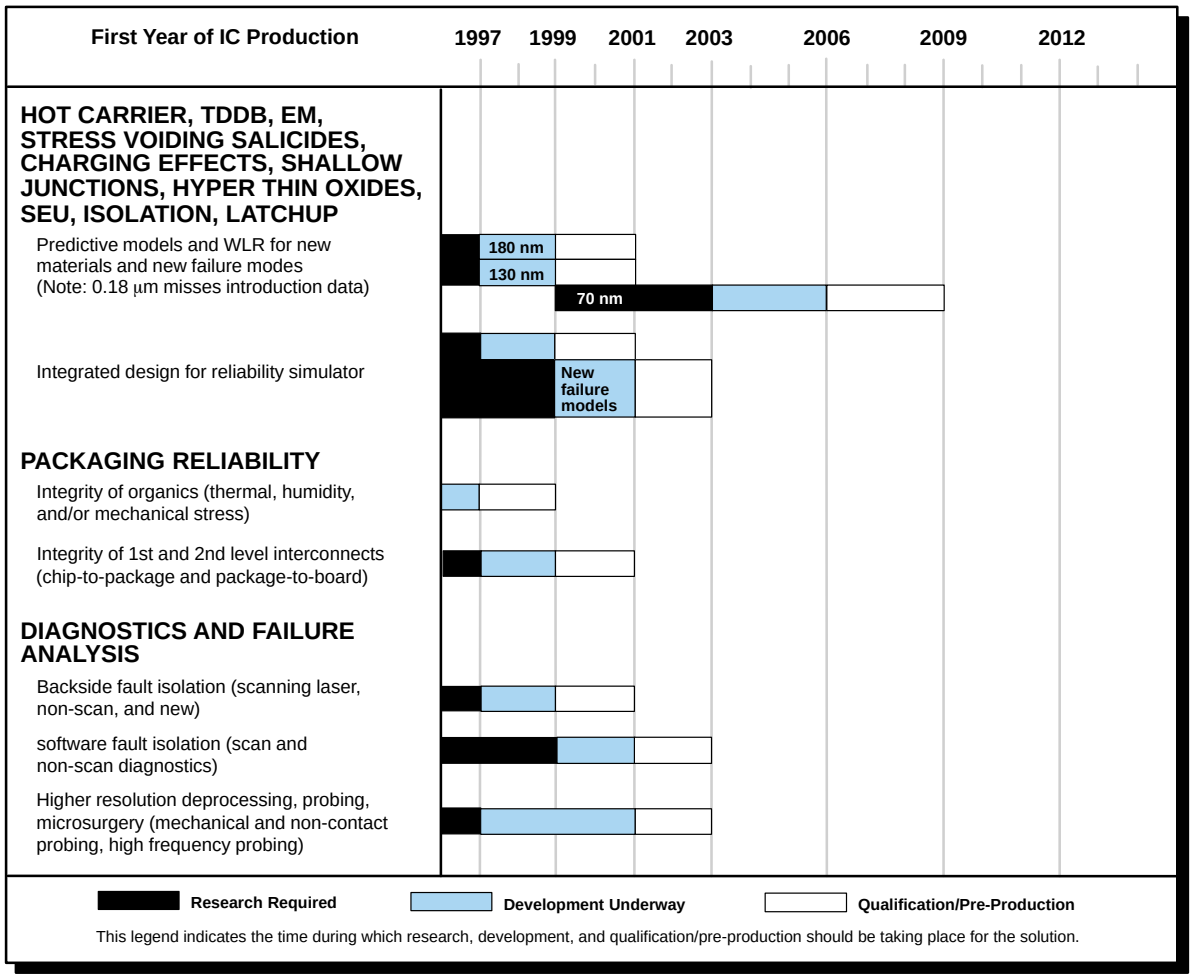


Figure 12 Short-flow Potential Solutions



SEU—single event upset

Figure 13 Reliability Potential Solutions

MEMORY AND LOGIC

With lower power supply voltages, achieving high-performance and low leakage will be very difficult. Scaling and control of threshold voltages will be a requirement. Multiple threshold voltages on the chip, switching threshold voltage by well bias, or dynamic threshold where the threshold voltage changes with gate bias are all potential solutions for low standby power. SOI presents some key attributes to address these issues in terms of reduced parasitic capacitance and improved device performance. There are a variety of SOI options that may also lead to 3-D stacking. Scaled transistors will require new materials such as high κ gate dielectrics to minimize tunneling currents, low resistance gate conductors such as metal gates, and ultra-shallow source/drain junctions. Process variability and lack of improvement in lithography tolerances will drive the need for new transistor structures. This can include advanced structures such as inherently self-aligned and feature-size regulated structures. To reduce RC delay and improve reliability, Cu metallization is being pursued. The increase in interconnect capacitance is being addressed by the integration of low κ dielectrics into the metal system. There are many material options with a spectrum of dielectric constants that are potential solutions. DRAM cell size scaling will drive the incorporation of high κ dielectrics for the storage capacitor in addition to new cell designs and architectures such as open bitline or multilevel storage for DRAMs.

To be able to develop and design the complex, highly integrated circuits of the future, improved CAD and modeling tools will be required to be able to deal effectively with problems such as crosstalk. Currently, distribution of power, ground, and clock is consuming an increasing percentage of the

available interconnect resources. Novel interconnect architectures at the chip-functional block level will be required for future circuits.

ANALOG, MIXED SIGNAL, AND RF

Potential solutions for analog are those that extend beyond or exclude memory and logic. Because successful analog technologies will leverage off digital, meeting the unique analog requirements will determine success. Two major issues that will continue to set analog apart from digital are the integration of passive components and the degree of signal isolation. In addition, matching requirements are severe for analog and exceed those for digital.

It is expected that, as the speed-power product of CMOS increases, the technology will replace BiCMOS and bipolar at around 180 nm (2000). Portable communications products lead the drive for low power (battery life). Active devices fabricated in SOI will be key in achieving low parasitic capacitance (low current).

The power supply trend for analog design is expected to follow that of digital. Near term, DC–DC conversion will provide needed headroom at the expense of higher power consumption. Long term, it is expected that low threshold, high gain CMOS devices will replace large geometry, low V_{be} bipolars in true sub-1.5V designs. Ultimately, full-digital implementations in CMOS will replace most analog designs.

Very low resistance metal interconnects are required for high Q integrated passives. New high κ dielectrics are needed to reduce the area of integrated capacitors. Alternatively, some passives may also be integrated into the printed wiring board or package as a method of cost reduction/simplification. The need for low loss, high Q inductors may justify use of 3-D or micromachined structures.

Precise active and passive device matching will be achieved through fabrication techniques such as optical proximity correction (OPC) and low D_t processes. Circuit design techniques such as active compensation will be utilized for matching control.

Protection of noise sensitive analog circuits from “noisy” digital circuits will become increasingly difficult as frequency of operation rises. Signal isolation is managed through a combination of substrate, interconnect, and package solutions. Near term, circuit blocks may be protected with oxide isolation and guard rings. Integrated shielding structures are required for protection of circuits and interconnects. Innovative optical and micromachining techniques may be employed as solutions in the future. Novel device structures and design architectures may be employed to enhance circuit signal/noise. Any cost-effective solution addressing these problems must be compatible with the mainstream CMOS technology of the time.

SHORT-FLOW

Effective and executable short-flow experiments will require standardized, scalable, reusable test structures along with the corresponding metrological and data analysis/modeling capability. The need to identify increasing numbers of key short-flow parameters to specify the major short-flow/full-flow interactions will drive towards more comprehensive process module characterization, leading to fully characterized process libraries. Integrated cluster tools will be needed to meet the cycle time requirements for future short-flow experiments.

The need to collect efficiently the large amount of required short-flow data will necessitate existing and future metrological techniques to shorten measurement times and reduce costs per measurement. Novel schemes for contactless electrical probing may also have an impact. Data analysis and modeling techniques along with the associated computational infrastructure will be needed to enable rapid short-flow model generation.

RELIABILITY

Below 180 nm, the key reliability issues will be the quality of very thin gate oxides and very shallow junctions, hot carrier reliability, and adequate protection against latch-up or ESD failures.

At 100 nm T_{ox} is expected to scale to about 2.0 nm. For thin nitrided oxide a key challenge will be understanding the mechanisms of basic oxide conduction and reliability wearout failure potential. Plasma induced damage will become more severe as the oxide thickness scales (until the thin oxides become resistive) and back end of line (BEOL) processing becomes more complex from added metal levels. Tunneling current will increase for "hyper" thin oxides and the impact on oxide reliability needs to be investigated.

The introduction of Cu and low κ dielectrics will bring the possibility of new failure modes. Electromigration characteristics improve with the introduction of Cu, but will need further improvement by 70 nm. Resistive contact vias will be a significant challenge as the number of vias is scaled and will require process perfection. Integration of updated reliability models into global TCAD tools that have predictive capability for device, process, reliability, and circuit design simulation has lacked progress and continues as a difficult challenge.

Reliability test and measurement will need to change as follows:

- from the IC to test structures (single device serial test to multi device parallel test)
- from DC to AC (measuring failures to measuring failure predictors)
- from packaged part to wafer (burn-in reliance to test, measurement, and WLR)

Achieving aggressive technology learning curves will be dependent upon diagnostics and failure analysis capabilities. Revolutionary advances in tools and techniques will be necessary to maintain even the basic ability to do failure analysis. Keeping costs and cycle times at reasonable levels will prove an even greater challenge. Area array I/O and flip chip packaging will drive the need for back-side fault isolation and software localization tools. Scaling will drive the need for smaller, higher resolution inspection tools (e.g., scanning electron microscopy [SEM] or scanning probe microscopy [SPM]) and smaller, high resolution probing techniques, both AC and DC. Multi level metals will drive the need for new deprocessing and microsurgical tools.

CROSSCUT NEEDS

DEFECT REDUCTION

As the scale of integration advances, the complexities of the manufacturing technologies and associated processes and materials will increase greatly. Radically different processes and new materials are to be introduced to continue the advance of the technology. These, coupled with the increase in interconnect layers, are sure to increase the difficulty of both defect detection and sourcing. Also, interprocess interactions will become critical, complex, and play a more significant role in defect generation. At the same time, the requirement for reduction in defect density to achieve acceptable yields and reliability, as shown in Table 58, "Defect Sources and Mechanisms", in the *Defect Reduction* section, will accelerate the demands on defect reduction technology. When coupled with the heightened requirements on purity of materials, these will demand tighter coupling and innovative aids from the process integration and device structure community.

Similarly, to accelerate cycles of learning within increasing cost pressures, defect sourcing in the context of the defect sourcing complexities will need predictive and diagnostic structures that can be used with conventional techniques. The advance of defect reduction technology will require device test structures in the following areas: 1) input materials such as water and chemicals; 2) inline test structures to detect very small levels of contaminants; 3) structures to aid in diagnosis/sourcing of invisible defects (defects with no visible physical remnant or are created in sublevels that become increasingly inaccessible by more conventional detection means); 4) electrical detection and/or screens for yield and reliability failure modes associated with the new processes and materials; and 5) predictive wafer level reliability test structures for pieces of the architectures of the IC technologies and associated modeling. These structures can be categorized into four areas—a) input materials,

b) transistor structures, c) interconnect, and d) yield enhancement systems and associated structures. Table 18 indicates the timeframe research and/or development is necessary to address issues in these areas.

Table 18 Process Integration Defect Reduction Needs

ISSUES	POTENTIAL SOLUTIONS		
	1–5 YEARS	5–10 YEARS	10–15 YEARS
Input Materials			
Water and chemical purity		Test structures and models for trace impurities	
Transistor Structure			
Substrate defectivity—Si		Improved electrical capability	
Substrate defectivity—SOI		Detection capability	
In-trench contamination	Early detection of trench contamination that can lead to electro-migration problems		
Localized gate oxide and field oxide defects (e. g., ionic contamination, charging effects)			Detection capability
Localized depletion effects in poly gates	Detection capability		
Dielectric and diode integrity	Electrical effects of thin film residues		
Single event upset	Detection capability		
Interconnect			
In-contact and in-via contamination (local)	Isolation and early detection of individual bad contacts		
Copper barrier metal integrity (local)	Detection capability		
Dielectric constant variation—vertical	Multi-layer measurement capability in stacked, planarized films		
Dielectric constant variant—horizontal	Measurement capability between metal lines		
Stringers—conductive leakage paths	Improved low-level leakage capability		
Electromigration		Predictive test structures/ tests	
Yield Enhancement			
Feed-forward/process zones (predictive)		Test structures/tests	
Feed-forward/full process (predictive)		Test structures/tests	
Feedback (analysis)		Test structures/tests	

METROLOGY

Physical metrology will be increasingly challenged by the need to provide process control that results in acceptable electrical performance. Physical variables such as gate dielectric thickness, gate electrode length, spacer width, and the 3-D dopant profile interact to provide the electrical properties of the transistor such as threshold voltage, off-current, and effective gate length. Metrology must have the resolution and precision (short term repeatability and long term reproducibility) to measure shrinking tolerances of electrical properties. The interaction of physical variables often results in tighter

tolerances; for example, ineffective overlay measurement and variations in the source/drain profile alignment with the gate electrode can greatly affect switching speed. Future requirements for metrology tool capability should be guided by device and circuit modeling of the manufacturing variation sensitivities of transistors. Characterization of failed test structures requires improved materials characterization tools such as focused ion beam (FIB) systems.

Process integration relies on verification of transistor and interconnect structures using transmission electron microscopy and immersion lens scanning electron microscopy. More rapid sample preparation is required for reducing the cycle time for process development and yield learning. Focused ion beam systems equipped with precision sample stages and scanning electron microscopes are already improving the quality of cross-sectioned samples and reducing cycle time. Despite this progress, additional improvements in sample preparation are required.

Efficient process transfer is a key need for rapid ramping of new factories. Reference materials for metrology tools that measure critical dimensions, dopant concentration, and oxide thickness are examples of critical factors that must be reproduced when processes are transferred between sites or from process tool supplier to fabrication site. Databases with local and reference information will greatly improve data management.

Physical and electrical measurements are required for implementation of statistical metrology. Test structures have been developed for the purpose of evaluation of stress in interconnect structures and the measurement of electromigration. Some of these test structures can be MEMS fabricated using traditional silicon process technologies. Further development of these prototype MEMS structures may be useful for evaluation of copper metalization and new interconnect dielectric materials.

The verification of TCAD models that will be used for simulation of the formation of 3-D dopant profiles for future device geometries requires considerable improvements in the physical characterization methods. The metrology roadmap states spatial resolution requirements for 2- or 3-D dopant profiles and dopant concentration precision for profile measurements. Physical characterization is challenged by the statistical fluctuations in dopant density that occur when low dose doping is used. Characterization of ultrashallow junctions using large area by secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) has been reported. Development, transfer, and control of doping processes requires careful attention to appropriate analysis conditions and reproduction of these conditions. Characterization of test structures for sub 100 nm doping processes will require improved SIMS and SRP. Although scanning capacitance microscopy characterization of 2-D dopant profiles in transistors has been demonstrated, considerable further development is required. High resolution images of etched cross-sections also provide 2-D dopant profiling. Improvements in existing physical characterization need to keep pace with shrinking junctions and changing profiles. A breakthrough in physical characterization is necessary for 2-D dopant profiling of sub-100 nm transistor cross-sections. Device simulations are useful indications of requirements for spatial resolution and precision of dopant concentration analysis.

FRONT END PROCESSES

SCOPE

The Front End Processes (FEP) Roadmap covers the key process areas in the front-end-of-line (FEOL) wafer fabrication processing of integrated circuits and includes the tools and processes used to fabricate device structures from the starting silicon material through the silicidation process. The focus areas covered in the FEP section include: *Starting Materials*, *Surface Preparation*, *Thermal/Thin Films and Doping*, and *Front End Plasma Etch*.

A review of the requirements and potential solutions will be covered for each focus topic. The targets and trends shown in the requirements tables are model-based unless otherwise noted. Potential solutions are known examples of possible solutions and should not be considered as the only approaches; innovative new solutions are desired.

Related topics for front end processes are presented in other sections of this Roadmap. The tool-related issues for plasma etch and chemical mechanical polish (CMP) for trench isolation are covered in the *Interconnect* section rather than in this FEP section because of their overlap with back-end-of-line (BEOL) tool issues. The FEP roadmap includes the processing issues as well as future requirements for plasma etch and CMP processing related to FEOL device fabrication. The crosscut needs of FEP will be covered in the following sections: *Defect Reduction; Metrology; Environment, Safety, & Health*; and *Modeling & Simulation*.

DIFFICULT CHALLENGES

Front end processes are critical to the overall device performance requirements and continued CMOS device scaling. Most difficult challenges are shown in Table 19. Transistor performance is determined primarily by three parameters: gate length, gate dielectric thickness, and junction depth. To date, primary attention has been placed in scaling gate length that is limited by lithography and etch. Future scaling will be limited by the ability to scale the vertical dimensions as well as the horizontal dimensions. Although there are many challenges facing front end processing there do not appear to be fundamental limits on device scaling to the 100 nm technology generation. However, due to fundamental limits such as tunneling currents, scaling bulk CMOS devices beyond 100 nm will require new materials for the gate dielectric (high κ) and gate electrode (metals) as well as new device structures, such as fully depleted silicon on insulator (SOI) and elevated source/drain structures. These are critical *showstoppers* if not solved. One should note that the high-κ gate materials needs may be able to leverage current research on DRAM high-κ capacitor dielectric materials. In addition, new technologies must be developed to form highly doped and abrupt layer profiles. Ultra-low thermal budgets will be required to limit diffusion at the expense of activating dopants and process damage removal. Interfacial layers will have more influence over device performance that will require reduced and stricter control of contamination and defect levels leading to increased utilization of *in situ*, single-wafer processing, and clustering. The ability to grow affordable 450 mm diameter and larger wafers of the quality required is uncertain. As an alternative, new substrate approaches might be pursued. Continued scaling beyond 100 nm, as projected in this Roadmap, cannot be achieved unless the critical challenges as outlined in Table 19 are solved in a timely manner. Increased attention and resources are required to meet these challenges.

Table 19 Front End Processes Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Gate dielectric scaling (including surface preparation)	Issues of scaling gate dielectric to below 2 nm are control of tunneling currents, boron out-diffusion and gate dielectric penetration, and charge-induced damage.
Channel engineering for optimized performance (V_t control)	Channel doping must increase to minimize short channel behavior: Maximize drive current.
Junction scaling with low resistance contacts	Producing highly doped and fully activated shallow junctions contacted with low sheet resistance materials will challenge the silicide process and the allowable thermal budget.
CoO of silicon materials quality (polished/Epi wafers)	Distinguishing particles, microroughness and silicon micro-defects for front/back-surfaces with improved understanding and control of both grown-in micro-defects and the wafer-carrier interaction, and subsequent impact on relevant device characteristics
Ambient control—interface control	Control of the interface and processing ambient are essential to low defect density processes for the FEOL, particularly for sub-3 nm gates.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Alternate materials for gate dielectric	The phase out of SiO_2 and identification of a gate-quality alternative high κ dielectric is required.
Alternative to bulk CMOS (e.g., dual gate, fully depleted SOI)	Increased channel dopant concentration will ultimately limit drive currents and may require new device structures
Elevated source/drain (e.g., sidewall spacers, selective silicide/Epi)	The need for lower sheet resistance and minimum silicon consumption requires new structures like elevated source/drain.
CoO for starting materials production (450 mm, 675 mm, SOI)	Methodology for fabricating silicon for the 64 Gbit DRAM era (450 mm and 675 mm wafers) as compared to the effective introduction of SOI and IC processing of wafers.
Alternate gate electrode (including etch issues)	Alternate gate electrode materials will be required to alleviate problems of poly depletion, high resistivity, and to achieve acceptable threshold voltages. Etching of these new gate stacks presents new challenges.

STARTING MATERIALS

The selection of starting materials involves choosing either Czochralski (CZ) polished or epitaxial silicon wafers. Silicon-on-insulator (SOI) materials may also become more than a niche technology for possibly 130 nm and beyond. Memory circuits are commonly manufactured on CZ polished wafers because of lower cost. Logic ICs are generally manufactured on higher cost epitaxial wafers because of their greater robustness during IC fabrication and latch-up suppression capability. The reduction of the price ratio of epitaxial to polished wafers, anticipated to reach approximately 1.5 or less for 300 mm wafers, favors continued use of epitaxial wafers, consistent with the declining fixed cost-of-ownership (CoO) for single wafer epitaxial reactors.

General characteristics and specific polished, epitaxial and SOI IC wafer requirements, after removal from the package, represent upper limit values corresponding to the allocated yield budget to ensure 99% yield for each parameter in Table 20. Since the parameters are statistically independent, these upper limit values would rarely coincide for more than one parameter. The median value for each parameter would be much better than the listed value, thereby ensuring the total yield for all parameters was at least 99%. The parameters are derived from model-based analysis based on CDs, bits, wafer size, etc., rather than extrapolation of trends or anecdotal inputs. However, understanding the

underlying models of parameter relationships may be more important than the numerical values themselves. The uniformity of all wafer parameters is critical, although the required tolerance is noted only for a few parameters, such as oxygen.

It is essential to balance the "best wafer possible" against the CoO opportunity of not driving silicon requirements to the detection limit but to some less stringent and optimized value. Therefore, the surface metals and particle trends are less stringent than the pre-gate values (see *Surface Preparation* section). Accordingly, the starting materials values represent the perceived critical material characteristics required to ensure that silicon materials support the continued growth of the industry. The CoO for wafer cleaning is especially important since the wafer supplier performs a final clean and the IC manufacturer often performs an incoming clean. The chemical structure of the wafer surface produced and delivered by the wafer supplier (hydrophobic versus hydrophilic) is a critical issue as is the wafer-carrier interaction in controlling the subsequent adsorption of metals, ionics, organics, and particles on the wafer surface.

The physical structure of the silicon surface has also emerged as a critical concern. Both polished and epitaxial surfaces exhibit defects that must be controlled to achieve high yielding ICs. These defects include particles, shallow pits, surface microroughness, residual polishing micro-damage, grown-in micro-defects such as crystal originated pits (COPs), surface chemical residues including organics, and structural defects such as epitaxial stacking faults.

Additionally, the wafer back-surface is increasingly being prepared with a shiny or polished finish to enhance the distinguishing of particles and crystal micro-defects from microroughness for Ultra Large Scale Integration (ULSI) cleanliness requirements (*see Metrology Roadmap* section) and to improve the uniformity of monitoring the wafer temperature during IC processes. The improvement in back-surface cleanliness more readily exhibits microscopic contamination and handling scratch damage from robotic handling systems. Standards for robotic handlers may be necessary to ensure conformance of the surface to the implicit cleanliness requirements. The measurement, counting, composition, morphology, removal, and prevention of surface defects is a state-of-the-art challenge in silicon wafer technology as is the development of laser scanning and other instrumentation utilized to monitor these defects.

Material Uniformity and Process Distributions—To control wafer-to-wafer and within-wafer variations, process-induced parameter distributions must become narrower. A number of critical wafer parameters can be described by a two-parameter distribution. Data symmetrically distributed about a central value can be described by a normal distribution, defined by the value ± tolerance at a specified (negotiated) parts per million (ppm) quality level. Asymmetrically distributed characteristics with a desired value of zero, typical of most defects such as particles and surface metals, exhibit long tails and can frequently be described by a log-normal distribution defined by an upper specification limit at a negotiated ppm quality level. If experimentally based data or models indicate that several parameters are mutually constrained, then these several parameters should be partitioned to ensure an overall effective yield of 99%.

Parameter distributions could also be utilized as materials acceptance criteria at IC companies. This method would alleviate the challenge of separating measurement variability from the true parameter variability that is becoming more difficult as the values for many parameters are approaching detection or resolution limits. Use of parameter distributions established by wafer suppliers for their processes to demonstrate that an ensemble of wafers will be satisfactory for the intended purpose will require improvements in both process capabilities and a significant paradigm shift in IC materials acceptance practices. Currently available models cannot sufficiently establish the real requirements for parameter uniformity or the effects of parameter variability on IC properties; the requirements in Table 20 do not adequately address either of these issues and development of such models is encouraged to enhance the utility of future Roadmaps.

Polished Wafer—The formation of uncontrolled SiO_x precipitates may result in excessive device leakage current, necessitating the optimization of oxygen internal gettering in polished wafers. The magnitude and uniformity requirements for oxygen, as well as dopants, may require the utilization of magnetic Czochralski (MCZ) silicon, especially for 300 mm and larger diameter wafers.

The dependence of gate oxide integrity (GOI) on the crystal growth parameters and the related role of point defects and agglomerates such as COPs and SiO_x precipitates has been extensively documented. Currently manufactured vacancy-rich material can result in GOI failures in sub-10 nm oxides due to the agglomeration of vacancies (COPs) into macroscopic voids and related structural defects. This leads to thinning of the gate oxide as well as other intermediate structures. Hydrogen or argon thermal annealing can reduce the near-surface COP density and improve the GOI. Tuning the crystal growth parameters to form interstitial-rich material also improves GOI, although IC DRAM yield may decrease.

The IC degradation may occur because the IC processes presently used were developed for vacancy-rich material and may not be optimal for interstitial-rich material for the same IC process conditions. The interstitials enhance the formation of interstitial dislocation loops which, if decorated with residual metallics, can degrade IC performance and yield. Therefore, the IC DRAM process flow may need to be re-engineered, in partnership with the silicon supplier, to ensure compatibility with the improved crystal growth processes developed to minimize the formation of point defect clusters.

Epitaxial Wafer—The improved GOI in epitaxial material is due to the improved structural perfection of epitaxial material as compared to residual polishing micro-damage and grown-in micro-defects in polished wafers. Surface microroughness excursions may become more significant in degrading device performance as the gate dielectric thickness approaches a few unit cells. The utilization of p/p^- material with H_2 or argon annealed substrates for advanced ICs is also receiving attention. The benefit of both epitaxial surface quality and reduced system capacitance may offset the lack of enhanced solubility gettering of Fe in p^-, compared with conventional p^+ epitaxial substrates.

If significant benefits are perceived and implemented, the IC industry will successfully cope with the absence of solubility enhanced gettering. The oxygen content, however, may have to be re-assessed since oxygen precipitates slower in p^- compared to p^+ material. Back-surface polysilicon gettering may become more fully utilized, in conjunction with the general reduction of the oxygen content, in both epitaxial substrates and polished wafers. Selection of the gettering system, however, is very dependent on the IC thermal process sequence. The role of MeV implantation and associated annealing procedures in polished wafers as a replacement for epitaxial structures continues to receive attention, although the control of COPs and related defects will be aggravated in polished wafers. However, the use of MeV implant/thermal anneal procedures, in conjunction with epitaxial wafers, has been proposed to achieve enhanced device architectures.

Silicon-on-Insulator Wafer—SOI obviates the concern about latch-up while offering the potential for improved device performance, soft error immunity, low power applications, fewer process steps, presumably smaller chip size, and the opportunity of utilizing the previous generation's factory equipment to achieve the required number of chips per wafer. Evaluation of the various SOI wafer fabrication techniques by material characterization and identification of the relationships between defects and SOI properties such as gettering and the effective recombination lifetime on subsequent device properties is essential. The small SOI supplier base impacts the cost structure although different SOI approaches may be necessary to service different IC applications. Some bulk IC designs can be directly transferred to SOI. Process and mask redesign may further improve performance and chip size. However, SOI applications may be limited until conventional silicon materials reach a technological or economic wall, perhaps 130 nm and beyond.

Large Diameter Wafer—The conversion to 300 mm diameter wafers, beginning about 1998–1999 with peak conversion about 2001–2002, is necessary to achieve the required economy of scale for large volume IC manufacturing. International cooperation and standardization of wafers, carriers, and factory protocol are critical for achieving this conversion in a cost-effective and timely manner. Business issues are the primary migration concern as it appears the engineering issues associated with cost-effective crystal growth and wafer gravitational stresses can be addressed.

Projections of the wafer diameter beyond 300 mm suggest 450 mm (followed by 675 mm) may be the appropriate next sizes. A doubling of the wafer area maintains the historical productivity enhancement growth rate. Implementation of research in 2006 to drive the 675 mm wafer (approximately one mm thick), including gravitational stresses and related equipment platform issues, appears warranted to ensure its implementation in approximately 2018, as noted in the potential solutions roadmap in Figure 14.

The engineering issues associated with these diameters, however, appear to be enormous and a paradigm shift in approaching the fabrication of cost-effective silicon materials, including the cost-effective introduction of SOI, is required. The fabrication of silicon materials on an appropriate substrate rather than grinding off approximately 50% of the wafer volume to ensure conformance with IC package dimensions could help mitigate the escalating costs associated with conventional silicon materials.

Table 20 Starting Materials Technology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
*General Characteristics * (A,B)*							
Wafer diameter (mm)	200	300	300	300	300	450	450
Critical surface metals (at/cm^2) (C,D)	$\leq 2.5 \times 10^{10}$	$\leq 1.3 \times 10^{10}$	$\leq 1 \times 10^{10}$	$\leq 7.5 \times 10^{9}$	$\leq 5 \times 10^{9}$	$\leq 2.5 \times 10^{9}$	$\leq 2.5 \times 10^{9}$
Other surface metals (at/cm^2) (C,E)	$\leq 1 \times 10^{11}$	$\leq 1 \times 10^{11}$	$\leq 1 \times 10^{11}$	$\leq 1 \times 10^{11}$	$\leq 1 \times 10^{11}$	$\leq 1 \times 10^{11}$	$\leq 1 \times 10^{11}$
Oxygen (tolerance ± 1.5 ppma) (ASTM '79) (F)	20–31	19–31	18–31	18–31	18–31	18–31	18–31
Edge exclusion (mm)	3	2	2	2	1	1	1
Site flatness (SFQR) (nm) (G)	≤ 250	≤ 180	≤ 150	≤ 130	≤ 100	≤ 100	≤ 100
Site size (mm × mm) (H)	22 × 22	25 × 32	25 × 34	25 × 36	25 × 40	25 × 44	25 × 52
Localized Light Scatterers (LLS) (includes particles) (nm) (I)	125	90	75	65	50	35	25
Total LLS (cm^{-2}) (J)	≤ 0.60	≤ 0.29	≤ 0.26	≤ 0.14	≤ 0.06	≤ 0.03	≤ 0.015
Total LLS (#/wf)	≤ 172	≤ 192	≤ 178	≤ 96	≤ 42	≤ 48	≤ 24
Particles ($\#/cm^2$) (C,K)	≤ 0.14	≤ 0.088	≤ 0.068	≤ 0.055	≤ 0.038	≤ 0.023	≤ 0.014
Particles (#/wf) (C)	≤ 41	≤ 60	≤ 47	≤ 38	≤ 27	≤ 36	≤ 22
D_0, DRAM (cm^{-2}) (L)	≤ 0.06	≤ 0.029	≤ 0.026	≤ 0.014	≤ 0.006	≤ 0.003	≤ 0.001
D_0, MPU (cm^{-2}) (L)	≤ 0.15	≤ 0.15	≤ 0.11	≤ 0.08	≤ 0.05	≤ 0.04	≤ 0.03
*Polished Wafer * *							
Total bulk Fe (at/cm^3) (M)	3×10^{10}	1×10^{10}	1×10^{10}	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$
Oxidation stacking faults (OSF) (cm^{-2}) (N)	≤ 7	≤ 4	≤ 3.5	≤ 3	≤ 2	≤ 1	≤ 1
Recombination lifetime (µs) (O) (P)	≥ 300	≥ 325	≥ 325	≥ 325	≥ 325	≥ 450	≥ 450
*Epitaxial Wafer * *							
Layer thickness (µm) (± % tolerance) (Q)	2–5 (± 5%)	2–4 (± 4%)	2–4 (± 4%)	2–4 (± 4%)	1–3 (± 3%)	1–3 (± 3%)	1–3 (± 3%)
Layer structural defects (cm^{-2}) (R)	≤ 0.0033	≤ 0.0029	≤ 0.0026	≤ 0.0023	≤ 0.0019	≤ 0.0016	≤ 0.0013
Layer structural defects (#/wf) (R)	≤ 1	≤ 2	≤ 1.8	≤ 1.6	≤ 1.3	≤ 2.5	≤ 2
*Silicon-On-Insulator Wafer**							
Silicon layer thickness (tolerance ± 5%) (nm) (S)	50–200	50–200	50–200	50–200	50–100	30–100	20–100
Buried oxide thickness (± 5%) (nm) (T)	≤ 400	≤ 200	≤ 200	≤ 200	≤ 100	≤ 70	≤ 50
$D_{BOX, MPU}$ (box defects) (cm^{-2}) (U)	≤ 0.12	≤ 0.12	≤ 0.09	≤ 0.06	≤ 0.04	≤ 0.03	≤ 0.02
$D_{INC, MPU}$ (inclusions) (cm^{-2}) (V)	≤ 0.15	≤ 0.15	≤ 0.11	≤ 0.08	≤ 0.05	≤ 0.04	≤ 0.03
$D_{TD, MPU}$ (threading dislocations) (cm^{-2}) (W)	$\leq 7.2 \times 10^{4}$	$\leq 7.4 \times 10^{4}$	$\leq 5.6 \times 10^{4}$	$\leq 3.9 \times 10^{4}$	$\leq 2.6 \times 10^{4}$	$\leq 2.0 \times 10^{4}$	$\leq 1.4 \times 10^{4}$
Effective recombination lifetime (µs) (X)	0.3	0.4	0.5	0.6	1	1	1

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Table 20 Starting Materials Technology Requirements (continued)

* *Parameters define upper limit values; independent predictors of yield, mathematically or empirically modeled at 99%. Upper limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one upper limit value "at a time;" other parameter values most likely near median value, thereby ensuring total yield for all parameters is at least 99%. It is essential that GOI yield of 99% be achieved (L) and other IC parametrics (leakage current, etc.) be minimized.*

A. *Organics/polymers modeled approximately 0.1 of a monolayer, $\leq 1 \times 10^{14}$ C at/cm^2.*

B. *Front-surface microroughness ≤ 0.10 nm for all CD generations except ≤ 0.15 nm @ 250 nm; instrumentation choice, target values, and spatial frequency range (scan size) selected based on application. Power spectral density analysis recommended to utilize full currently accessible range of 0.01-50 μm^{-1} (tapping mode atomic force microscopy (AFM))*

C. *Values more tolerant than pregate surface preparation levels*

D. *Metals empirically modeled for 99% yield by $Y = \exp[-D_M R_M T \beta(CD)^2 \delta]$, R_M kill ratio =1, T=# transistors or bits/chip per CD generation, β = width/length CD ratio = 1 for DRAM, δ = 1 CD for gate active area.* [6] *$D_M = K_1 (M)^3 \exp[-T_o/7]$, $K_1 = 1.854 \times 10^{-29}$ cm^{+4}, T_o = equivalent oxide thickness per CD generation. (The experimental data resulting in this model is based on and extends the precursor publication. W.B. Henley, L. Jastrzebski and N.F. Haddad, The Effects of Iron Contamination on Thin Oxide Breakdown—Experimental and Modeling, MRS 262, 993 (1992).) Metals (Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni) increased by factor 2 for CoO and assumes gettering. If no gettering decrease metals by factor 2. If IC manufacturer has initial cleaning process, group K and Na with other surface metals*

E. *Metals are Al, Ti, V, Zn. Assumes wafer gettering. Al is maximum surface concentration to prevent modification of silicon's oxidation rate; Al also forms charged defects in oxide*

F. *Range of center point value to provide IG (no IG) based on IC requirements. ± tolerance is min-max range about center point value; tolerance of ± 2 ppma appropriate @ 250 nm CD. Bulk Micro Defects (BMD) in IG (no IG) polished wafer > 1×10^8/cm^3 (< 1×10^7/cm^3) after IC processing. IOC '88 value obtained by multiplying ASTM value by 0.65*

G. *SFQR = CD for dense lines (DRAM half pitch). Partial sites included. Scanning stepper to be utilized ≤ 180 nm and new site flatness metric required. Non-optical lithography may be required for CD < 130 nm and site flatness may be decoupled from CD. Warp < 50 μm for all CD generations*

H. *Site size assumes scanning stepper with fixed height of scan field and essentially two MPU chips per field (post 250 nm CD)*

I. *Total front surface Localized Light Scatterers size (includes particles and COPs) = K_2 (CD); K_2 = 0.5. Less than 50 "visual" back-surface particles recommended*

J. *99% yield as in (D), R_{LLS} = 0.1, β =1, δ =1; includes particles and crystal defects such as COPs; instrumentation available to separate particles from other scatterers such as COPs. Control of growth of COPs during IC processing is required*

K. *Particle density empirically modeled by $K_3 (CD)^{1.42}$; CD in nm and $K_3 = 5.50 \times 10^{-5}$* [7]

L. *Gate oxide defects total electrical yield = 99% as in (D); β =1 (DRAM) and 10 (MPU), R_o = 1 and δ = 1CD unit. Test @ 10 MV/cm for 100 seconds under accumulation conditions*

M. *Fe consistent with τ_r (O); other bulk metals also important. Bulk Fe concentration (at/cm^3) cannot be converted to surface concentration (at/cm^2) via wafer thickness*

N. *OSF density empirically modeled by $K_4 (CD)^{1.42}$; CD in nm; $K_4 = 2.75 \times 10^{-3}$* [7]*; test at 1100°C, 1 hour steam, strip oxide/etch; n-type material more difficult to control OSF*

O. *$\tau_r \geq 2$ (wf thickness)$^2/D_n$, D_n = minority carrier diffusion coefficient at 27°C;* [8] *safety factor of 2 used. Appropriate technique(s) to control, passivate, or control surface effects required*

P. *$\tau_g = (qWn_i)(I_{limit}/(A_{CRI})^2)^{-1} \geq 50$ μs* [8, 9, 10] *ensures DRAM junction leakage current $I_{limit} \leq 10^{-16}$ A/bit @ 27°C (≤ 10^{-13} A/bit @ 100°C) for $A_{CRI} = 2.5$ μm^2* [11] *and W = 0.5 μm; I_{limit} scales with CD generation. Assumes subthreshold device leakage, gate oxide leakage, and diffusion current less than junction leakage current at 100°C*

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Table 20 Starting Materials Technology Requirements (continued)

Q. *Range of center point value with tolerance min-max % range about center point value. Flat zone modeled as 0.8 Epi thickness p/p^- with H_2 or argon substrate anneal useful*

R. *Epitaxial growth induced defects such as mounds and stacking faults where $Y = \exp[-D_{EPI}\ R_{EPI}\ A_{MPU}]$ for Y = 99%, $R_{EPI} = 1$ and A_{MPU} function of CD generation*

S. *Range of center point value with min-max tolerance of ± 5% about center point value*

T. *Center point value with min-max tolerance of ± 5% about center point value. Fully depleted silicon layer anticipated for CD < 100 nm, reflected in BOX thickness and dependent on IC application. Interface charge < $10^{11}/cm^2$*

U. *99% yield as in (D); $Y = \exp[-D_{BOX}\ R_{BOX}\ T\ \beta\ (CD)^2\ \delta]$, D_{BOX} = BOX defect density, R_{BOX} = BOX kill ratio = 0.2, $\beta = 10$, δ = 6 CDs (gate, source, and drain [includes LDD extension])*

V. *Similar to (U), D_{INC} = inclusion defect density, R_{INC} = inclusion kill ratio = 1, $\beta = 10$, and δ = 1 CD for inclusion defects (gate)*

W. *Similar to (U), D_{TD} = threading dislocations defect density, R_{TD} = TD kill ratio = 1×10^{-6}, $\beta = 10$ and δ = 2 CDs for TD (gate and LDD extensions [in source and drain])*

X. *$(\tau_r)^{-1} = (\text{SOI layer thickness}/2s)^{-1} + (\tau_{bulk})^{-1}$ where s = surface recombination velocity* [8]

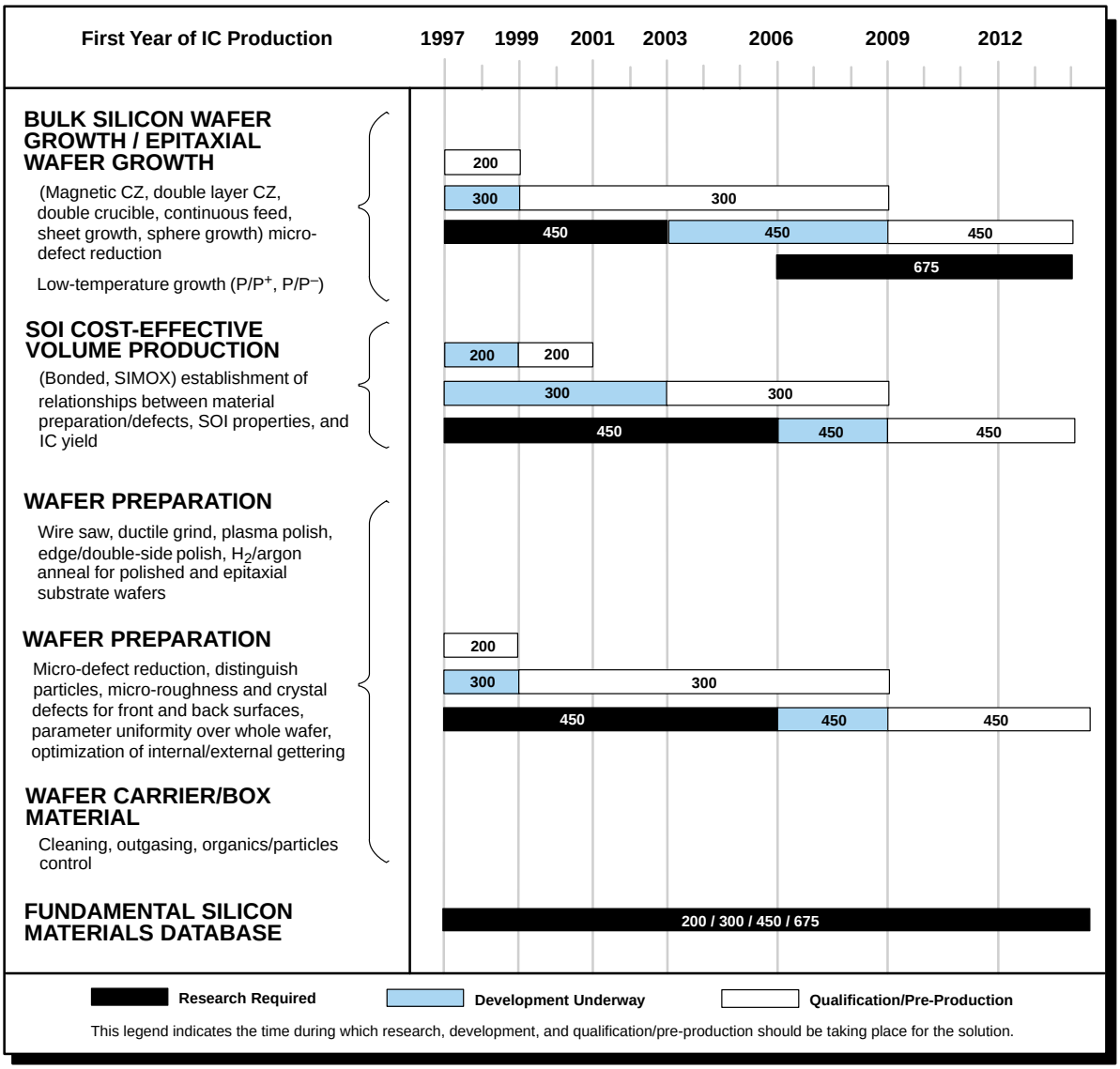


Figure 14 Starting Materials Potential Solutions

SURFACE PREPARATION

Surface preparation technology requires an increased understanding of fundamentals of surface and interface sciences including surface microstructure. Surface preparation techniques differ significantly between the FEOL and the BEOL because of materials and topography. With the shrinking device geometries and scaling of gate dielectrics, new materials will be required for gate dielectric (high κ) and gate electrodes (metal). Because of these changes in gate dielectric and gate electrode materials, new surface preparation tools/processes may be needed. Thus, the need for improvement in the area of surface preparation is immediate and continuous.

The FEOL process requirements are driven by gate oxide dielectric performance. The pre-gate surface preparation process is the most critical. Minimizing particles and metal contamination will dictate changing from the traditional clean to alternative chemistries. Research is required to understand the impact of surface termination, anions, organics, surface roughness, surface uniformity, and gate oxide thickness variations on device performance.

The BEOL surface preparation technologies are driven primarily by metal deposition, etch, contact formation, and planarization process requirements. Alternatives to solvent-based cleans need to be developed to minimize particles, corrosion, and contact resistance. Extensive fundamental and applied research is required. Table 21 summarizes the technology requirements for wafer surface preparation.

Surface preparation potential solutions are shown in Figure 15. Wet chemical cleaning technologies are favored because of the many inherent properties of aqueous solutions, such as the high solubility of metals, zeta-potential control, and efficient sonic energy transfer for megasonic particle removal. Hence, wet chemical surface preparation methods are likely to continue to find wide application in the foreseeable future. Gas phase cleaning technologies will find acceptance if device and cost benefits are demonstrated. This may be particularly critical for later 300 mm generation and first 450 mm generation where cleans and strips integrated with the processes will likely be required to meet productivity goals.

Surface preparation technology overlaps many technology thrusts. Reduced chemical use, chemical and water recycling, and alternative process technologies offer ESH and CoO benefits. Additional CoO benefits can be realized by footprint reduction, fluid flow optimization through modeling, and *in situ* sensor-based process control.

Table 21 Surface Preparation Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Front End of Line (A)							
DRAM critical area (cm^2) (B)	0.16	0.32	0.50	0.68	1.60	3.14	6.40
Logic critical area (cm^2) (C)	0.06	0.10	0.15	0.13	0.19	0.24	0.43
DRAM GOI D_0 (cm^{-2}) (D)	0.06	0.03	0.026	0.014	0.006	0.003	0.001
Logic GOI D_0 (cm^{-2}) (D)	0.15	0.15	0.11	0.08	0.05	0.04	0.03
Light scatters (E)							
DRAM	0.3	0.15	0.1	0.075	0.03	0.015	0.01
Logic	0.75	0.5	0.45	0.4	0.25	0.2	0.15
Particle size (nm)	125	90	75	65	50	35	25
Critical metals (atoms/cm^2) (F)	5×10^9	4×10^9	3×10^9	2×10^9	1×10^9	$< 10^9$	$< 10^9$
Other metals (atoms/cm^2) (G)	5×10^{10}	2.5×10^{10}	2×10^{10}	1.5×10^{10}	1×10^{10}	5×10^9	$< 5 \times 10^9$
Organics/polymers (C atoms/cm^2) (H)	1×10^{14}	7×10^{13}	6×10^{13}	5×10^{13}	3.5×10^{13}	2.5×10^{13}	1.8×10^{13}
Oxide residue (O atoms/cm^2) (J)	1×10^{14}	7×10^{13}	6×10^{13}	5×10^{13}	3.5×10^{13}	2.5×10^{13}	1.8×10^{13}
Back End of Line (K)							
Particles (cm^{-2})	0.3	0.15	0.13	0.1	0.06	0.045	0.03
Particle size (nm)	125	90	75	65	50	35	25
Metals (atoms/cm^2) (L)	1×10^{11}	5×10^{11}	4×10^{11}	2×10^{11}	1×10^{11}	$< 10^9$	$< 10^9$
Anions (atoms/cm^2) (M)	1×10^{11}	1×10^{11}	1×10^{11}	1×10^{11}	1×10^{11}	1×10^{11}	1×10^{11}
Organics/polymers (C atoms/cm^2) (N)	1×10^{14}	7×10^{13}	6×10^{13}	5×10^{13}	3.5×10^{13}	2.5×10^{13}	1.8×10^{13}
Oxide residue (O atoms/cm^2) (N)	1×10^{14}	7×10^{13}	6×10^{13}	5×10^{13}	3.5×10^{13}	2.5×10^{13}	1.8×10^{13}

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Table 21 Surface Preparation Technology Requirements (continued)

A. Starting wafer up to deposition of the pre-metal dielectric

B. Bits/chip multiplied by the critical dimension squared

C. Transistors/chip multiplied by 10 times the critical dimension squared

D. Based on the critical area at a 99% yield per critical step (with 10 critical steps, the total GOI defect level would be approximately 10 times this number); suggested short loop GOI test (includes some reliability failures): 10 MVolt/cm for 100 sec. (corresponds to 1 coulomb/cm^2 for thicker oxides)

E. Acceptable GOI defect densities and a kill ratio of 20% measured post-critical clean; tighter levels may be required if critical, non-gate area is considered.

F. DRAM requirement for Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni, W measured post critical clean for a gettered wafer

G. DRAM requirement for Al, Ti, V, Zn (Ba, Sr, and Ta if present in the factory measured post critical clean for a gettered wafer)

H. Measured post critical clean including pre-gate, pre-poly, pre-metal, pre-silicide, pre-contact,and pre-trench fill

I. RMS roughness with 1×1 μm AFM scan measured pre-gate requirement for wavelengths < 50 nm also needs to be specified

J. Measured pre-metal, pre-silicide, and pre-contact

K. Poly-silicide metal dielectric deposition through passivation

L. K, Li, Na, measured post critical clean

M. Cl, N, P, S, F measured post critical clean. Assumes no fluorinated oxide.

N. Measured post critical clean of a metallic surface region

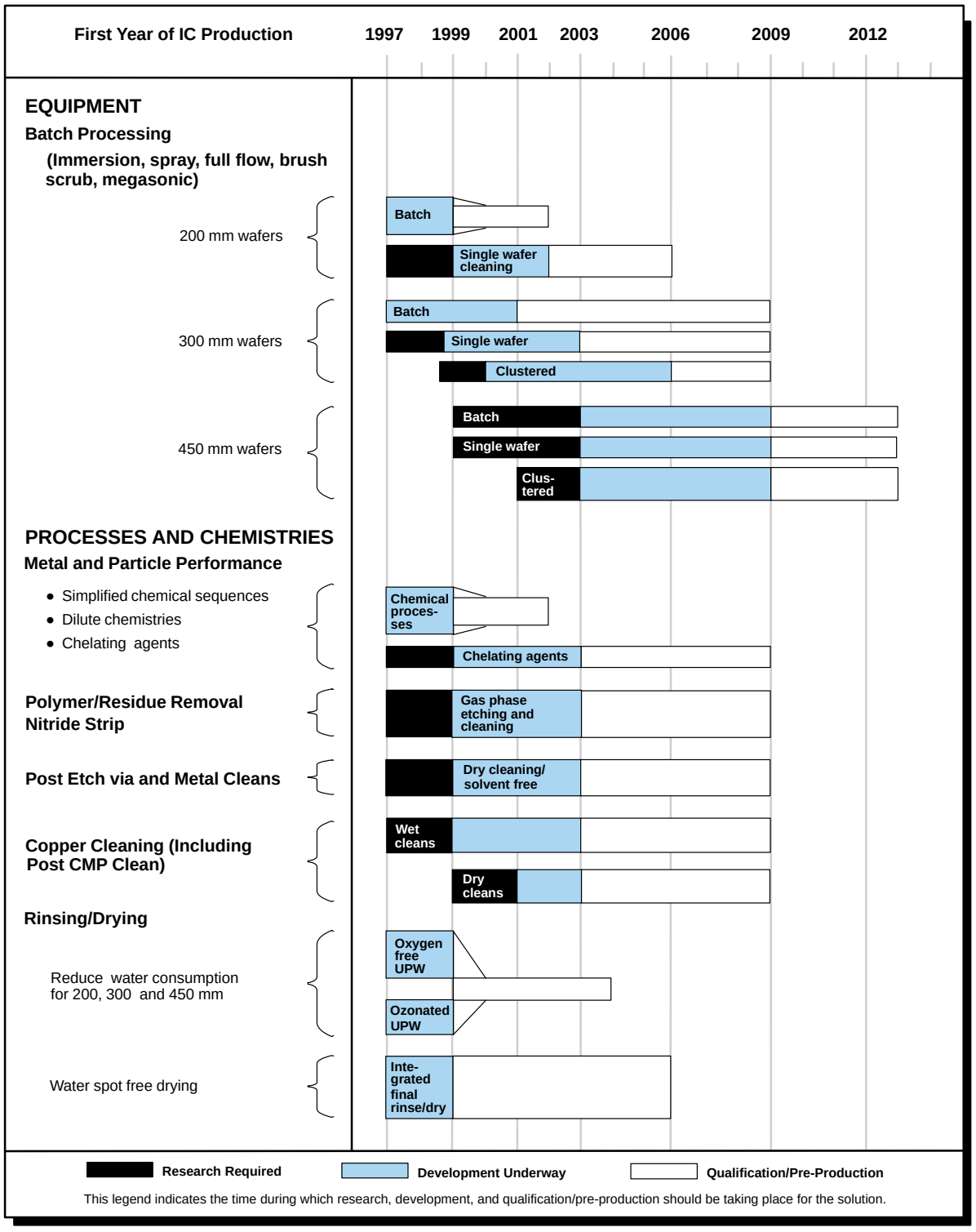


Figure 15 Surface Preparation Potential Solutions

THERMAL/THIN FILMS AND DOPING

Front end processing requires the growth and deposition of high quality, uniform, defect-free insulating films, silicon, and conductors and the precision doping of the underlying substrate and deposited layers. In addition to reduced thermal budgets required by device scaling, several other difficult

challenges have been identified for this area including the growth of reliable very thin gate dielectric layers; the identification and development of alternate high dielectric constant layers for both gate and DRAM capacitor applications; the formation of and making contact to ultra-shallow device junctions; and the development of alternate, depletion-free, low-resistivity gate materials. Other important challenges include the achievement of abrupt channel doping profiles, defect management for minimum post implant leakage in small thermal budget environments, sidewall spacer formation, and drive current limits by high channel doping levels that ultimately will require the development of new device structures. CMOS-compatible innovative solutions are needed in all of these areas. Underlying all these concerns is the inevitable rise of leakage currents associated with threshold scaling, gate dielectric tunneling, and junction tunneling.

THERMAL/THIN-FILMS

The gate dielectric has emerged as one of the most difficult challenges for future device scaling. Requirements summarized in Table 22 indicate an oxide equivalent thickness of less than 1 nm. Tunneling currents preclude the use of SiO_2 dielectric layers below about 1.5–2 nm thickness where tunneling currents larger than 1 A/cm^2 are predicted. Since tunneling currents will scale exponentially with further thickness reductions, phase-out of this dielectric material is likely beyond the 100 nm node. No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material. Similar problems are anticipated with the DRAM storage capacitor dielectric at an earlier technology node. The near-term gate dielectric solution requires the fabrication and use of ultra-thin silicon oxide, oxynitride films, or silicon nitride films. The latter film shows attractive boron diffusion penetration resistance and a moderately higher dielectric constant value of 7. Near term solutions will impose severe restraints on surface preparation, pre-and post-process ambient control, silicon compatible materials development (gate electrodes and contacts for example), and post processing thermal budgets. Improved thickness control and uniformity will be essential to achieve V_t control on 450 mm wafers. Sensitivity to post-gate process induced damage associated with ion implant and plasma etching is expected to increase especially as it relates to leakage associated with gate perimeter. Long-term solutions require the identification of materials with a higher dielectric constant (>20 suggested) with other electrical characteristics (e.g., stability and interface state densities) and reliability approaching that of high quality gate SiO_2. A major problem with a material other than SiO_2 is the probability that a very thin SiO_2 layer will still be required at the channel and/or gate electrode interface to preserve interface state characteristics. This would severely degrade any benefits that accrue from the use of the high κ dielectric. Another challenge is the achievement of acceptably low electrical leakage. To fill these needs, the high κ dielectric must have a band gap of 4–5 eV with a barrier height of >1 eV to limit thermionic emission and Fowler-Nordheim tunneling. In addition, the candidate dielectric material must have negligible trap densities to inhibit Frenkle-Poole tunneling. Finally, the material must have excellent diffusion barrier properties to prevent gate material (or gate dopant) contamination of the transistor channel.

The gate electrode also represents a major challenge for future scaling. Channel autodoping associated with boron out-diffusion from the p^+ polysilicon gate and depletion associated loss of channel charge control will eventually require the phase-out beyond the 100 nm technology node of the currently used dual-doped polysilicon gate material. A long term solution such as a low resistivity CMOS-compatible alternative gate material is not presently comprehended and years of research will be required to identify and qualify an alternative. Work function, resistivity, and compatibility with CMOS technology are key parameters for the new candidate material. The latter may require that different gate materials be used for the PMOS and NMOS transistor gate electrodes to achieve acceptable threshold voltages; the former having a Fermi level near the silicon valence band, and the latter having a Fermi level near the conduction band. Alternatives are the use of SOI or dual-junction isolated transistors where a mid band-gap Fermi level may be used in conjunction with substrate or well biasing. Near term potential solutions to the gate electrode problem include improvements in the doped polycide gate

stack. The boron penetration resistance of the gate dielectric is of great importance (e.g., silicon nitride) as is the development of enhanced means of activating the doped polysilicon for achieving tighter control of the work function.

Sidewall spacers are currently used to achieve isolation between the gate and source/drain regions, as well as to serve as an element for the achievement of self-aligned, CMOS-compatible drain-engineered dopant structures. The robustness of the sidewall spacer limits the gate and source/drain contacting structure and processes that can be used. The lack of a potential spacer solution beyond the 100 nm technology node will become acute when elevated source/drain structures are likely to be required. Single drain elevated structures will require sidewall thicknesses in the range of 5–10 nm and gate dielectric-like reliability and stability to manage parasitic series resistance. In addition, the spacer will be subjected to processes such as selective epitaxial silicon, or selective titanium silicide deposition that are known to degrade thin dielectric layers. Sidewall spacers have traditionally been formed from deposited oxides, thermal oxidation of polysilicon, deposited nitrides, and combinations of these. These technologies will continue to be used at least until the time when elevated or raised source/drain structures are required. Research has shown that below about 20 nm even the best thermal oxides are susceptible to defect formation when subjected to selective Epi processes. Nitrides or oxynitrides may offer a better alternative than oxide; however, additional research is needed to find and qualify an acceptable sidewall spacer. Key issues are the integration of the sidewall process into the gate stack process, cumulative thermal budget issues, and the dependencies between process variables and L_{eff} tolerances. Reasonable process times will limit the maximum temperature severely with each generation in order to maintain shallow junction profiles. By the 100 nm technology generation timeframe the maximum temperature will be approximately 900°C, and at 50 nm the maximum temperature is likely to be 800°C. A potential solutions roadmap for FEOL Thermal/Thin Films is given in Figure 16.

DOPING TECHNOLOGY

Scaling laws will challenge conventional methods used to dope deep submicron silicon devices. A difficult challenge is the doping and contacting of ultra-shallow CMOS source and drain regions. The conflicting demands of producing highly doped, more shallow source/drain and drain extension junctions and contacting these with low sheet resistance contact material, will initially challenge the conventional titanium salicide process. These issues require development of innovative new device structures in which the source and drain contact regions are elevated with respect to the channel. In addition, scaling of the contact area will result in unacceptable parasitic resistance if the specific contact resistivity of the silicon/silicide interface cannot be correspondingly reduced. An acceptable contact resistivity will require that the maximum concentration of activated dopant be achieved in the silicon at the silicide interface, and may also require that the metal/semiconductor barrier height be reduced. Before these limits are reached, the interim extension of conventional salicided source/drain structures will challenge process capability and manufacturability of incumbent methods for producing doped contact regions. Concurrently, the conventional means of shunting the contact regions with a self-aligned silicide will be challenged by the need to achieve low sheet resistivity while at the same time continuously minimizing silicon consumption.

Potential doping solutions for these problems include ultra low energy ion implantation, plasma immersion ion implantation (PIII), projection gas immersion laser doping (PGILD), as well as rapid thermal gas immersion doping. Contact shunting potential solutions include progressively scaling of the incumbent salicide process; selectively depositing titanium silicide; the siliciding of deposited sacrificial silicon; and the selective depositing of an alternate low resistivity contact metal. The doping and contact shunting processes are highly interactive and result in a complex materials science problem for which innovative integrated CMOS-compatible solutions are required. Similarly, current methods under investigation for producing elevated contact structures needed for the 100 nm node are still in the research stage and are not yet production qualified.

Scaling is also expected to have a significant impact on processes used for doping drain extensions, channels, and channel edges. Drain extension doping levels are expected to increase, driven by the need to reduce both parasitic resistance and junction depth. Similarly, drain extension doping profiles, which with earlier technology nodes required lateral grading for minimum hot carrier damage, will in the future need to become laterally abrupt to support low voltage operation. Ultimately, single drain devices may provide the best solution for optimum device on-current. Channel doping levels are expected to increase for suppression of short channel behavior. For the same reasons, higher doping concentrations will also be required for drain engineering implants such as Halo or large angle tilt implant (LATID). As a result, it will be difficult to scale threshold voltages and transconductance will decrease significantly. The use of abrupt, vertically steep, transverse retrograde channel dopant profiles will help control threshold voltage increases and maximize device on-current. The conflicting requirements for increased doping, more abrupt dopant profiles, and reduced thermal budget, will require a greater level of fundamental knowledge about point defect interaction, migration, and clustering to minimize transient enhanced diffusion (TED) and to minimize defect induced junction leakage which would ordinarily ensue with small thermal budget activation methods.

One near-term channel doping solution is the achievement of abrupt profiles through implantation of large atomic number species such as indium and antimony. Ultimately, the need for very abrupt damage free junctions may require the use of epitaxially deposited hyper-abrupt channel structures. In the very long term, it is expected that increasing channel dopant concentrations will result in threshold voltages that will increase, despite very aggressive scaling of the gate dielectric and the use of abrupt channel doping protocols. This will impose a fundamental limit on the historically achieved increase in device transconductance with each technology node. This fundamental limit expected at the 50–70 nm nodes will require the use of innovative new device structures, or fully depleted devices made on SOI substrates. Manufacturable CMOS-compatible solutions are much needed in this very important area.

Increased transistor densities will cause significantly reduced n^+/p^+ spacing resulting in the need for improved inter-well isolation and the abandonment of local oxidation of silicon (LOCOS) in favor of shallow trench isolation methods. Increased use of triple well structures is anticipated. This is driven by the need to achieve dynamic control of channel potential for both p- and n-channel devices. High energy ion implantation techniques, aided by improved understanding of point defect kinetics and better TCAD modeling, offer potential solutions to these isolation doping needs. In addition, epitaxial silicon and SOI substrates offer potential solutions. In the isolation area, solutions that accrue from enhanced doping processes are expected to occur as a result of innovation and improvements that result from normal day-to-day interactions between equipment suppliers and users. However, TCAD and defect kinetics research are needed in support of these interactions. The potential solutions roadmap is shown in Figure 17.

Table 22 Thermal/Thin Films Gate Etch and Doping Technology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Equivalent oxide thickness T_{ox}(nm)	4–5	3–4	2–3	2–3	1.5–2	< 1.5	< 1.0
Thickness control (% 3σ)	± 4	± 4	± 4	± 4–6	± 4–8	± 4–8	± 4–8
Sidewall spacer thickness (nm)	100–200	72–144	60–120	52–104	20–40	7.5–15	5–10
Gate electrode sheet Rs (Ω/□)	4–6	4–6	4–6	4–6	4–6	4–6	4–6
Post etch CD (nm, 3σ)	20	14	12	10	7	5	4
Maximum gate dielectric loss from etch (nm)	0.7	0.5	0.5	0.4	0.3	0.3	0.3
Drain structure	Drain Extension				+ Elev. S/D	Elev. Single Drain	
Contact Xj (nm)	100–200	70–140	60–120	50–100	40–80	15–30	10–20
Xj @ channel (nm)	50–100	36–72	30–60	26–52	20–40	15–30	10–20
Silicide thickness (nm)	70	55	45	40	45–70	New Structure	
Contact silicide sheet Rs (Ω/□)	2	2.7	3.3	3.8	2	2	2
Si/Silicide max resistivity (Ω–cm)	$< 1 \times 10^{-6}$	$< 6 \times 10^{-7}$	$< 4 \times 10^{-7}$	$< 3 \times 10^{-7}$	$< 2 \times 10^{-7}$	$< 8 \times 10^{-8}$	$< 3 \times 10^{-8}$
Drain extension conc. (cm^{-3})	1×10^{18}	1×10^{19}	1×10^{19}	1×10^{19}	1×10^{20}	1×10^{20}	1×10^{20}
Channel conc. for $W_{depletion} < 1/4L_{eff}$ (cm^{-3})	1×10^{18}	2×10^{18}	2.5×10^{18}	3×10^{18}	4×10^{18}	8×10^{18}	1.4×10^{19}
Unif. channel conc. (cm^{-3}), for V_t=0.4	$4–6 \times 10^{17}$	$6–10 \times 10^{17}$	$7–13 \times 10^{17}$	$1–2 \times 10^{18}$	$2–3 \times 10^{18}$	$> 3.5 \times 10^{18}$	$> 7 \times 10^{18}$
Retro channel peak depth (nm)	50–100	36–72	30–60	26–52	20–40	15–30	10–20
Retro channel peak conc. (cm^{-3})	$5–20 \times 10^{17}$	$2–6 \times 10^{18}$	$4–8 \times 10^{18}$	$6–10 \times 10^{18}$	$1–2 \times 10^{19}$	$1.5–4 \times 10^{19}$	$2–8 \times 10^{19}$

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Note: All junction depths measured from x=0 at gate dielectric/silicon interface

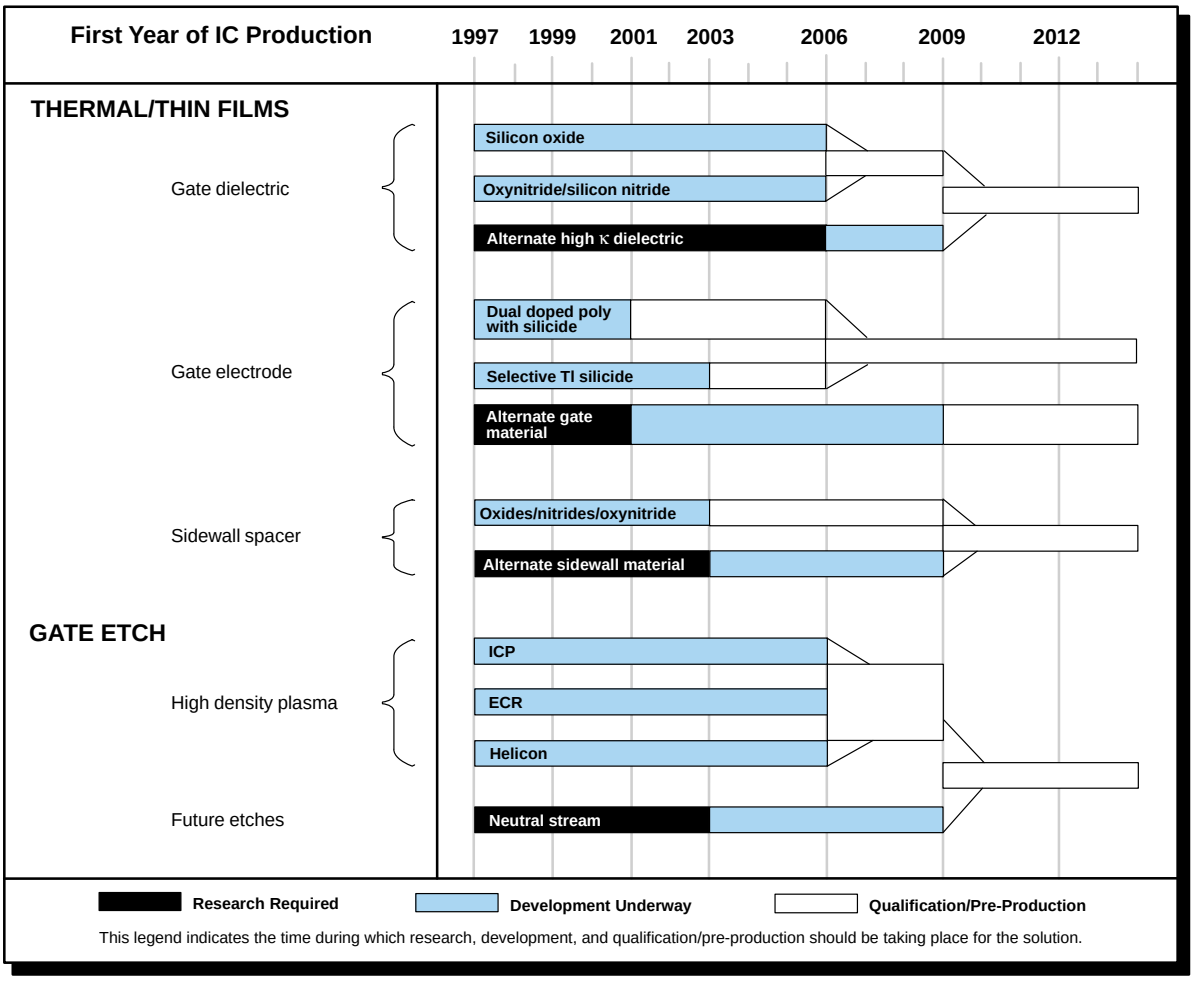


Figure 16 Thermal/Thin Films and Gate Etch Potential Solutions

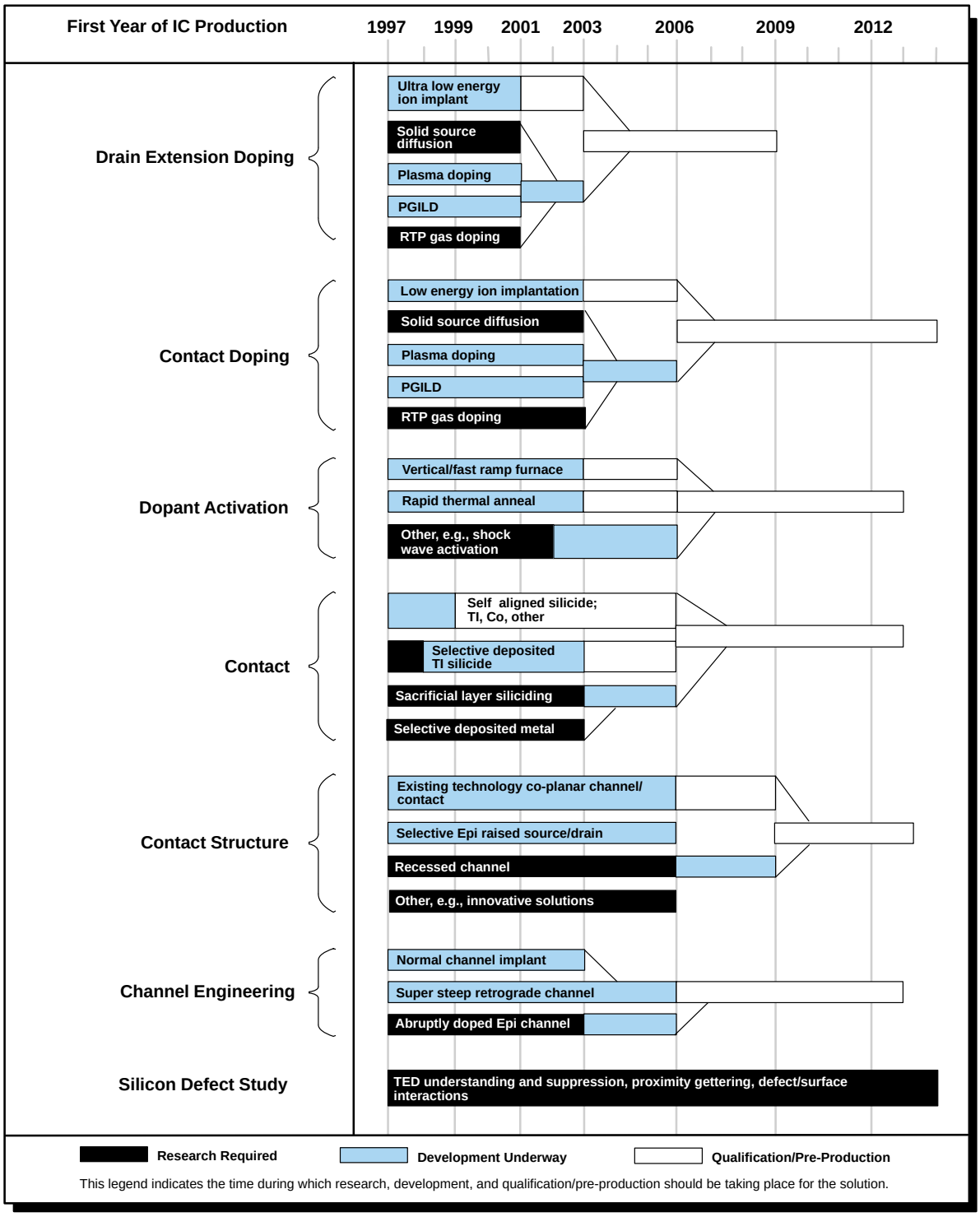


Figure 17 Doping Potential Solutions

FRONT END ETCH PROCESSING

Future challenges for front end etch processing are largely driven by decreasing critical dimensions (CDs) and new materials that will be used in front end wafer manufacturing. The most challenging front end etch technical requirements are maintaining low CD bias and high CD uniformity at continually larger wafer diameters and obtaining the required etch selectivity and etch profiles for the new front end materials. Post-etch gate CD requirements are given in Table 22.

To preserve the CD of the etch mask, high etch selectivity is required between the mask material and the one or more underlying materials to be etched. If sufficient selectivity cannot be obtained to an organic photoresist mask then it may be necessary to transfer CD to a hard mask (which could also serve as an anti-reflective coating) and then use the hard mask to transfer the CD to the underlying material. Successfully transferring the CD from the mask to the underlying material also requires the etch process to be extremely anisotropic to produce structures with near vertical sidewalls, especially for gate and sidewall etch. In addition, microloading must be minimized to match etch rate and profile for both isolated and high aspect ratio dense structures.

Decreasing CD also imposes strict front end etch requirements in the areas of defect density (etch block) and plasma damage. To meet future defect density requirements the plasma processes and etch tools must generate considerably fewer and smaller particles. Improvements will be required in the etch chemistries, the control of deposition in the etch chamber, and the cleaning procedures used for the etch chamber. Decreasing gate dielectric thickness makes the gate dielectric more susceptible to plasma charging damage. Plasma etch tool design and plasma processing conditions must be developed that do not cause charging damage.

New materials present a challenge since several front end etch processes require extremely high selectivity between subsequently etched layers. For example, polysilicon gate etching requires high selectivity between the polysilicon gate electrode and the silicon dioxide gate dielectric to allow an adequate over-etch of the polysilicon without etching into the silicon substrate. In the future, high etch selectivity will be required between new lower resistivity gate electrodes, such as metals, and higher dielectric constant gate dielectrics. New etch chemistries and process conditions may be needed to etch these new materials with the required etch selectivity and feature profile.

In the future, front end etch processing will move towards low pressure, high density plasma (HDP) etch tools that have separate radio frequency (RF) power sources for plasma generation and wafer biasing. Fewer collisions at low pressure allow for a more anisotropic etch with less microloading. The RF power to the plasma can be used to control the ion and reactive radical densities while the RF power to the wafer controls the ion energy. High etch rates and high selectivity can be obtained through this independent control of the chemical and ion driven components of the etch process. Another benefit of HDP etch tools is the high degree of plasma uniformity that can be obtained with a large variety of etch chemistries and etch processing conditions.

High density plasma etch tools and processes can be developed with considerably less plasma charging damage than their lower density reactive ion etcher counterparts. However, the process windows and hardware configurations for these low damage, high density etches have been difficult to tune and lock in. Plasma damage will continue to be a major issue as reactors are designed for higher density processing to meet gate dielectrics scaling, and larger diameter wafer processing requirements. Furthermore, it is unknown if plasma charging damage can be avoided through the 70 nm technology node since the gate dielectric for that node is not yet defined. If plasma charging damage cannot be avoided in plasma etch tools then chemical downstream etching or neutral stream etching must be pursued as an option. However, considerable research and development is required to build a large area chemical downstream etch tool that has sufficiently high directed neutral kinetic energy to satisfy the anistropic etch requirements of the future. Gate etch potential solutions are summarized in Figure 16.

CROSSCUT NEEDS

ENVIRONMENT, SAFETY, & HEALTH

The key ESH concerns for front end processes center on natural resources use (especially water), management of physical and chemical hazards to ensure worker protection, and optimization of processes to reduce chemical use and generation of wastes requiring abatement. New gate materials (and corresponding etch gases) for 100 nm technologies and beyond should undergo thorough ESH review.

Major ESH issues affect all areas of front end processes. The primary chemical management strategy should be to optimize processes to maximize chemical use efficiency, including consideration of chemical throughput, waste generation, and tool utilization factors. On-demand/*in situ* chemical generation can contribute to improved efficiency. Integrating POU abatement technologies with tools can provide desired control levels at a reduced energy cost. Energy needs (tool and facility systems) must be evaluated for new technologies. Worker protection measures should address potential physical (e.g., thermal, non-ionizing radiation, laser, and robotics hazards) as well as chemical hazards, especially during equipment maintenance. Factory planning should identify ergonomic design criteria for wafer handling (especially for 300/450/675 mm wafers), tools, and fab layout. ESH cost-of-ownership (CoO) and risk assessment tools should be utilized to evaluate process improvements and identify potential risks of new materials. In addition, key ESH issues apply to specific areas of front end processes:

Surface Preparation—ESH concerns for surface preparation focus on chemical use efficiency, water, and energy consumption. Chemical use optimization should be applied to conventional and alternate clean processes. Several alternate clean processes have potential for significant chemical use reduction (cryogenic, spray tool, dilute chemistries, sonic solvent cleans, simplified process flows, O_3 cleans, alternate BEOL cleans, cleans for new interconnect). Continued reductions in chemical bath temperature and other measures will extend bath life. The use of anhydrous gases (HF/HCl and alternatives) should be reviewed through process hazards analysis. Sustainable, optimized water-use strategies utilizing improved ultrapure water (UPW) production efficiency, reduced tool consumption, and cascade reuse can be developed. However, the energy-use impact of alternate clean methods (such as cryogenic wafer and parts cleaning and hot-UPW wafer cleaning) or UPW production methods (such as continuous electrolytic ion-exchange) needs to be considered. Development of reliable sensors to speciate low-level organics is needed to mitigate the process risk of UPW recycling. The larger volumes of water associated with CMP and post-CMP rinses warrant consideration of recycle systems. The optimization of test wafer usage can reduce chemical, water, and energy consumption. Wet-tool designs should continue to incorporate enclosed processes, ergonomic principles, and robotics safety.

Thermal/Thin Films and Doping—Chemical use efficiency can be optimized through improved delivery systems and tool designs (e.g. small batch furnaces, single-wafer tools). Energy use for diffusion and implant tools and associated facility systems (i.e., exhaust) should be evaluated and optimized. The potential physical and chemical hazards of alternate technologies (e.g., plasma doping, PGILD, rapid thermal gas doping) need to be evaluated and mitigated. Process hazards analysis tools will assist in managing hydrides (SiH_4, B_2H_6, PH_3, SbH_3, others), metal alkyls, and laser sources. The evaluation of alternative high-κ dielectrics (BST, Ta_2O_5, TiO_2, other materials) must include thorough assessment of potential process hazards associated with both materials and deposition processes. Alternate silicides (e.g., Co) present potential hazards requiring mitigation.

Front End Plasma Etch—Continued use of perfluorocompounds (PFCs) will necessitate near-term process optimization/increased gas utilization (i.e., conversion efficiency within the process). Over the longer term, alternative chemistries for PFCs that do not emit PFCs as by-products need to be developed. Changes in gate dielectric materials will drive corollary changes in etch chemistries, necessitating review of potential ESH impacts.

DEFECT REDUCTION

Front end processes and defect reduction have strong crosscut interdependencies. In high-volume manufacturing of multi-level metallization processes, BEOL defectivity is a dominating factor in overall yield. But because of the significant yield and device performance impact from trace contamination (e.g., metals, particles) and defect levels (e.g., silicon structural, COPs, stacking faults, etc.) front end processes will continue to drive defect reduction issues.

Impurity specifications for critical materials in front end processes need to be linked to known fault mechanisms to achieve economic viability of raw materials. Yield modeling based on atomistic level impacts of trace contaminants and ultra-small, widely distributed defects, and phenomenological data

need to be coordinated and linked to raw material specifications and defect density requirements. Fundamental research will be required to discontinue detection limit-based specifications of raw materials.

Detection of surface defects of ~0.5 per technology generation for both incoming materials and throughout the FEOL is economically achievable with some continuous improvement through the 130 nm technology generation. Research will be required to extend this detection sensitivity to the 50 nm technology generation. Complicating this requirement is the issue of kill ratio of these size defects. The previous Roadmap noted ~0.33 per technology generation as the critical particle size. Of course these size particles can also kill, but with a lower probability than 0.5 per size particles per technology generation. With kill ratios in the 20%–30% range, it may be possible to control front end processes while monitoring a slightly larger particle size. Research into particle size distributions below ~50 nm and into particle size yield impacts will aid in developing the appropriate line monitoring and engineering tools. It should also be stated that these assumptions do not account for the obvious near 100% kill ratio of gate thickness size particles in the transistor gate area, and yet have not been a driving factor for particle detection tool sensitivity.

Surface termination control will continue to drive requirements in isolation technology for FEOL processes. Outgassed organic and ionic species from cleanroom materials, cassettes, pods, or filters impact device performance and yield. At the same time inert ambient solutions for storage and process-to-process transport (e.g., gate oxide deposition to gate electrode deposition) have been demonstrated. Research and development (R&D) of these potential solutions in conjunction with process, yield, and performance requirements will be necessary to understand the appropriate technology generation insertion point as a necessity for cost-effective, high-volume manufacturing environments.

Clearly, the greatest challenge in front end defect inspection is the reliable, fast detection of partially etched contacts, missing/extra pattern local interconnects, and small residues in the bottom of contacts and isolation trenches. Current detection technology is limited to slow, capital intensive, SEM-based tools intended for engineering analysis, not as inline production monitoring tools. Research in short wavelength optical and novel detection schemes will be necessary to provide cost-effective production tools to support continued yield learning in front end processes.

METROLOGY

In this section the specific metrology needs for starting materials, surface preparation, thermal/thin films and doping, and front end plasma etch technologies are covered.

Starting Materials—Materials acceptance practices based on specifications for silicon wafers are rapidly approaching detection and resolution limits. This will require significant improvements in the sensitivity (detection limit) and resolution of the metrology for several key characteristics including oxygen content variation, site flatness, particle density, and surface metal concentration. Of particular importance are front and back-side particles. Over the last several years, the ability of particle detection technology to distinguish particles from haze has advanced, but meeting future needs will require continued effort. Improved methods for determining bulk micro-defects are required. Carrier lifetime measurements for very thin Epi needs improvement.

Surface Preparation—Particle detection is covered in the *Defect Reduction TWG* section. Particle/defect and metallic/organic contamination analyses are covered in the *Metrology* section.

Thermal/Thin Films—Tools for film thickness, electrical characteristics, and composition are sufficient to 2 nm; however, significant metrology challenges will arise for gate films below 2 nm oxide-equivalent thickness. As manufacturers move to single-wafer and cluster processing tools, improvements in offline, inline and *in situ* metrology will be required. The move toward gate dielectric stacks and new gate electrode materials/stacks including poly-on-poly layers requires development of optical models and proof of metrology manufacturability. Optical measurements of sub-2 nm SiO_2 will need to comprehend the atomic structure of oxide and interface layers. Measurement of interfacial

oxide layers in combination with high κ materials will be required. Reference materials, optical constants of one to two monolayers of gate dielectric materials, standard procedures including analysis area, and optical models for non-SiO_2 materials need to be developed. Electrical measurements such as C–V must be further developed for application to the sub-100 nm technology generation. Improved metrology is required for characterizing surface roughness. Ellipsometry will continue to be the leading method for film thickness and composition metrology. The development of innovative optical models that correlate with electrical measurements are especially needed as the film thicknesses shrink below 2 nm. The currently available offline tools will have to be significantly redesigned for inline/*in situ* use, increased spatial resolution, and improved long-term stability. X-ray photoelectron spectroscopy systems with whole wafer sample stages are being used for thin dielectric characterization during development.

Doping Technology—Improvement in inline process measurement to control active dopant implants is required beyond 180 nm. Presently, 4-point probe measurement is used for high dose implant and thermally modulated optical reflectance is used for low dose process control. Both methods need improvement, and a new method is needed that provides a more direct measurement of dose, dopant profile, and dose uniformity. *In situ* measurement should be targeted. Offline secondary ion mass spectrometry equipped with whole wafer stages has recently been introduced as an alternative method for doping process control. New measurement methods based on acoustic waves are expected to be capable of nondestructive, inline measurement of dose and junction depth. Two and preferably three dimensional profiling is essential for realizing future scaling technologies. Activated dopant concentrations and profiles, TCAD modeling, and defect profiles are key for development of new doping technology.

Front End Etch—Improved metrology methods are needed for etch stop, damage, and etch induced surface roughness.

MODELING AND SIMULATION

Modeling and Simulation has a critical role to play for front end processes to meet the needs outlined in this Roadmap. The timely and cost-effective development of processes that most effectively use available technology will require the use of process and device simulation for both accurate prediction and analysis of device performance. In addition, reduced tolerances point to an increased need for simulations as tools in the development of processes that minimize the effect of process variations.

One of the most immediate concerns is the ability to model vertical and lateral doping profiles. This ability requires a fundamental understanding of dopant/defect diffusion processes, including interactions with extended defects and interfaces. Of particular importance is the evolution of dopant profiles and implant damage for very low source/drain and very high (well) implant energies. In the longer term, it will become necessary to develop accurate models for alternative doping technologies as they become integrated into process sequences. In addition, the need for higher doping levels to minimize parasitic resistance and poly depletion will make accurate modeling of nonequilibrium activation over multi-step anneals necessary.

As the technology pushes the limits of silicides for both source/drain and gate contacts, it will be necessary to develop physical models for silicide processing. This includes microstructural evolution of and interactions with both silicon diffusion profiles (e.g., dopant segregation) and the resulting device behavior (e.g., series resistance). As new technologies are developed (e.g., epitaxial silicides, selective Epi, metal gates) process models must keep pace. Modeling of the silicide is directly linked with modeling of the dopant profile and its activation in predicting capacitance and sheet resistance parasitics.

Accurate models will be required for the evolving gate dielectric materials, first for ultrathin oxides, oxynitrides, and nitrides, and later for higher κ dielectrics. Models are necessary not only for growth processes, but also for stress evolution, dopant penetration from the gate, and other interactions of the dielectric with dopant and defect populations in the substrate.

Modeling of front end deposition and etch processes becomes increasingly important as larger wafer diameters push the limits of uniformity across the wafer while finer gate stack and isolation structures require improved feature scale simulation. Modeling is also needed for the effects of damage, contamination, and stress from deposition and etching on subsequent processes.

Stringent defect density requirements point to a renewed importance of gettering processes and associated models. The use of lower oxygen levels and alternative substrates such as SOI or p/p^- Epi increases the need for predictive modeling of both intrinsic as well as proximity gettering.

SUMMARY

The semiconductor industry has been able to scale device dimensions far beyond expectations of just a few years ago. This reduction has been possible through innovation, persistence, and the properties of silicon, especially silicon dioxide, and a very limited number of other elements such as nitrogen, aluminum, and tantalum. The dimensions of devices are still based on bulk properties as interface properties have been kept to a minimum. In addition, a few new processes such as ion implantation have found their way into production. The advances have been successful through the development of analytical techniques to display the structure and to measure impurities along with processes for model development. The resulting knowledge base will permit continued scaling through several more technology generations with evolutionary changes. Several difficult challenges have been identified in the FEP Roadmap and include the gate dielectric, shallow junction formation, control of the channel doping profile, source/drain contacts, and larger diameter silicon wafers > 300 mm. Ambient and interface control will become more critical as will process integration and process modeling. For example, thermal budgets will be significantly reduced to temperatures below 800°C. Cost-of-ownership (CoO) will become more important and must be traded off against performance quality and yield.

Beyond the 100 nm technology generation, there are front end processes challenges as severe as the pattern definition challenges. Fundamental material limits at and beyond the 100 nm technology generation will significantly degrade the desired device performance if not solved and will prevent further scaling. Carrier confinement and control such as quantum considerations will require that new silicon compatible materials be used in the gate stack as well as new ways to form high concentration abrupt junctions. There is even a strong case for new materials that form the channel (e.g., Ge) region that simplify the implementation of high κ dielectric gate materials. Device operation will depend not only on bulk properties but interfacial layers a few atomic layers thick. To meet this challenge, significantly new resources must be directed toward new silicon compatible materials including high κ dielectrics and metals for gate electrodes with appropriate work functions and resistivities that are thermally stable. New device structures such as elevated source/drain and fully depleted structures will be required. The learning curve must be based on fundamental physics, chemistry, and materials science at the atomic scale. New metrology will be required along with model development to reduce development cycle time and to control processes. Phenomenon such as direct tunneling through the gate dielectric and the depletion region of p^+ and n^+ junctions must be limited to acceptable values. Reliability and “burn-in” must be re-evaluated as the result of different mechanisms that will accompany the scaled device. These challenges can be solved; however, they require immediate attention to ensure they are met in a timely manner.

LITHOGRAPHY

SCOPE

Lithography is the key technology driver for the semiconductor industry. The continued growth of the industry has been the direct result of improved lithographic resolution and overlay across increasingly larger chip areas. Lithography is also a significant economic factor, currently representing over thirty-five percent of the chip manufacturing cost. In addition, it is a technology with heavy global interdependence for equipment and materials. Significant investments from research and development to commercialization will be required to improve the infrastructure of this vital technology and to maintain industry growth.

The key elements of the lithography infrastructure include:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask equipment and materials
- Metrology equipment for critical dimension (CD) and overlay

This section covers the current status for each of these elements and provides a 15-year roadmap defining lithography difficult challenges, technology requirements, and potential solutions. Additionally, the section defines the Lithography Technology Working Group (TWG) interaction with and dependencies on other technologies. Potential paradigm shifts are also identified.

DIFFICULT CHALLENGES

The ten most difficult challenges to maintaining the industry productivity improvements are shown in Table 23. The five difficult challenges down to 100 nm include:

- Post-optical technology consensus
- Post-optical mask fabrication
- Optical mask fabrication with resolution enhancement techniques (RET) for <180 nm
- Gate CD control improvements
- Overlay improvements

Below 100 nm, the five difficult challenges are:

- Post-optical mask fabrication and process control
- Metrology
- Cost control
- Gate CD control improvements
- Overlay improvements

Table 23 Lithography Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Post-optical technology consensus	Narrowing of Roadmap options for 130–100 nm generations. Achieving global consensus among technology developers and chip manufacturers
Post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., membranes or multi-layer films)
Optical mask fabrication with resolution enhancement techniques for ≤ 180 nm	Development of equipment infrastructure (writers, inspection, repair) for relatively small market
Gate CD control improvements	Development of processes to control minimum feature size to less than 10 nm, 3 sigma
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Post-optical mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., membranes or multilayer films) Development of equipment infrastructure (writers, inspection, repair) for relatively small market Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm generations
Metrology	R&D for critical dimension and overlay metrology
Cost control	Development of innovative technologies, tools, and materials to maintain historic productivity improvements Achieving constant/improved throughput with larger wafers
Gate CD control improvements	Development of processes to control minimum feature size to less than 10 nm, 3 sigma, and reducing line edge roughness
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option

CURRENT TECHNOLOGY STATUS

Optical lithography continues to be the mainstream technology for the industry and is being used in production by leading-edge, high-volume factories at 250 nm design rules. Extensions of optical technology are being used to support 180 nm product and process development. Resolution enhancement techniques (RET) used for optical extensions include exposure tool advances such as wavelength reduction (248 nm→193 nm) and off-axis illumination, as well as phase shift mask (PSM) and optical proximity correction (OPC). While the industry momentum is behind optical extensions to 130 nm, the key challenge will be maintaining an adequate and affordable process latitude (depth of focus/exposure window) necessary for 10% post-etch CD control.

Advanced technologies, such as X-ray and electron beam direct-write (EBDW), have been used to fabricate functional semiconductor devices below 100 nm over small field sizes at low throughput. In addition, various technologies have been proposed and proof-of-concept studies are underway for resolution capability down to 50 nm.

Overlay and CD improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm. This will be inadequate for ground rules less than 100 nm. Overlay and CD control over large field sizes will continue to be a major concern for sub-130 nm lithography.

Mask-making capability exists for 250 nm generation chrome binary masks. Capability for complex PSM, OPC, and 180 nm binary masks are in development and pilot production. X-ray mask capability for 180 nm generation is in development. Mask processes for other advanced technologies are being researched.

Advanced I-line resists are in manufacturing with resolution capabilities down to 300 nm. Deep ultraviolet (DUV) resists at 248 nm are commercially available and being implemented in the manufacturing ramp for 64M DRAM and microprocessor (MPU) products. Resists are now being developed for specific levels to optimize their response and manufacturing robustness.

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Product Critical Level Lithography Requirements (Table 24)
- Product Critical Level Resist Requirements (Table 25)
- Critical Level Mask Requirements (Table 26)

Overlay, masks, resists, metrology, environment, safety, and health (ESH), and business issues are applicable to most technology approaches and will require increased emphasis.

Overlay requirements are among the most difficult technical challenges in lithography. Advances in stage technologies, environmental controls, interferometers, and alignment systems will be needed for sub-65 nm overlay.

Continuous improvements in mask making technology (mask writers, inspection, repair, and substrates) continue to be required to support the technical and manufacturing needs of optical lithography below 250 nm. Mask inspection requirements will become more aggressive as optical lithography pushes to lower resolution constant factors (k_1). Defect sizes for hard, soft, and transmission lost defects will potentially decrease faster than the Roadmap scaling. In addition, significant improvements will be necessary for all non-optical approaches, especially 1× proximity X-ray. Major process and materials development is required to achieve the tolerances and mechanical properties necessary in the unique substrates used in these advanced technologies. Key issues will be identification and repair of defects and the ability to keep the masks defect free in manufacturing. Also, solutions for rapidly growing data volumes need to be developed, especially for optical proximity correction.

The need for a proactive approach to ESH has been identified by the semiconductor industry. Using safer solvents, abating volatile organic compounds (VOCs) at point-of-use (POU), minimizing waste, dry processing, and eliminating heavy metals used in masks are possible ways to meet the roadmap ESH requirements.

Cost containment and reduction will require a total systems approach that includes exposure tool, mask, resist, and metrology. Cost projections and cost targets are diverging in the sub-250 nm resolution regime. For lithography solutions below 130 nm, significant R&D resources will be required.

Table 24 Product Critical Level Lithography Requirements

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*	*2006* / *100 nm*	*2009* / *70 nm*	*2012* / *50 nm*
Product Application							
DRAM (bits)	256M	1G	—	4G	16G	64G	256G
MPU (logic transistors/cm^2)	4M	6M	10M	18M	39M	84M	180M
ASIC (usable transistors/cm^2)*	8M	14M	16M	24M	40M	64M	100M
*Minimum Feature Size (nm)***							
Isolated lines (MPU Gates)	200	140	120	100	70	50	35
Dense lines (DRAM Half Pitch)	250	180	150	130	100	70	50
Contacts	280	200	170	140	110	80	60
Development capability (minimum feature size, nm)	140	120	100	70	50	35	25
Gate CD control (nm, 3 sigma at post-etch)**	20	14	12	10	7	5	4
Product overlay (nm, mean + 3 sigma)**	85	65	55	45	35	25	20
DRAM Chip Size (mm^2, 2:1 aspect ratio)							
Year 1	280	400	480	560	790	1120	1580
Year 2	220	320	390	450	630	900	1300
Year 3	170	240	290	340	480	670	950
MPU Chip Size (mm^2, 1:1 aspect ratio)							
Year 1	300	360	400	430	520	620	750
Year 2	240	290	320	340	420	500	600
Year 3	180	220	240	260	310	370	450
Field Size (mm × mm)	22 × 22	25 × 32	25 × 34	25 × 36	25 × 40	25 × 44	25 × 52
Field Area (mm^2)	484	800	850	900	1000	1100***	1300***
Depth of focus (µm, usable @ full field with ± 10% exposure)	0.8	0.7	0.6	0.6	0.5	0.5	0.5
Defect density, (defects per layer/m^2 @ nm defect size, lithography only)**	100 @ 80	80 @ 60	70 @ 50	60 @ 40	50 @ 30	40 @ 20	30 @ 15
Mask size (mm, square, quartz for optics)	152	152	230	230	230	230	230
Wafer size (mm, diameter)	200	300	300	300	300	450	450

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *ASIC will use maximum available field size*
** *Requirements scale with resolution for shrinks*
*** *Field size requirements are based on Year 2 chip sizes, the year demanding the full field size for high volume production*

Table 25 Product Critical Level Resist Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Resist thickness (µm, imaging layer)	0.6–1.0	0.5–0.7	0.45–0.65	0.4–0.6	0.3–0.5	0.25–0.35	0.2
Post-exposure bake sensitivity (nm/°C)	7	5	4	3	2	2	1
Contaminants (ionic/metal)	5 ppb						
Liquid defect particle size (nm, mean @ density of 25 particles/ml)	120	90	80	70	50	35	25
Airborne amine contamination (pptM)	1000	1000	1000	1000	1000	1000	1000
Backside particles (particles/m^2 @ critical size, nm)	3000 @ 200	3000 @ 200	3000 @ 200	2000 @ 100–200	2000 @ 100	2000 @ 100	2000 @ 100
Other requirements:	– Need for positive or negative resist will depend on the critical feature density – Slope should be 90 +0 –2 degrees – Thermal stability should be in the range of 130–150°C – Etch selectivity should be comparable to or exceed novolac – Strippability with no detectable residues						

Exposure Dependent Requirements

Exposure technology	248 nm DUV	193 nm DUV	X-Ray	Extreme ultra-violet	E-beam projec-tion	E-beam direct write	Ion pro-jection
Sensitivity (mJ/cm^2, range)	20-50	10-20	50	10	9		
Sensitivity ($\mu C/cm^2$, range)					5–10 @100KV*	1–5 @50KV*	0.2–5.8

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *Linked with resolution*

Table 26 Critical Level Mask Requirements

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*		*2006* / *100 nm*		*2009* / *70 nm*		*2012* / *50 nm*	
Wafer Minimum Feature Size (nm)	200	140	120	100		70		50		35	
Magnification	4	4	4	4	1	4	1	4	1	4	1
Mask Minimum Image Size (nm)	800	560	480	400	100	280	70	200	50	140	35
Mask OPC Feature Size (nm)	400	280	240	200	100	140	70	100	50	70	35
Image Placement (nm, multi-point)	52	36	32	28	14	20	10	16	8	12	6
CD Uniformity (nm)											
Isolated lines (MPU gates)	26	18	16	13	9	9	6	6	4	4	3
Dense lines (DRAM half pitch)	32	23	20	17	10	13	8	9	5	6	4
Contacts/vias	36	26	22	18	11	14	9	10	6	8	5
Linearity (nm)	40	28	24	20	9	14	6	10	5	7	3
CD Mean to Target (nm)	20	12	10	8	4	6	3	4	2	3	1
Defect Size (nm)	200	150	125	100	26	80	20	60	14	40	10
Data Volume (GB)	8	32	64	128	32	512	128	2048	512	8196	2048
Mask Design Grid (nm)	20	10	8	4	1	4	1	4	1	4	1
Mask Materials and Substrates (Exposure Tool Dependent)	**Optical**	**– Absorber on quartz, 152 mm and 230 mm square with pellicles** **– Primary PSM choices are embedded shifter and alternating aperture**									
	X-Ray	**– Refractory metal on Si Carbide Membrane (100 mm diameter)** **– "Pellicle" definition required**									
	E-Beam Projection	**– Refractory metal scatterer on strutted Si membrane (200 mm diameter)** **– "Pellicle" definition required**									
	EUV	**– Absorber on multilayer reflector substrate (300 mm diameter)** **– "Pellicle" definition required**									
	Ion Projection	**– Carbon coated silicon membrane stencil mask (200 mm diameter)** **– "Pellicle" definition required**									

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Note: The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.

POTENTIAL SOLUTIONS

The lithography strategy is presented in the following roadmaps:

- Critical Level Exposure Technology Potential Solutions (Figure 18)
- Critical Level Resist Technology Potential Solutions (Figure 19)
- Critical Level Mask Technology Potential Solutions (Figure 20)

Optical lithography is the desired mainstream approach to its cost-effective limits. Significant efforts are required to extend 248 nm DUV lithography beyond 250 nm production. Lens designs and optical enhancements must be developed to increase depth of focus. Improved DUV resists and anti-reflection materials and processes are also required.

Significant emphasis and resources have been applied to 193 nm DUV technology in the past three years. Current programs are targeted to bring the technology to the marketplace for the 180 nm generation. Affordable solutions to the depth of focus challenge must also be developed for this technology.

Alternative technology paths must be pursued to ensure the availability of production-worthy systems for the post-193 nm optics generations. Proximity X-ray lithography has had the most resources applied to its development both in the United States and Japan. Success will depend on the ability to manufacture 1× masks to specification, cost and cycle time, and on the ability to provide within-field magnification control.

In addition, E-beam projection, E-beam direct-write, extreme ultraviolet (EUV), and ion projection are being studied for sub-130 nm lithography. Particle beam column and system research is underway to understand particle interactions, error budgets, and manufacturing tolerances. This effort, along with new materials, sensors, resists, and mask substrates, has created critical checkpoints. If successful in the laboratory, these technologies would be candidates for manufacturing applications in the future.

Advanced resist systems will need to be developed for most advanced lithography approaches. Chemically amplified, multilayer, or thin layer imaging (TLI) resists may be needed to maintain the requirements of process latitude, etch resistance, implant blocking, and mechanical stability.

Evolutionary upgrades for existing mask equipment (e.g., mask writer, inspection, repair, and metrology) will be needed for each lithography generation. Mask inspection will require at-wavelength solutions for 193 nm technology and beyond. Significant process and materials development will be needed for all advanced lithography alternatives. Mask equipment for 1× proximity X-ray will drive some requirements for advanced n× technologies.

Although many technology approaches exist, the industry is limited in its ability to fund the development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions among government, industry, and universities are absolutely necessary to narrow the options for these future generations.

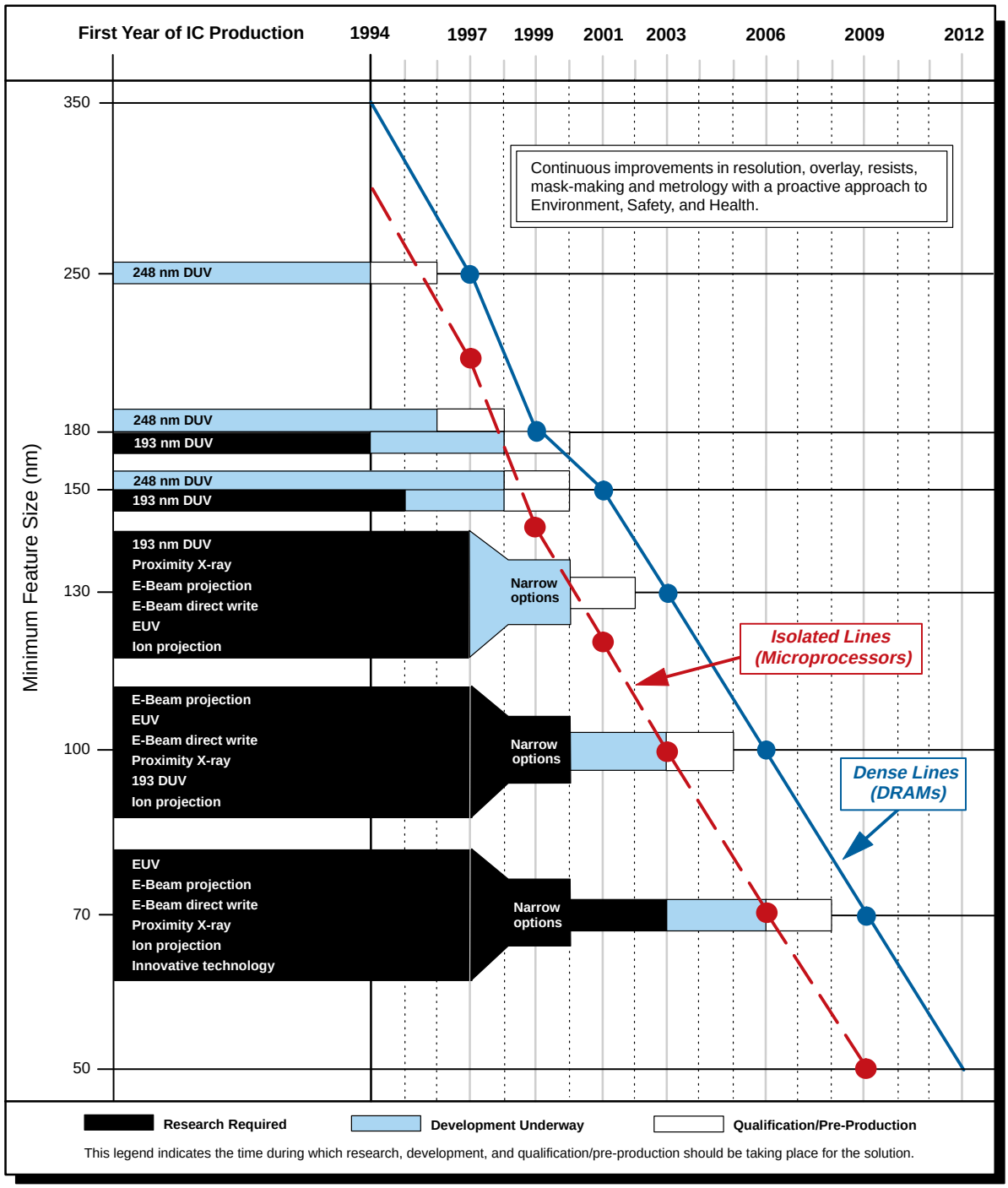
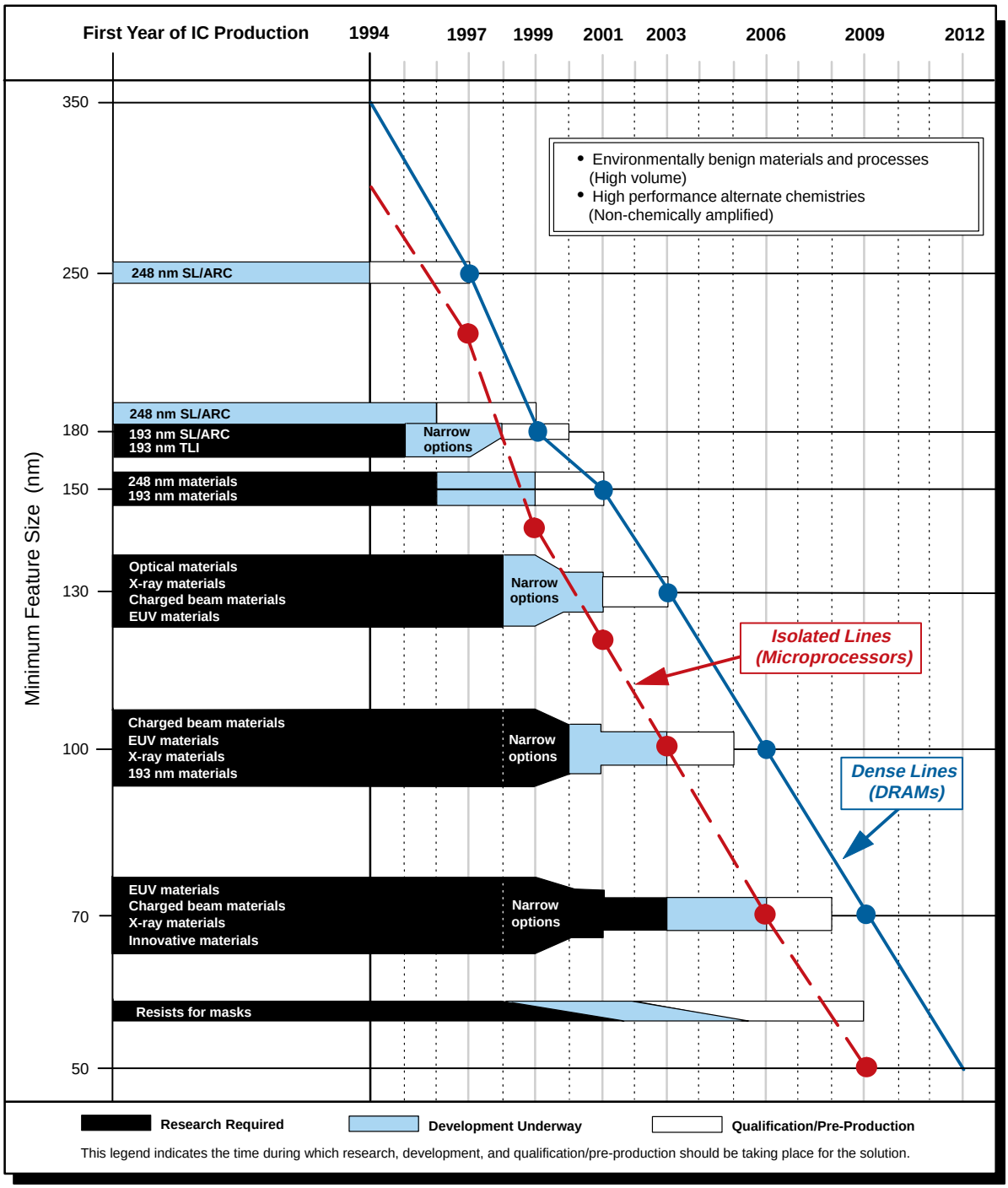
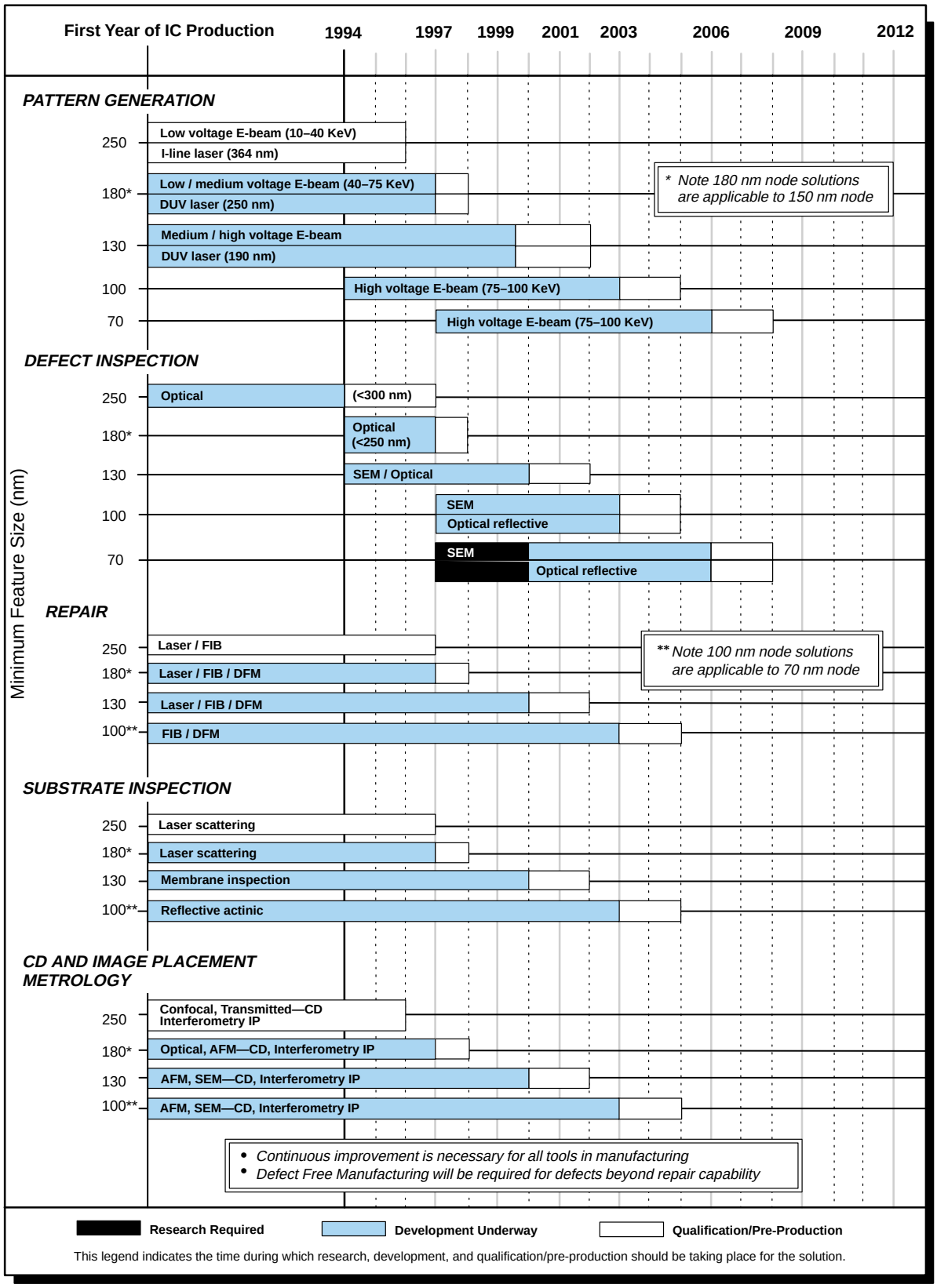


Figure 18 Critical Level Exposure Technology Potential Solutions



SL—single layer
ARC—antireflective coating
TLI—thin layer imaging

Figure 19 Critical Level Resist Technology Potential Solutions



SEM—scanning electron microscope
FIB—focused ion beam
DFM—defect free manufacturing
AFM—atomic force microscopy
IP—image placement

Figure 20 Critical Level Mask Technology Potential Solutions

CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions are defined in the following tables and figures:

- Lithography ESH Needs and Potential Solutions (Table 27)
- Lithography Defect Reduction Needs and Potential Solutions (Figure 21)
- Lithography Metrology Requirements (Table 28)
- Lithography Metrology Potential Solutions (Figure 22)
- Lithography Modeling & Simulation Needs and Potential Solutions (Table 29)

ENVIRONMENT, SAFETY, AND HEALTH

From the perspective of ESH, lithography is represented by four subject areas. These are lithography and mask manufacturing chemicals (e.g., photoresists, thinners, developers, rinses, and strippers); processing equipment (e.g., spinners, vapor-phase deposition systems, and silylation ovens); exposure equipment (e.g., DUV, E-beam, X-ray, and ion beam); and equipment cleaning. Of critical concern with respect to these areas and the implementation of new lithography technologies is the avoidance of showstopper problems (see Table 27). In particular, issues such as new process chemicals evaluation, compliance with environmental regulations, equipment safety, and worker protection must be considered before changes are made.

Table 27 Lithography ESH Needs and Potential Solutions

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*
Photolithography and Mask Manufacture Chemicals	Chemical toxicity, risk assessment, status under TSCA* for new chemicals, availability of adequate supplies, ability to monitor potential exposures, and emissions from processes (HAPs** and VOCs)	Preparation of a list of acceptable lithography chemicals based on evaluation of TSCA conformance; robust chemical selection criteria; risk assessment; and the use of pollution prevention principles Use of dry resist and aqueous resist technologies Use of additive technologies Use of benign materials§
Processing Equipment	Exposure to toxic materials, emission of HAPs and VOCs, hazardous waste disposal, cost of ownership, and energy consumption Ergonomic design of equipment, PFC† usage, and plasma byproducts§	Effective point-of-use abatement, optimization of tool exhaust, use of pollution prevention and DFESH‡ principles, specify supplier use of S2 and S8 standards Deployment of zero impact processes, elimination of the need for materials with significant global warming potentials, and utilization of DFESH tools in design for manufacture§
Exposure Equipment	Toxicity of chemicals, exposure to radiation, risk assessment, cost-of-ownership, hazardous energies, and beam shielding	Perform risk assessment and cost-of-ownership analyses Establish radiation protection programs as necessary
Equipment Cleaning	Solvent usage, emission of HAPs and VOCs, hazardous waste disposal, and personal protective equipment Selection of cleaners and cleaning methodologies§	Cryogenic cleaning, solvent free cleaning, dry resist technology, point-of-use abatement, pollution prevention, and optimization of tool design Redesign of processes and equipment to achieve minimal environmental impact§

* *TSCA—toxic substance control act*
** *HAPs—hazardous air pollutants*
† *PFC—perfluorocompound*
‡ *DFESH—design for ESH*
§ *Issues and potential solutions <100 nm/beyond 2006*

DEFECT REDUCTION

Figure 21 is intended to be a guide to enhance awareness of some of these defect reduction issues as the industry follows the 1997 Roadmap.

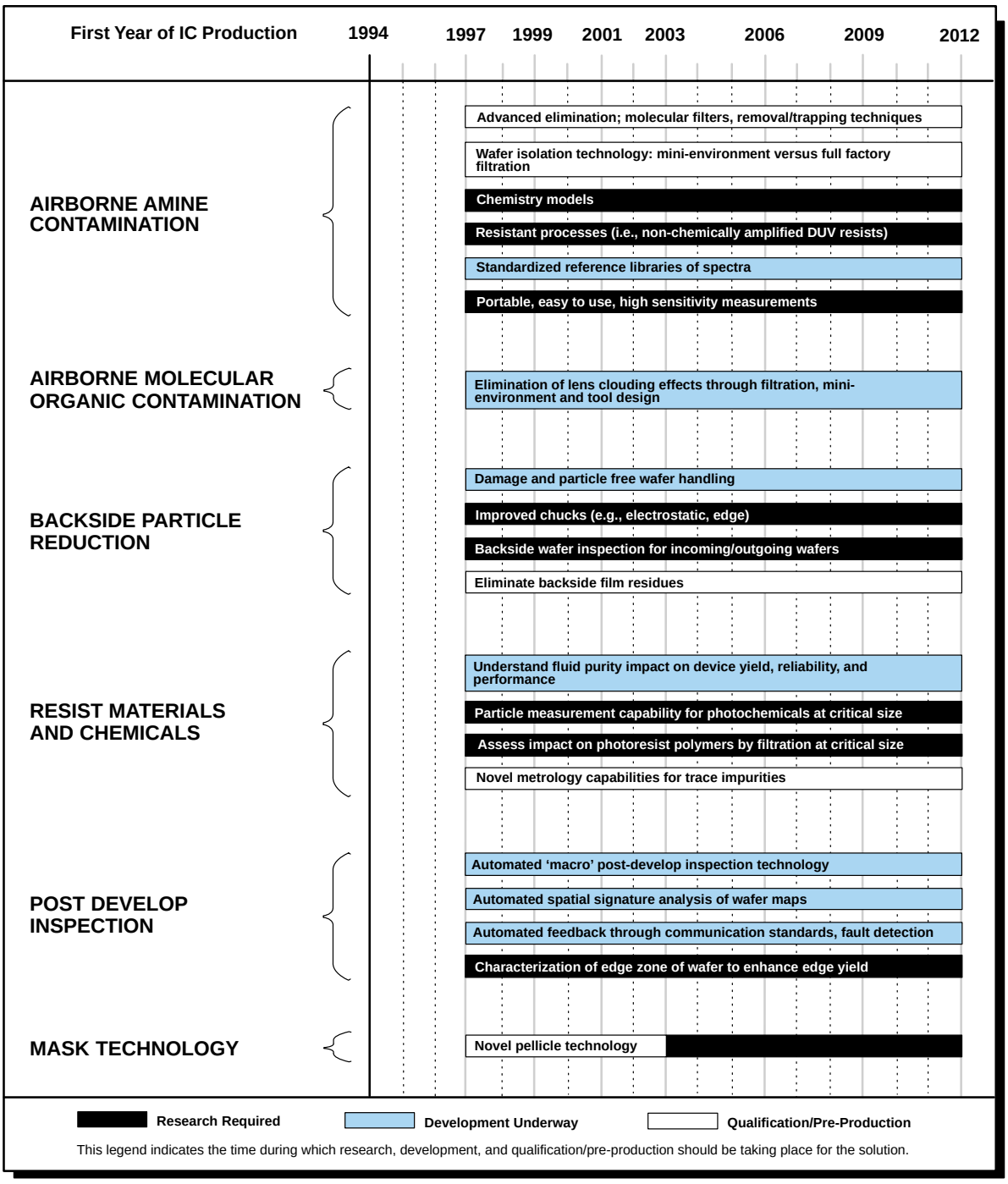


Figure 21 Lithography Defect Reduction Needs and Potential Solutions

METROLOGY

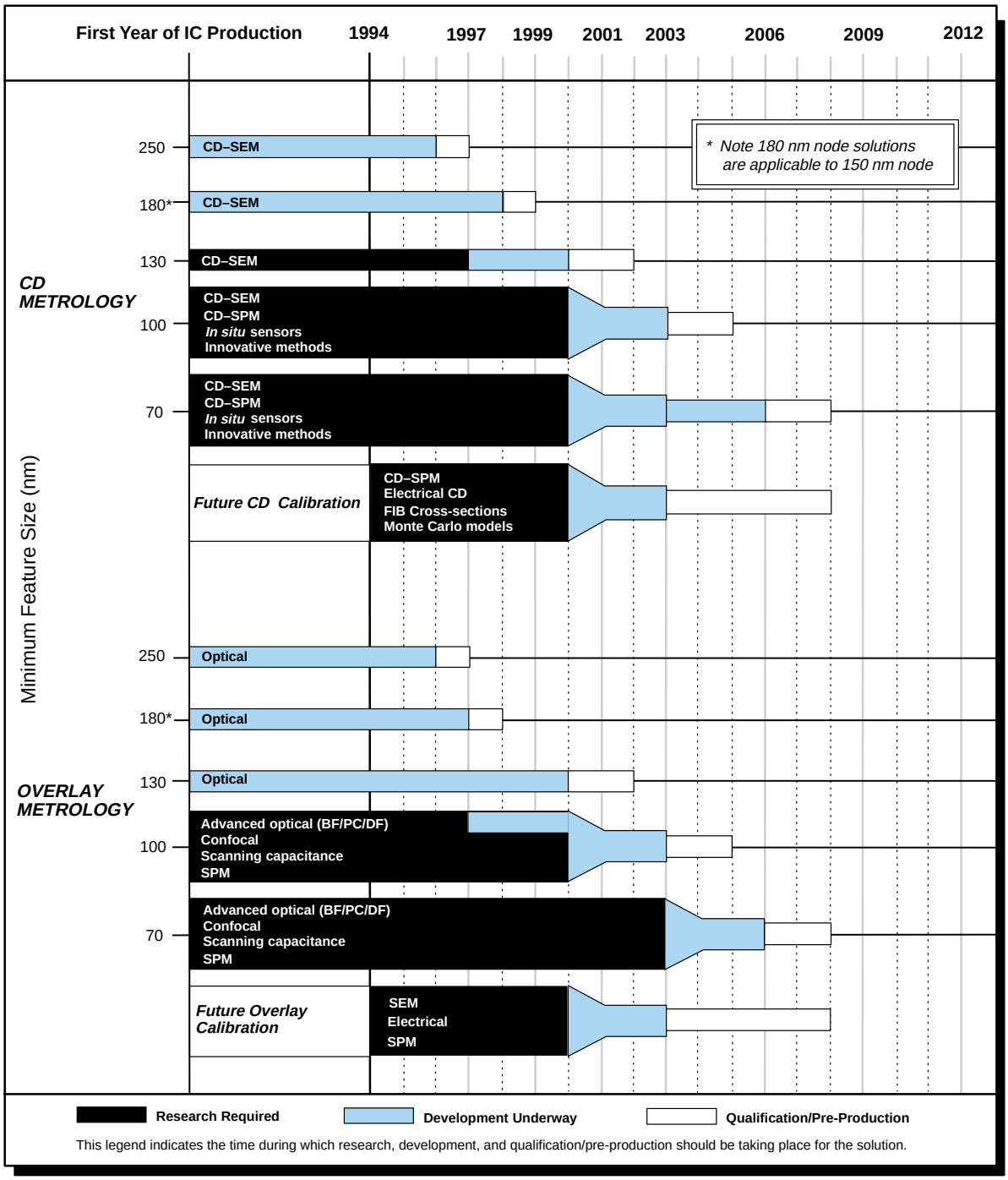
Physical metrology is challenged by the rapid advancement of lithography capabilities and is not meeting scheduled improvements for precision and reproducibility. CD metrology tool resolution, accuracy, tool-to-tool matching, and reproducibility all require significant advancement if they are to meet the goals stated in Table 28. Electrical measurements provide a monitoring of gate and interconnect linewidth, but only after the point where reworking the wafers is possible. Future overlay metrology requirements, along with problems caused by the low contrast levels, will drive the development of new optical methods along with scanning probe microscopy (SPM) and scanning capacitance microscopy (SCM). Statistical methods such as dynamic averaging are under investigation. Innovations, such as scatterometry sensor-based measurement, will require application development before being accepted. Further innovations are required, including those captured in the Metrology roadmap section on microscopy.

Table 28 Lithography Metrology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Gate CD control (nm)	20	14	12	10	7	5	4
Final CD output metrology precision (nm, 3 sigma) *	4	3	2	2	1.4	1	0.8
Overlay control (nm)	85	65	55	45	35	25	20
Overlay output metrology precision (nm, 3 sigma)*	9	7	6	5	4	3	2

Solutions Exist *Solutions Being Pursued* *No Known Solution*

** Measurement tool performance needs to be independent of line shape, line materials, and density of lines*



BF—bright field
PC—phase contrast
DF—dark field

Figure 22 Lithography Metrology Potential Solutions

MODELING & SIMULATION

Table 29 outlines the technology needs and potential solutions for Lithography modeling and simulation.

Table 29 Lithography Modeling & Simulation Needs and Potential Solutions

KEY AREAS	SUMMARY OF NEEDS	POTENTIAL SOLUTIONS
Resist Modeling	Predictive quantitative models, polymer surface interactions, coating and baking processes, silylation, edge roughness, E-beam, X-ray, and EUV resists	Establish mechanism-based models from basic studies on model materials Extend models to emerging materials Develop methodology for calibrating models on production tooling Validate models on 2-D and 3-D profiles
Optical System Modeling	Nonuniformity over field, resolution enhancements, and interactions with optical system nonidealities, global application of OPC* and PPC** to 10^8 features, photomask nonidealities, substrate reflections	Strategies and engines for transparent application of process and tool dependent OPC and PPC Engineering workbench TCAD*** tools for optical system level consideration of resolution enhancements and device pattern/transfer context Simulation of mask writing nonidealities and their impact on printing Calibration of simulators with profile SEMs† and statistical metrology
130 nm and Beyond	Image quality, overlay, throughput, and patterning/transfer in advance lithography systems based on EUV, X-ray, E-beam and maskless approaches, pattern dependence, stress and edge roughness in dissolution	Full system simulation of lithography tools with emphasis on balancing trade-offs in performance limiters such as resolution throughput, nonidealities in masks and mechanical and electrical components, materials inhomogeneities and transport effects in resists Simulation-based assessment of out-of-the-box approaches to maskless lithography
TCAD and Metrology	Implications of processing physics at the IC system design level, knowledge of manufacturing tolerance in simulating process design, technologist friendly tools, accurate interpretation of optical monitors, scanning probes and SEMs	Integration of TCAD with IC CAD‡ Integration of TCAD simulation with parameter extraction and statistical metrology of CIM§ Standard engineering workbench-based simulation environments Modeling of optical monitoring and SEM measurements

* *OPC—optical proximity correction*
** *PPC—process proximity correction*
*** *TCAD—technology computer aided design*
† *SEM—scanning electron microscope*
‡ *CAD—computer aided design*
§ *CIM—computer integrated manufacturing*

LITHOGRAPHY TWG–TO–TWG INTERACTIONS

The crosscut technology needs and Lithography TWG interactions with other TWGs are shown in Table 30. The technology and business complexities in delivering a total solution will require increased TWG-to-TWG and supplier interactions.

Table 30 Lithography TWG-to-TWG Interactions

TECHNOLOGY	*CROSSCUT ISSUE*
Modeling and Simulation	Improved capabilities for optical enhancements Resist modeling System overlay modeling
Materials	Optical materials Resist materials Mask substrates Advanced materials for precision mechanics
Environment, Safety, and Health	VOC abatement Solvent reduction Exposure tool safety standards
Process Integration, Devices and Structures	Reduced topography/planarization Design rule relaxations
Interconnect	Antireflection layers for optical lithography Better etch selectivity
Materials and Bulk Processes	Wafer flatness requirements Thin resist shortcomings for high energy implants
Design and Test	Design/layout software for optical enhancement techniques (OPC, PSM)
Factory Integration	Cost analysis for larger wafer sizes CoO targets versus business model assumption

POTENTIAL PARADIGM SHIFTS

The introduction of non-optical lithography will be a major paradigm shift that may be necessary to meet the technical requirements and complexities driven by Moore's Law This shift will drive major changes throughout the lithography infrastructure and require significant resources to commercialize the system.

Breakthroughs in direct-write technologies that achieved high throughput would be a significant paradigm shift. It would eliminate the need for masks, offering inherent cost and cycle-time reductions. Other technologies that eliminate the need for masks and resist would likewise constitute a paradigm shift.

SUMMARY

Optical lithography is the mainstream approach for the industry with global momentum behind extensions to the 130 nm generation. The key limit to extending optical lithography will be the gate CD control. Continued emphasis and resources are needed on 193 nm technology for the 180 nm and 150 nm generations.

Alternatives to optical lithography must be aggressively pursued to ensure the availability of cost-effective production-worthy systems. At 100 nm, the change to a non-optical lithography is likely to occur. Development of an advanced technology (X-ray, EUV, electron, or ion beam) must be accelerated for sub-130 nm generations. Improvements in mask making capabilities are necessary in most lithography approaches. Overlay requires significant emphasis for all generations below 250 nm. To achieve success, a systems approach is needed that develops the exposure tool, mask, resist, and metrology

concurrently. The cost to develop a single total system solution through to a commercially available tool and infrastructure is expected to approach one billion dollars. This necessitates a narrowing of the options in the near future to ensure a manufacturing solution on a timely basis. Achieving a global consensus on an affordable post-optical technology is the grand challenge for lithography.

The technology complexities and magnitude of investments in the future require a new global model for research, development, and commercialization. While lithography development is complex and expensive, the *leverage it provides is essential to the continued growth of the semiconductor industry.*

INTERCONNECT

SCOPE

Interconnect has been represented as the technology thrust with the largest potential technology gaps. The natural progression to copper metalization and low dielectric constant (κ) materials can provide cost reductions through process simplification but leads to a six-fold improvement in signal delay. The deviation from performance/price trends will occur as soon as the 100 nm technology node. The 1994 NTRS identified materials as key to addressing the performance bottleneck, however, materials solutions alone are inadequate to address the gap. Improvements in design and layout, including the use of smart routing and systolic arrays, must also occur. Chips will need wiring solutions that manage signal delay with the use of local clock control. Other solutions include 3-dimensional (3-D) devices and on-chip/off-chip optical interconnect. The interconnect portion of the chip will need to be viewed as an integral very large scale integration (VLSI) radio frequency (RF) system (including impedance control) as the nature of functionality migrates to mixed signal and analog circuits. Chip functionality will no longer be extrapolated from traditional performance scaling but through new 3-D and multi-level connectivity schemes.

DIFFICULT CHALLENGES

The most difficult anticipated interconnect challenges are associated with the material changes expected in the near future (copper and low κ dielectrics). These material changes will likely also drive process architecture changes (e.g., Damascene). Process integration using these new materials becomes progressively more difficult as feature sizes shrink below 100 nm. See Table 31.

Table 31 Interconnect Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Chip reliability	New materials and architecture (copper, low κ, Damascene) create some chip reliability exposure. Detecting, testing, modeling, and control of new failure mechanisms will be key.
Process integration	Integrating copper/low κ and aluminum/low κ with low cost, high yield, and acceptable reliability
Barriers	Barrier materials that address the integration issues identified with copper/ low κ
Dimensional control	Control of critical feature size and multi-layer film thicknesses is becoming an increasingly important predictor for circuit performance and reliability. Improved metrology, *in situ* process control, and CAD* techniques are needed to meet this challenge.
Low κ dielectric materials that meet integration requirements	Materials that simultaneously meet electrical, mechanical, and thermal requirements have been elusive

** CAD—computer aided design*

Table 31 Interconnect Difficult Challenges (Continued)

FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Dimensional control	Improved metrology, *in situ* process control, and CAD techniques are needed.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging. Dual-Damascene metal structures are expected to be especially difficult.
Barriers	The barrier material challenge becomes especially severe as feature sizes shrink. To take advantage of the low resistivity of copper, barriers must be very thin.
Solutions after copper and low κ	Although copper and low κ materials will be used for many years to come, other innovations will be required to meet future performance requirements.
FEOL** benign processes	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage (soft etch and clean) will be required.

* *CAD—computer aided design*
** *FEOL—front end of line*
*** *BEOL—back end of line*

Significant effort will be required to successfully integrate new materials into planned chip products at low cost and high yield. Finding a low κ material that meets all mechanical and electrical requirements will be difficult. A barrier material that is suitable for copper metalization is needed, and the thickness requirement becomes more severe with shrinking feature sizes. New chip reliability failure modes are anticipated with new materials and process architectures. Work must be done to test for and identify these failure modes, then model and control them. Many of the anticipated back end interconnect process modules are expected to be plasma intensive. Considerable planning and testing will be required to ensure that back end interconnect processing does not damage the front end device structures.

As the technology nodes migrate below 100 nm, high aspect ratio structures will be required. Etching and filling these structures is expected to be very difficult, especially for a dual-Damascene architecture. Dimensional control of critical feature sizes with multi-layer films will become increasingly important to assure circuit performance and reliability. Film properties in all directions must be controlled for unusual material configurations. Improved metrology, *in situ* process and material controls, and CAD techniques are expected to be required to meet this challenge. Aluminum, copper, and low κ materials will certainly be used for many generations. Copper and low κ materials are expected to enable the industry to meet signal delay requirements at least until the 100 nm technology node. Other innovations will be required to meet anticipated performance requirements (clock speed, circuit density, and cost) beyond the 100 nm technology node. Developing these solutions within the time frame of the expected need will be the most significant challenge for the interconnect area. Table 32 presents the interconnect technology requirements.

Table 32 Interconnect Technology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Number of metal levels—DRAM	2–3	3	3	3	3–4	4	4
Number of metal levels—logic	6	6–7	7	7	7–8	8–9	9
Maximum interconnect length—logic (meters/chip)	820	1,480	2160	2,840	5,140	10,000	24,000
Reliability—logic (FITs*/meter) $\times 10^{-3}$	4.9	1.7	1.3	0.9	0.5	0.2	0.1
Planarity requirements within litho field for minimum interconnect CD (nm)	300	250	230	200	175	175	175
Minimum contacted/non-contacted pitch—DRAM (nm)	550/500	400/360	330/300	280/260	220/200	160/140	110/100
Minimum contacted/noncontacted interconnect pitch—logic (nm)	640/590	460/420	400/360	340/300	260/240	190/170	140/130
Minimum metal CD (nm)	250	180	150	130	100	70	50
Minimum contact/via CD (nm)	280/360	200/260	170/210	140/180	110/140	80/100	60/70
Metal height/width aspect ratio—logic (microprocessor)	1.8	1.8**	2.0**	2.1**	2.4**	2.7**	3.0**
Via aspect ratio—logic	2.2	2.2**	2.4**	2.5**	2.7**	2.9**	3.2**
Contact aspect ratio—DRAM	5.5	6.3	7.0	7.5	9	10.5	12
Metal effective resistivity (μΩ–cm)	3.3	2.2	2.2	2.2	2.2	< 1.8	< 1.8
Barrier/cladding thickness (nm)	100	23	20	16	11	8	6
Interlevel metal insulator—effective dielectric constant (κ)	3.0–4.1	2.5–3.0	2.0–2.5	1.5–2.0	1.5–2.0	≤ 1.5	≤ 1.5

Solutions Exist *Solutions Being Pursued* *No Known Solution*

** FIT—failure in time*
*** Metal and via aspect ratios are additive for dual-Damascene process flow*

METALS POTENTIAL SOLUTIONS

The need to introduce new materials such as copper metalization and low κ materials will begin as soon as the 180 nm technology node. Aluminum alloy-based interconnect will continue to play a substantial role as the interconnect metal for at least 10 more years. The introduction of Cu will be in phases for some manufacturers, with the upper (fat) wiring levels first converted to Cu to accommodate the high current of those levels. The upper level Cu may be combined with low κ dielectrics and also may be fabricated using a Damascene or dual-Damascene approach. Copper will eventually appear in all metal levels, including first level metal, even though more understanding of the role Cu plays in contamination and integration is needed. The number of levels are extrapolated from the traditional scaling of 0.75 levels per technology generation; additional reference levels may be needed for logic products. Thermal conductivity is not considered a limiting factor through the 100 nm generation, even with the highest performance products using low κ dielectrics. Figure 23 shows the potential solutions for metals.

POTENTIAL SOLUTIONS ≥ 100 nm

The continued trend for even greater aspect ratios for contacts and vias suggests that chemical vapor deposition (CVD) and physical vapor deposition (PVD) solutions with conformal coverage and enhanced filling (void free) will be required. Designs can be influenced by via resistance and to obtain the best performances via resistance needs to be low and controlled. Limitations in cleans may negatively impact via resistance. Although Cu metalization will eventually become the dominant interconnect material, Al alloys will continue to play an important role for several generations. To accommodate

high aspect ratios, advanced Al fill techniques will be used. Potential solutions include high pressure Al fill, multi-step PVD Al fill, and blanket CVD Al. CVD Al can also be used as a seed layer for a follow-on PVD flow fill process. Selective CVD Al can be combined with either Al chemical mechanical planarization (CMP) or with a blanket PVD flowed Al process. Dimethyl aluminum hydride is the likely precursor and may be modified in various adduct forms for improved deposition performance. Both *in situ* doping with Cu, or post-deposition of AlCu or Cu followed by diffusion can be used to produce the AlCu alloy.

These Al processes will continue to use titanium nitride diffusion barriers. The TiN technology will evolve from the current PVD or collimated PVD techniques to either a CVD technique, or one form of the ionized PVD processes (post or self-ionized). Ionized PVD techniques may be used for filling, although they will need to be used in conjunction with a post-deposition planarization step with CMP or flowed Al.

Copper interconnect will likely be introduced using an electrochemical deposition process. The copper plating bath life must be extended and chemical measurement and replenishment or recycling addressed to reduce cost of ownership (CoO). CVD Cu is attractive because it can be combined with the barrier deposition on a single cluster platform. All of the CVD processes will require advancements in CoO and either precursor recycling or reductions in precursor consumption. Copper flow techniques, either PVD versions of the multi-step Al plug process, or post deposition thermal, or laser reflow require development efforts and may lead to cost-effective filling. Tantalum or tantalum nitride may be used as the barrier for electrodeposited Cu or CVD Cu. The Ta can be deposited by any of the enhanced PVD techniques, including ionized, or conformally using a CVD process. Thin oxides might also be used to enhance diffusion properties of these barriers. Titanium nitride may also find applications as a barrier for Cu, especially during the initial phase-in of Cu. Additional barriers such as TaSiN, WN, WSiN, etc. may find applications.

POTENTIAL SOLUTIONS < 100 nm

Currently envisaged potential solutions for 100 nm are to extend the use of Cu metalization, but these material solutions alone,are inadequate to meet the stated performance requirements. Design and layout must find wiring solutions that manage signal delay on a local scale. Other solutions include the use of 3-D devices and on-chip/off-chip optical interconnect. Research breakthroughs might allow the use of high temperature superconductors combined with lower temperature chip operation (Tc near 400 K), provided these materials can accommodate the current density requirements called out in the *Process Integration, Design, & Structures section, Reliability Requirements* (Table 17). For efforts such as superconductors or self-constructing systems to become reality, the challenge must be issued, but activity must be leveraged with existing research programs and focused to interconnect needs.

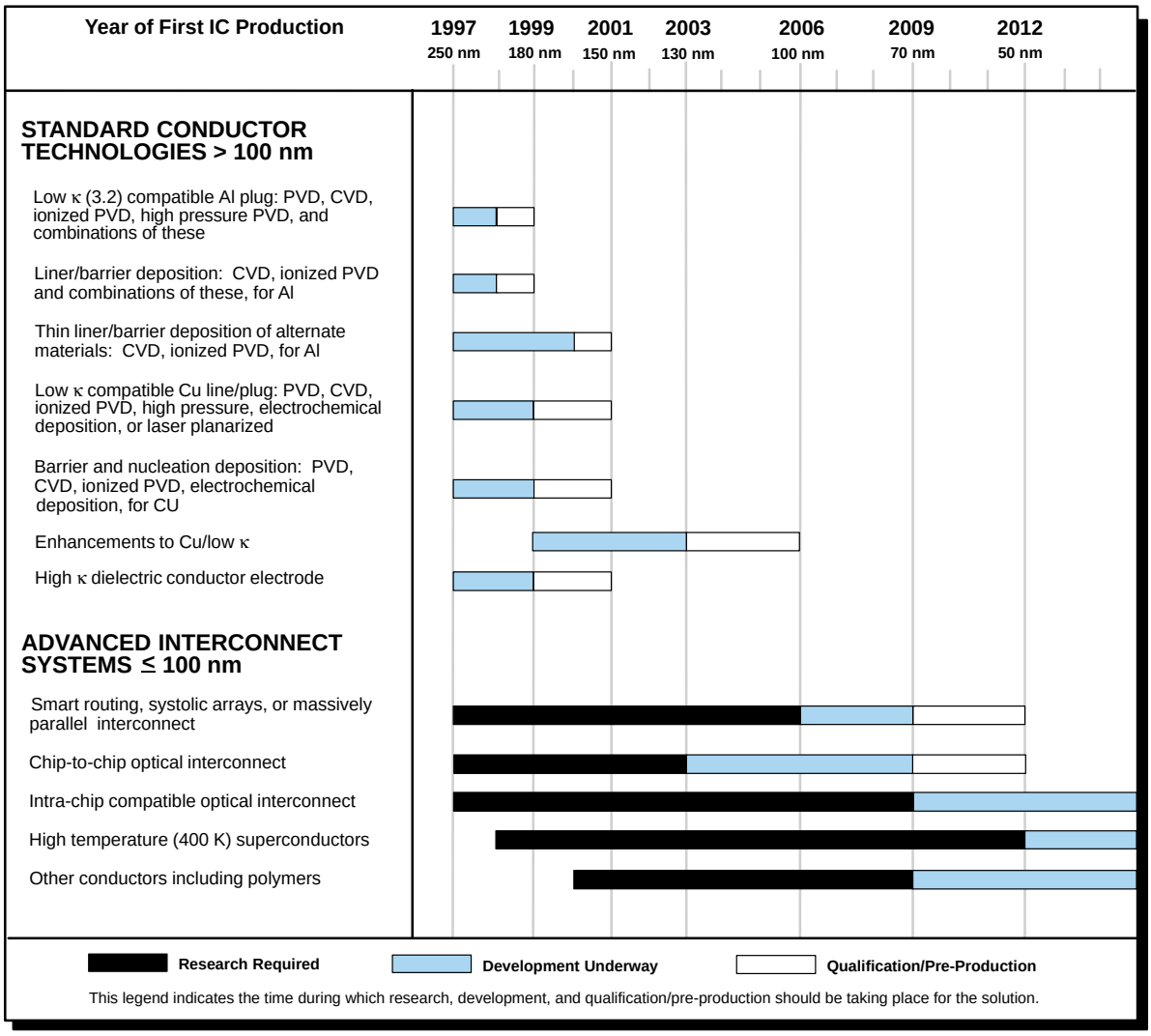


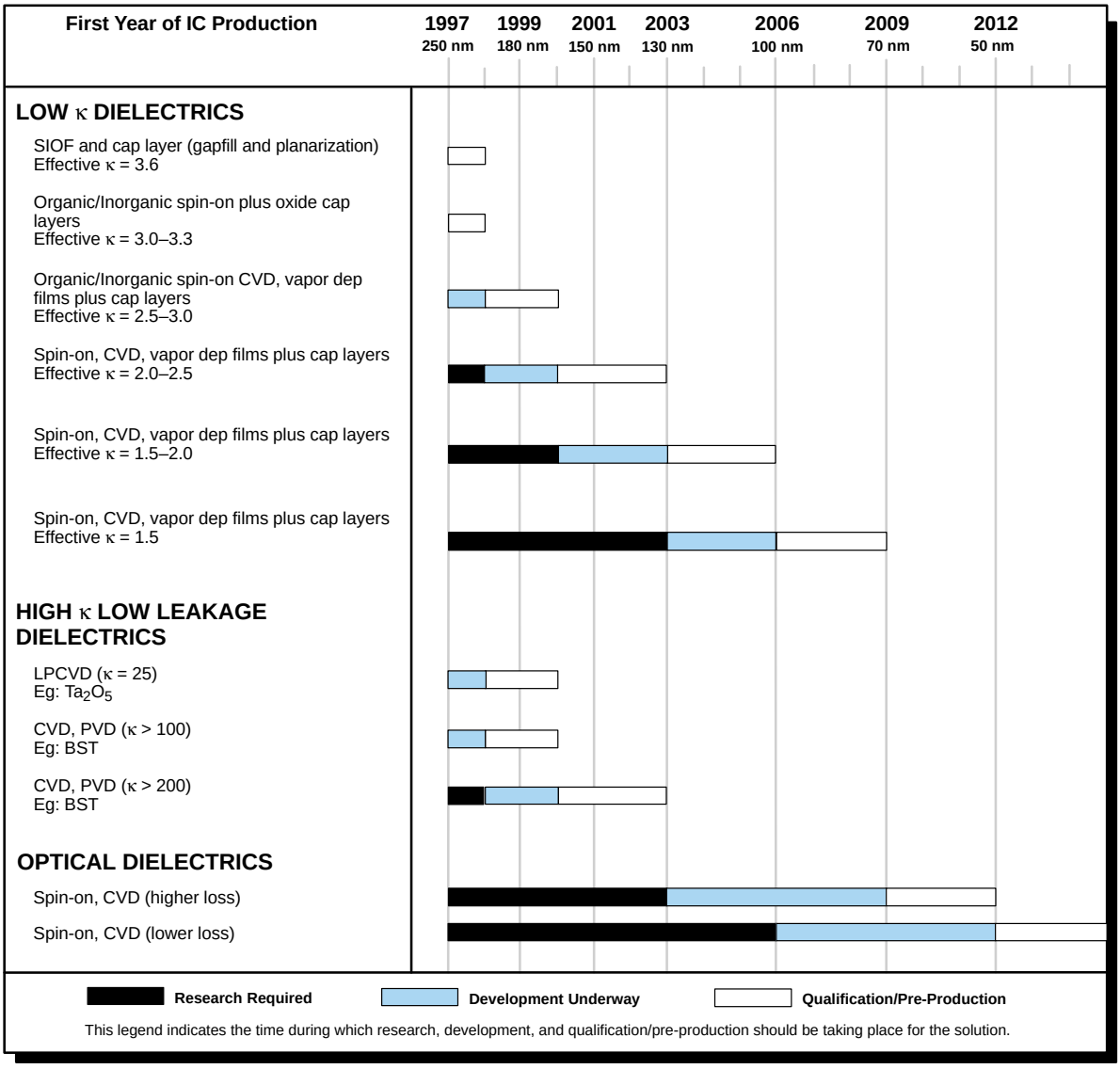
Figure 23 Metals Potential Solutions

DIELECTRICS POTENTIAL SOLUTIONS

DIELECTRICS REQUIREMENTS

As interconnect geometries continue to scale downward, interlevel dielectrics (ILDs) with lower permittivity (low κ) will be needed to reduce parasitic capacitance and crosstalk. Additionally, low leakage dielectrics with higher permittivity (high κ) will be required for DRAM storage node capacitors and on-chip filtering/decoupling. These new material requirements present formidable challenges for process integration and device reliability. For ILDs, material requirements and characteristics vary depending on process and structural constraints. For example, thermal properties of the dielectric must be consistent with subsequent processing temperatures and thermal conductivity requirements for heat transfer. Gapfill and dielectric planarization requirements for traditional ILDs are absent in the Damascene approach. New issues include mechanical strength requirements along with metal trench fill. Isotropic material properties are preferable; however, designers may be able to accommodate anisotropic materials with special structures. Since a single material solution is unlikely to serve all needs, a variety of materials and deposition techniques will be needed, and choices will depend largely on cost and performance goals.

The dielectrics potential solutions in Figure 24 lists the effective values of dielectric constant for the ILD stacks. Most of these approaches are equally applicable to subtractive and additive (Damascene) metalization structures. The expected introduction of copper interconnects by the year 1997 suggests that ILDs with an effective $\kappa < 2.5$ will be predominantly used in Damascene structures that do not require gapfill or thick capping layers for dielectric CMP. However, compatibility with copper CMP and deposition techniques will still be necessary.



SiOF—fluorinated oxide
LPCVD—low pressure CVD
BST—barium strontium titanate

Figure 24 Dielectrics Potential Solutions

In the near term, fluorine doped oxide and a variety of low κ spin-on dielectrics are being qualified for 250 nm production. However, at 180 nm lower κ materials ($\kappa < 3.0$) will be required to counter higher parasitic capacitance. New spin-on materials, as well as new CVD and vapor-deposited films, offer potentially lower κ solutions, and ideally these same materials and deposition techniques can be modified and extended to provide even lower values of dielectric permittivity. Once again, material and process decisions for interlevel dielectrics, along with back end structures will be driven by perfor-

mance and cost, but interconnect reliability is expected to play an increasing role as material properties change. Although a progression of decreasing dielectric constants is predicted, not every step will be adopted by every manufacturer. The lowest dielectric constant is desirable, but must be traded off with integration challenges; material changes at every generation are unrealistic and undesirable.

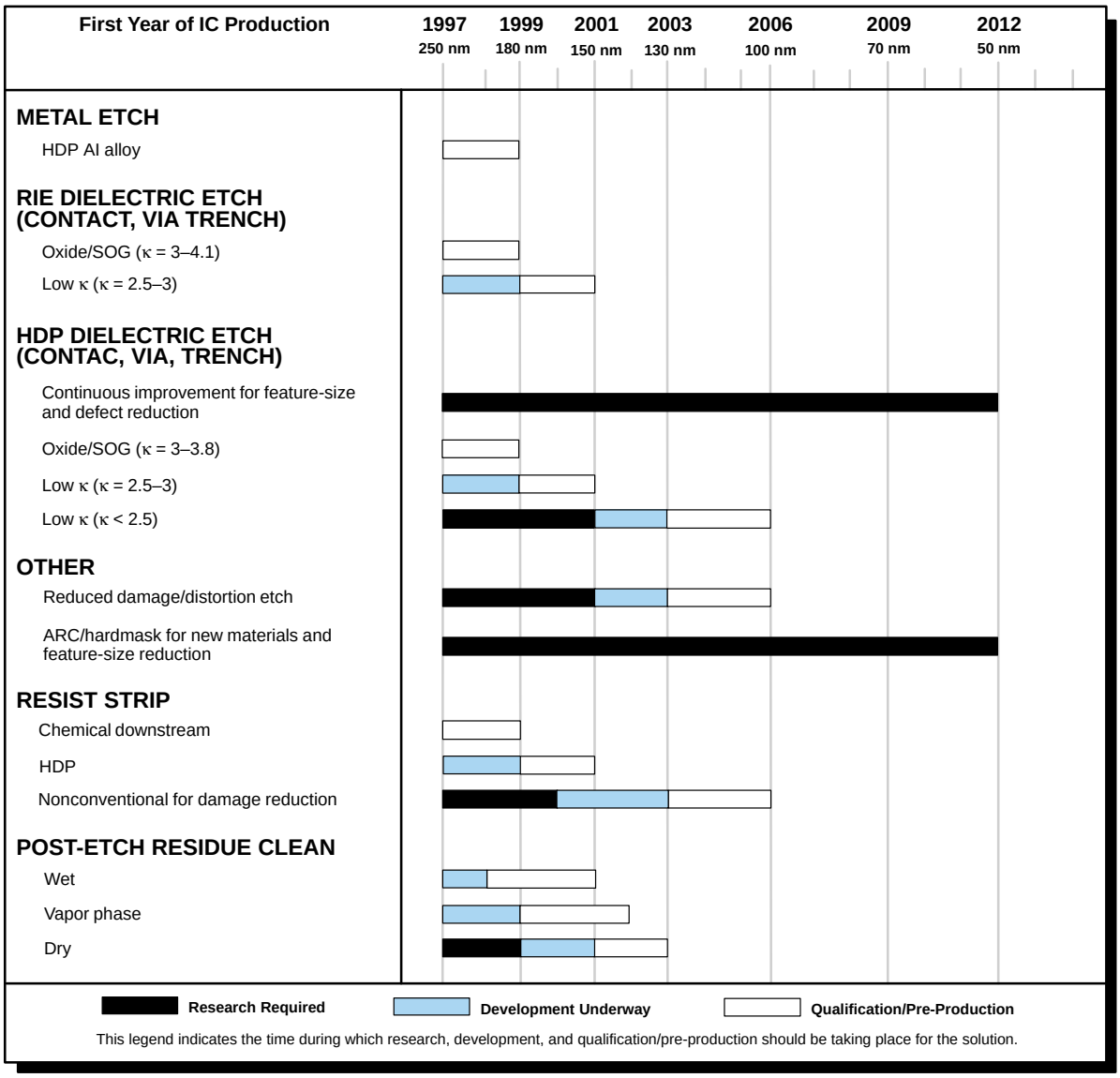
DRAMs will continue to provide the impetus for low leakage, high κ dielectric development, but high κ dielectrics may also find use in logic, mixed signal, or merged memory/logic devices as power supply filter capacitors, digital-to-analog converters, and isolation capacitors. Near term high κ material development is focused on CVD solutions with κ~25. Longer term solutions involve both PVD and CVD approaches with κ values of 100 or greater, while maintaining low leakage characteristics. Integration of new high κ materials will also drive the development of novel electrode materials.

ETCH POTENTIAL SOLUTIONS

ETCH REQUIREMENTS

High-density plasma (HDP), low-pressure etch tools are now being implemented in manufacturing for critical anisotropic etch steps. The driving force for this is the ability for high rate etching of small feature sizes with accurate dimensional control and minimal aspect-ratio-dependent etching (ARDE). The focus on HDP does not preclude extending existing technologies such as reactive ion etching (RIE) or high pressure etching. The control of charge-induced damage and selectivities to resist and underlying layers are essential features. A possible solution to reduce damage for some steps is neutral stream etching. Selectivity to nitride is particularly important for self-aligned contacts. The introduction of new interlevel dielectric materials (e.g., organic low κ, fluorine-doped oxide, and aerogels) will necessitate the development of new, selective etch chemistries. See Figure 25.

Damascene and dual-Damascene processes will require new trench etch processes in interlevel dielectrics, for which surface morphology may be an issue. Hard masks may be required for organic dielectrics, and also to accommodate thin resist layers. Significant work on both wet and dry cleans for residue removal is needed. Copper and low κ materials add new concerns about residues, but the requirement for low and controlled via resistance remains. Approaches to reducing the CoO include more extensive use of modeling/simulation in tool design, process monitoring and control, and *in situ* cleans. ESH considerations will necessitate the development of etch processes using feedstocks with lower global warming potential than many currently in use.



SOG—spin-on glass
ARC—anti-reflective coating

Figure 25 Etch Potential Solutions

PLANARIZATION POTENTIAL SOLUTIONS

Chemical mechanical planarization will be the dominant method of planarization for shallow trench isolation, interlevel dielectrics, and metals. The changes in CMP processes and tools serve several technology nodes, but are dependent on the generic process being implemented. Presently, the industry needs new tools and processes designed for Damascene metal signifying a trend away from ILD planarization. There is a synergy between process nonuniformity at etch and deposition, and in-field planarity at CMP. Continuous improvement efforts are expected to reduce costs and environmental issues and raise yield. Figure 26 shows CMP protential solutions.

SHALLOW TRENCH ISOLATION

Chemical mechanical planarization is presently being used in manufacturing to planarize shallow trench isolation (STI) structures. There is opportunity for new processes or CMP consumables to reduce cost and improve process control.

ILD PLANARIZATION

Dielectric CMP is needed to be employed for etched metal process flows. Pattern dependent thickness variation makes via etch more difficult and produces less predictable ILD capacitance. The use of dummy metal, HDP oxide, improved pads, slurries, and polishing tools may alleviate this problem. Low κ dielectrics will be employed on etched metal and may or may not be capped with a material more amenable to CMP. Chemical mechanical planarization may adversely change the bulk properties of low κ materials and these effects need to be thoroughly investigated.

DAMASCENE METAL

Tungsten Damascene processing of plugs and local interconnect structures is likely to continue indefinitely, constrained only by line and plug resistivity. Aluminum Damascene may be employed to alleviate problems with aluminum etch and difficulties planarizing low κ dielectrics over etched metal. To realize the benefits of copper, CMP of copper and underlying barrier films could be employed universally. Fortunately, the ILD thickness variation problem with etched metal is greatly reduced with Damascene; the challenge is controlling metal thickness through minimization of dishing and erosion for a given range of pattern densities.

Solutions to this problem are anticipated through the development of film structure and composition, polish tools, polish pads, slurries, and process parameters. Tools capable of at least two sequential CMP steps with different consumable sets are desirable. Low κ dielectrics may need to be capped with thin dielectric films serving as stop layers and/or moisture barriers. Film interfaces must be strong enough to withstand the mechanical stress of CMP.

All metal Damascene structures may be susceptible to corrosion of the metal or the underlying films by the CMP process, clean, or subsequent processing. Defects due to particulates or scratches will need to be continually reduced.

GENERIC CMP

Various optical and electrical endpoint systems are emerging for dielectric and metal CMP to facilitate control. *In situ* thickness metrology must be built into the CMP tools to monitor the process drifts and provide automatic control.

Post-CMP cleans, both mechanical and chemical, are being devised to remove abrasives, chemicals and CMP by-products from the wafer. Integrating the post-CMP clean into the CMP tool will occur when the reliability of the separate tools is proven, cleans are well defined, and the combination provides reduced CoO. A variety of modular clean capabilities designed for a particular tool will facilitate rapid introduction of integrated post-CMP clean.

Defect metrology for CMP is presently not well established, especially for patterned wafers. Distinguishing between scratches of different depth and particles, without operator intervention, may need tools and/or software specifically designed for CMP. Defect metrology will become more difficult as geometries shrink.

The waste streams from CMP tools will contain a variety of environmentally adverse contaminants. Ideally, the CMP processes must be designed to reduce the consumption of these materials; metals (especially Cu) from Damascene structures will wind up in the waste stream and extraction methods will be necessary to remove them. Planarization alternatives to CMP may be developed to address the stated issues with CMP, as well as to reduce cost and improve process capability.

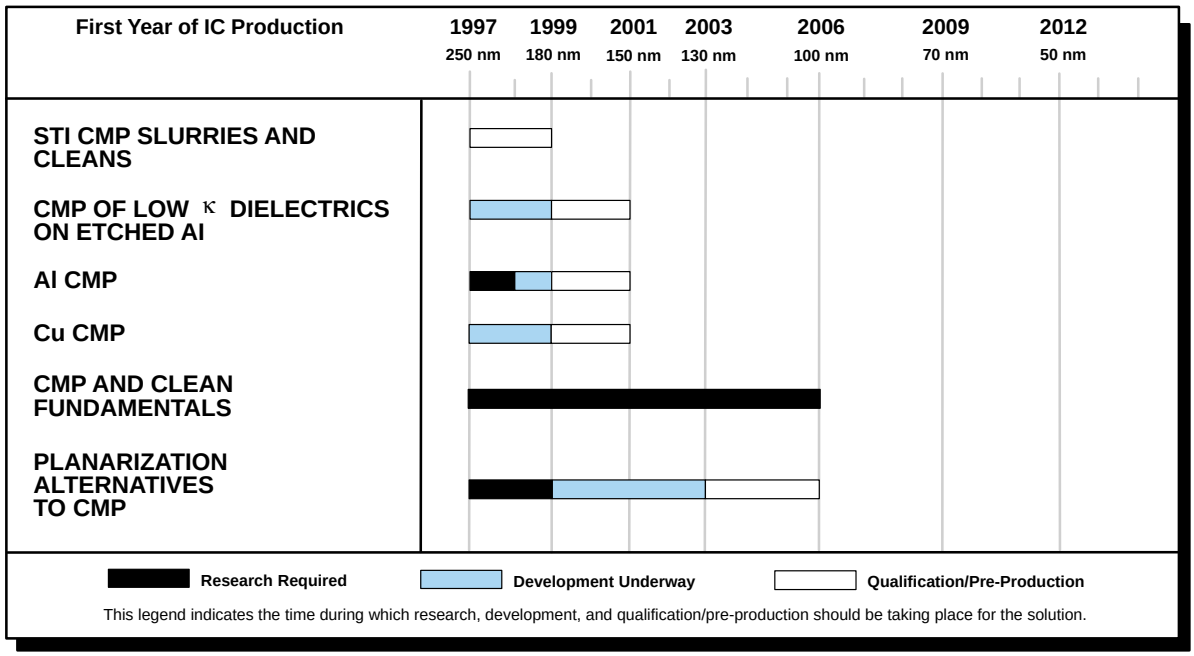


Figure 26 Planarization Potential Solutions

ARCHITECTURE POTENTIAL SOLUTIONS

REQUIREMENTS

Interconnect technology will more severely impact the performance, density, and yield with future reductions of feature size envisioned for sub-micron integrated circuits. Since more than half of the chip fabrication process budget is already absorbed by interconnect, it is crucial to develop new architectures that improve device performance and manufacturability. New interconnect architectural approaches must be realized in 1) material systems and processes used in the interconnect construction and 2) physical connectivity of the materials that are dictated by design. Both will be required to help meet future device needs. The future state of interconnect technology from a materials and connectivity perspective will reach an impasse within the next two to three generations of technology (~100 nm).

POTENTIAL SOLUTIONS

The use of Cu and lowest possible (κ~1) dielectric will provide, at best, a signal delay improvement of 6×. Work on integrating these materials in production-worthy processes is in progress. The potential of making further order of magnitude improvements in interconnect capability will be accomplished primarily through design. Interconnect systems that are structured properly (such as neural network implementations) could have much greater computational bandwidth and higher yield due to their inherent robustness to defects. System interconnect design that takes advantage of waveform shaping and propagation should also be addressed to reduce cross-coupling between close proximity wiring. The design area of interconnect architecture needs much greater future focus to achieve greater computational density and performance. See Table 33.

Architectures employing new high Tc superconductors would provide a dramatic breakthrough in interconnectivity. A dramatic improvement could be realized if architectures employing fine line on-chip optical interconnect were available. However, development of devices having high efficiency electro-optical conversion for receiving and transmitting signals is also required. The ability to self construct interconnect systems in two and three dimensions is a highly attractive concept in the earliest stage of development. A number of major technological breakthroughs will be required to have this approach seriously considered for interconnect applications. Breakthroughs in this area may come

from other peripheral fields dealing with genetics or biotechnology. Superconductors and biotechnology are revolutionary examples and there is no evidence that these concepts could be implemented.

Table 33 Architecture Potential Solutions

POTENTIAL SOLUTIONS—SOME OR ALL OF THE BELOW NEED TO BE REALIZED BY 2012			
Architecture/Device	*Signal Propagation*	*Connectivity*	*Packaging*
3-D	Low temperature operation	Self construction	Multi-chip module
	Optical	Fault tolerant	Area array
		Neural wiring	Functional partitioning

RELIABILITY POTENTIAL SOLUTIONS

MULTI-GENERATIONAL

Increases in product reliability have slowed since 1993 as aggressive scaling continues and traditional materials are being pushed to their limits. The need to reduce signal delays through the interconnects will require the replacement of the traditional aluminum-alloy metals and oxide interlevel dielectrics with new materials—copper and low κ dielectrics. Prevention of further erosion of product reliability as new materials are introduced will require rapid circuit design, materials, and process learning. An integrated, multi-disciplinary approach for multiple generation solutions is needed.

The rapid learning required for these material introductions makes the development of an optimized, best-practice measurement tool set more important. This tool set is needed to characterize the reliability of the interconnect system and to develop predictive reliability models. It is also critical in helping to identify and ultimately to control the key parameters that affect product reliability in circuit design, materials, processing, and processing equipment. *In situ* sensors and other metrology tools are essential in identifying and ultimately controlling these reliability-affecting parameters.

The emphasis on pre- and in-process controls offers the best means for achieving optimum reliability and performance. It permits progressive reductions in process variations and the development of multi-generational reliability solutions. With this emphasis on building-in reliability through informed design and control, the use of time-consuming, expensive, and imprecise end-of-line tests can be reduced to a minor role. This approach will permit a more rapid time-to-market and the use of more realistic measures of product reliability, based upon design and process.

The introduction of new materials and their interactions will present significant reliability challenges related to deposition, stability, and integration. Diffusion barriers for copper interconnects must be very thin and still remain impermeable to copper. These and other new films must be compatible with and have good adhesion to any contiguous materials/films. The relatively low thermal conductivity of low κ dielectrics may present reliability problems associated with heat dissipation on the chip beyond the 100 nm generation.

Metrology improvements are needed to develop an understanding of the interactions of the constituent materials, processes, thermal history, and equipment. Basic understanding of interconnect films and the metrology to achieve this understanding is lacking. In particular, improved experimental and modeling techniques for characterizing the mechanical and interface adhesion strengths are needed.

Significant gaps and deficiencies in the tool set exist for reliability test structures and methods. Characterization of electromigration in sub-micrometer sized lines, contacts and via structures under DC, and pulse current conditions will be required. Filling these gaps will require a better, commonly accepted understanding of the effect of accelerated stress conditions on the interconnect system. More accurate estimates of the stress test acceleration factors are needed to extrapolate test results to actual use conditions. Standard test structures or methods need to be developed to characterize the susceptibility of interconnects to stress voiding and to study the synergistic effects of electromigration and stress voiding.

Computer-aided design tools will need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure-mechanism understanding and modeling, which result from the use of improved test metrologies, be utilized to provide the input data for these new CAD tools. With these data and reliability CAD tools, the impact on product reliability of design selections can be evaluated.

New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect lines and vias resulting from 1) line length; 2) current densities expected for the currents required by the circuit; and 3) calculated local operating temperature that includes the effects of joule heating in the circuit element and elsewhere among the metal levels. Such tools will need to become an integral part of the circuit designer's tool set to help predict product reliability before processing begins and to develop solutions that anticipate coming technologies and thereby accelerate their introduction.

CROSSCUT NEEDS

ENVIRONMENT, SAFETY, & HEALTH

The interconnect area poses unique environment, safety, & health (ESH) challenges. Because technology development demands it, the industry is seeing a proliferation of new chemicals being evaluated in the areas of low κ, advanced metalization, and CMP. Many new chemicals are not Toxics Substances Control Act (TSCA) listed and little information is available about their toxicity. Being able to qualify new chemicals for use in production volumes is a potential showstopper for interconnect. Perfluorocompounds (PFCs), one of a number of types of greenhouse gases, are used almost exclusively in interconnect. The industry must strive to minimize PFC emissions via process optimization, alternative chemistries, and recycle and abatement so that these gases remain available for industry use. The increased requirement for CMP will result in interconnect becoming a major user by volume of both chemicals and water. Efforts must be made to reduce chemical and water requirements.

Major ESH issues affect all areas of Interconnect as indicated in Table 34 and Table 35:

Table 34 Interconnect ESH Crosscut Issues

MAJOR ESH ISSUES	*POTENTIAL SOLUTIONS*
Chemical Management Proliferation of new chemicals	Define a process to conduct thorough new chemical reviews and ensure that new chemistries can be utilized in manufacturing without jeopardizing human health or the environment or delaying process implementation. (1998)
Poor chemical utilization efficiency	Optimize chemical utilization efficiency through use of endpoint sensors or other means to reduce reactor sidewall deposition. (1998)
Natural Resources Resource requirements for support equipment	Optimize/reduce energy costs associated with plasma systems. (2003)
Worker Protection Potential employee exposure during cleans or preventative maintenance	Develop minimal ESH impact *in situ* cleans. (>2006)
ESH Design Tools Difficulty quantifying ESH factors	Develop a simple, comprehensive risk model which can be used to evaluate new chemistries and processes. (2000)

In addition, ESH solutions are needed for issues related to specific development areas of Interconnect.

Table 35 Key Interconnect ESH Issues

INTERCONNECT AREA ISSUES	*POTENTIAL SOLUTIONS*
Low κ	
VOC emissions from spin-on process	Solvent management for spin-on low κ materials (1998) Develop ESH benign low κ process. (2003)
Unknown process emissions	Develop emissions models for vapor phase systems. (1998)
Planarization	
Large volume of potentially hazardous materials used and disposed	Decrease amount of slurry required for CMP. (1998) Develop slurry recycling. (2000) Develop ESH benign slurries. (2000) Eliminate slurry. (2003)
Large volumes of water required in CMP and post-CMP cleans processes	Reduce water consumption. (1998) Develop water recycling systems to reuse CMP and post-CMP cleanup wastewater. (2000)
Advanced Metalization and MOCVD (including Al, Cu barriers)	
Inefficient chemical utilization	Develop chambers with less sidewall deposition. (2000)
New process chemistries	Identify safety and health issues associated with precursors. (1998) Develop safe precursor delivery systems. (2003)
Limited understanding of process emissions	Determine if fine metal praticulate emissions are a concern. (1998) Characterize emissions. (2000)
Cu Plating and Related Processes	
Generation and disposal of potentially hazard wastes	Extend Cu plating bath life using monitoring and replenishment. (1998) Develop techniques for bath recycling. (1998)
Amount of waste generated	Minimize quantity of rinse water. (1998)
New tool development	Develop zero impact plating processes. (2000) Develop process tools which minimize employee exposure to chemicals. (1998)
Hazardous chemistries for electroless plating	Develop and utilize chemistries with safer substitutes for cynanide and formaldehyde. (1998)
High κ	
Precursor materials not determined yet	Utilize precursors with lowest ESH impact. (1998)
Plasma Processes	
PFCs identified as global warming gases	Process optimization/increased gas utilization for PFCs. (1998) Develop alternative chemistries for PFCs that do not emit PFCs. (2006) Develop low CoO PFC abatement and recycle systems. (1998) Minimize PFC emissions via recycle or abatement. (2000)
Chamber cleans utilize hazardous chemicals	Develop minimal ESH impact *in situ* cleans. (2006)
Emissions not fully characterized	Develop predictive plasma emissions models. (2000)

DEFECT REDUCTION

The *Interconnect* and *Defect Reduction* sections of the NTRS exhibit a very strong crosscut interdependency. Yield loss due to contamination and field failures will continue to occur with higher frequency in the back end of the line than in all other manufacturing operations combined. Issues common to interconnect and defect reduction include ultra-small particle detection (<< 100 nm) and detection of scratches in transparent dielectrics, rationalization of defectivity targets, particle detection in trenches and at via sidewalls/base, and detection of defects in complex layered films. Detection of submerged voids in vias and contacts will become increasingly important, as will the problem of distinguishing defects from voids in highly porous dielectric films.

Issues with new materials and structures also present special problems, such as problems in novel spin-on dielectrics, including bubbles, striations, shrinking, cracking, and delamination. Problems associated with CMP of soft metals (e.g., Cu) include pitting, corrosion, and chemical etching. Integration issues, such as delamination of Cu from the dielectric, must also be addressed. Implementation of copper interconnect technology will also require trace-level real time metrology to establish acceptable copper levels and copper contamination vectors in the fab and backside to frontside metal contamination transport.

Via and trench etch requirements will dictate highly isotropic etches for vertical wall profiles, generating organic residues on the sidewalls and bases of these structures. The effectiveness of high temperature and/or high pressure Al or Cu reflow techniques to achieve integrated metalization will depend on the wetting characteristics of sidewalls and bases of trenches and vias. Acceptable wetting will require effective removal of etch residues. Effective post trench and via etch cleans and subsequent surface prep treatments to facilitate nucleation layers for electroplated copper and CVD of silicides, barriers, and via/trench fills will be one of the most challenging requirements facing implementation of advanced metalization techniques.

To achieve fundamental understanding of processes and material behavior in interconnect tools, numerical modeling will be utilized to realize inherently clean tools and processes. Effective particle repulsion techniques, such as thermophoresis, will become a necessity as killer particles strongly increase in number with shrinking linewidths. Avoiding gas phase particle nucleation in reactors will require detailed knowledge of parameters such as local temperature, pressure, concentration, flow rate, etc. at many points within the tool for which sensor deployment is impractical. Even when sensor use is appropriate, numerical modeling will be necessary to guide sensor placement and to relate sensor readings with on-wafer particle measurements. Better understanding of process chemistry regimes will be needed to help reduce the rate of residue build-up on chamber walls and subsequent flaking, increasing mean-time-before-cleaning. Modeling and trace-moisture sensor technology will guide protocols and processes to reduce chamber recovery time. Sensors, such as fiber optic monitors, must be developed and refined to alert operators to film build-up and incipient flaking conditions within CVD reactors and sputtering chambers. Impurity specifications in critical materials used in dielectrics and metalization will become increasingly important for materials such as CMP slurries, low or high κ dielectric materials, and novel barrier and conductor materials.

METROLOGY

Interconnect metrology for the production environment relies on physical measurements and limited electrical measurements to assure process control and integrated circuit electrical performance. Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the inline metrology measurements for interconnect structures are made on monitor wafers (unpatterned), or rely on destructive techniques. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires nondestructive measurement on patterned wafers. As wafer processing covers more of the area close to the wafer edge, metrology tools will also be required to have reduced edge exclusion. Large diameter wafers and the requirement for increased stability from equipment and processing will drive more inline and *in situ* measurement techniques (see the *Metrology TWG* section). With the advent of more stringent process control requirements, materials used to construct process chambers need improved metrology (e.g., high frequency dielectric constants).

The new materials being pursued for metalization and dielectrics, and the new architectures (Damascene) will require new measurement technology. Time-to-market considerations for Damascene interconnects may require additional metrology measurements during pilot line and early production to compensate for immature processing. A better approach would be to have metrology available for characterization in the development stage so that robust processes are transferred to production. Areas

of concern with the new materials and architectures are as follows: in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), line resistivity (versus bulk resistivity), availability of high frequency dielectric constant values, and test structure design for high frequency (≥ 1GHz). Calibration techniques and standards need to be developed in parallel to be available at the same time the metrology system is ready. Imaging of the bottom of a contact or via and determining the sidewall slope can be done in an engineering intensive mode, but rapid imaging is still impossible with current microscopy. Additionally, measurement tools need to easily locate and measure the one contact of interest in millions of contacts on one chip and send the data on to the next measurement tool, data analysis system, and fab data systems.

The goal of inline film thickness measurement is rapid measurement of individual film layers on a product wafer with patterned interconnect layer stacks (i.e., smaller illuminating spot sizes) at many locations on the wafer. Current film thickness methods such X-ray fluorescence, optical reflectivity, ellipsometry, profilomotery, and microbalance do not meet this goal. New methods for measuring multiple film layers in production using laser stimulation of acoustic and thermal waves at this time require test structures in the scribe region between chips.

CRITICAL MEASUREMENT NEEDS

Design of interconnect structures requires measurement of the high frequency dielectric constant of low κ materials. High frequency testing of interconnect structures must characterize clock harmonics (5× to 10× base frequency), skin effects, and crosstalk effects. Other metrology needs include measuring resistivity (sheet ρ) at high frequency, measurement of adhesion, and measurement of mechanical strength. Also needed are imaging of high aspect ratio structures for process control, and endpoint for CMP, including Damascene/copper processes.

FACTORY INTEGRATION

SCOPE

Historically, the semiconductor industry has maintained steady productivity growth (25–30%/year reduction in cost/function) despite escalating factory costs (20%/year). The industry growth has been driven by improvements to feature size, wafer diameter, yield, and factory productivity (equipment and operations). However, annual gains from yield and wafer diameter are diminishing, thus requiring greater emphasis on factory productivity. As a result, increased significance must be placed on fully exploiting equipment and operational productivity through advanced factory integration technology.

To achieve the levels of factory productivity needed to maintain the historic cost curve, the factory must be viewed as a technological business entity defined by four fundamental challenges and eight technology areas. Table 36 defines the four significant difficult challenges facing semiconductor factories. The eight technology areas that address the collective technology defined as Factory Integration are:

- Product and Material Handling Systems
- Process and Equipment Control
- Manufacturing Information and Execution Systems
- Operational Modeling and Simulation
- Productivity Analysis
- Facilities Infrastructure
- Human Resources
- Software Improvement

DIFFICULT CHALLENGES

Table 36 Factory Integration Difficult Challenges

DIFFICULT CHALLENGES	*SUMMARY OF ISSUES*
Factory Cost	Escalating factory capitalization and operational costs
Operational Effectiveness	Low productivity of semiconductor equipment and manufacturing operations
Factory Investment Risk Management and Time Factors	The rapidly diminishing time allowable to recover initial and recurring factory investments
Process/Factory Complexity	Increasingly difficult data, material, process, and technology management in an increasingly interdependent environment

FACTORY COST

For the industry to remain on the historic cost improvement curve the affordable packaged unit cost per function must decrease 24% per year for microprocessors and 29% per year for DRAMs. These challenging projections present a need to optimize wafer cost/cm^2 with each generation of feature size. Factory capital costs have a major impact on cost/cm^2 and have been increasing at a compounded annual growth rate (CAGR) of 20% resulting in capital costs/cm increases of 15% per year. These costs are driven by the increasing cost of the complex tools, the process complexity, and wafer size increases. With tool capital costs increasing toward 90% of the total factory investment, depreciation (5-year straight line) will approach 45% of the wafer cost/cm^2. A key element in the strategy to remain on the historic improvement curve is a modest 1%/year continuous improvement in operating cost/cm^2.

OPERATIONAL EFFECTIVENESS

Productivity analyses (conducted by SEMATECH) completed for 250 nm and 180 nm feature sizes and for 200 mm and 300 mm wafer diameters indicate that reductions in feature size and increases in wafer diameter are not sufficient to keep the industry on its historic 25–30% manufacturing cost learning curve. As a result, improvements in developing, purchasing, and operating equipment are required. A measure of this improvement is overall equipment effectiveness (OEE). Operational measurement will evolve from single tool OEE measurements to a measurement of the average tool OEE throughout a factory and ultimately to an overall factory effectiveness measurement. These OEE measurements will be complementary to cost-of-ownership (CoO) and throughput measurements. Improving on all of the operational measurements is a shared responsibility of both the manufacturing companies and the supplier companies. See Table 37.

Today, the OEE improvement focus is on bottleneck tools. However, with the cost of equipment approaching 90% of factory capital costs, the average tool OEE will become significant as such tools can collectively cost hundreds of millions of dollars. OEE requires improved software reliability, advanced process and equipment control techniques (to detect and correct faults, reduce monitor wafer usage, and optimize tool throughput), enhanced equipment integration, and performance tracking.

Exceeding 65% OEE (without adversely impacting cycle time and inventory levels) requires significant improvements in factory planning/scheduling, better modeling tools for assessing and optimizing capacity, increased flexibility of tool granularity, as well as improved equipment reliability. These parameters must be optimized to each IC manufacturer's business model.

Table 37 Operational Effectiveness Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Bottleneck tool OEE (%)	65	73	80	87	89	91	92
Average tool OEE (%)	45	52	59	65	71	76	80

Solutions Exist *Solutions Being Pursued* *No Known Solution*

FACTORY INVESTMENT RISK MANAGEMENT AND TIME FACTORS

Trends in the amount of time needed for factory construction, tool installation, and factory ramp are in conflict with future needs. Exponential growth in factory cost is creating an exponential increase in factory investment risk. More incremental, or modular, approaches to factory construction and start up are needed to reduce long start-up times and spread massive capital investments. See Table 38.

MINIMUM ECONOMICAL CAPACITY INCREMENT

In the early 80's, factories producing 8K wafer starts per month (WSM) were commonplace. During the mid-90's, much larger factories (20K WSM) have become the norm. This trend toward larger factories indicates that efficient and profitable factories will be sized at 30–40K WSM in the near future. Efficient operation accompanying large factories has dictated relatively large increases in initial and additional factory capacity for each change in feature size and wafer diameter. This trend must be mitigated by means of a more modular approach to factory construction and utilization. Smaller, more modular, "just enough, just-in-time" increments of capacity should allow factories to better match revenue generation, improve return on investment, and reduce risk.

TIME TO FIRST WAFER START

Elapsed time from factory groundbreaking to first wafer start has doubled during the last twelve years. To reverse this trend, the elements of factory construction and production preparation must be shortened in duration and performed in parallel.

YIELD RAMP

DRAM product yield learning has improved with each new product generation and must improve even more rapidly in the future. Future initial yield levels must be much higher and the rate of improvement must be much faster for each successive product generation.

OVERALL EQUIPMENT EFFECTIVENESS RAMP

Typical bottleneck tools have initial OEE levels of 45%. A total productive manufacturing (TPM) improvement project can improve that performance by about 1%/month to a level 65%. This is the minimum required OEE for a 250 nm/200 mm factory to maintain the historic manufacturing productivity curve. This 18-month TPM cycle is roughly eight months longer than the typical tool installation and qualification cycle in a factory start-up. As a result, first-year productivity is unacceptably low. Bottleneck tool OEE levels must be achieved in cycle times less than (or equal to) the total months consumed by tool installation and qualification (by 2012, this will be three months). This, coupled with increasing demands for higher bottleneck tool levels at future technology nodes, results in the need for a quadrupling of the average monthly OEE improvement rate by the year 2012. To accelerate this OEE ramp, best practices need to be identified, structured into an OEE improvement roadmap, and propagated throughout the semiconductor community. To reach the defined OEE targets, the industry also requires a higher, more productive initial OEE when equipment is delivered to a manufacturing site.

Table 38 Factory Investment Risk Management and Time Factors Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Minimum Economical Increment of Capacity (WSM)	20K	20K	20K	10K	10K	5K	5K
Time to First Wafer Start (months)							
Factory design time	6	6	5	4	3	3	2
Construction time	10	10	9	8	7	7	6
Tool selection and delivery time	10	10	9	8	7	7	6
Tool installation and qualification	10	9	7	6	5	5	3
Total time to first wafer start	23	21	18	15	13	12	10
Production Ramp Time (months)							
0 to 5K WSM	3	3	3	2	2	2	1
5K to 10K WSM	3	3	2	2	1		
10K to 20K WSM	3	2	2				
Max time to min economical capacity	9	8	7	4	3	2	1
Yield Ramp (DRAM probe yield w/repair)							
Initial yield level (%)	25	50	70	80	85	88	90
Time to mature yield level (yrs)	4	3	2	1	0.8	0.6	0.5
OEE/OFE Ramp							
Initial bottleneck tool OEE (%)	45	48	52	55	60	70	80
Months to target bottleneck tool OEE	18	16	14	12	9	6	3
Monthly OEE improvement (% points)	1	1.5	2	2.5	3	3.5	4
Initial average tool OEE (%)	30	31	32	35	44	55	68

OFE—overall factory effectiveness

Solutions Exist *Solutions Being Pursued* *No Known Solution*

PROCESS/FACTORY COMPLEXITY

SEMICONDUCTOR MANUFACTURING SYSTEMS

The number of process steps needed to complete an IC is projected to more than double by 2012. The complexity associated with process difficulty and the increase in process steps is driven by advancing

IC design requirements, increasing wafer size and value, and more demanding process physics. As a result, the decision quantity and quality required of manufacturing personnel will dramatically increase. A useful measure of manufacturing system complexity is computer integrated manufacturing (CIM) system function points. A CIM system currently contains approximately one apparent function point (i.e., the decisions made by the system user) for every 23 actual function points (i.e., computer-assisted decisions) embedded within the CIM system decision support tools—generating a function point ratio of 1:23. The productivity of computerized decision support tools must improve by almost 6× during the next 15 years.

ADVANCED DECISION SUPPORT TOOLS

Software is increasingly called upon to enhance manufacturing performance. Highly advanced decision support tools are needed to present processed data to decision makers as trends, recommendations, and even automated decision implementations. The proliferation of computerized decision support tools throughout manufacturing systems as well as the need to integrate many of these software applications has added a new area of complexity to the manufacturing environment. This trend will accelerate in the future. The computerized decision support tools available to the engineers and managers who are operating these highly complex, interrelated systems are not keeping pace with factory complexity. The result is data overload. Research is needed to develop useful metrics for tracking escalating manufacturing complexity and for tracking the yield rate for converting data into actionable knowledge.

TECHNOLOGY REQUIREMENTS

Table 39 Factory Integration Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Facilities Infrastructure							
Factory effluent reduction (% of 1988 baseline)	50%	50%	80%	80%	80%	90%	90%
Product and Material Handling							
Loaded carrier weight (lbs.)	7.5	18	18	18	18	42	42
Carrier volume (cu. ft.)	1.1	1.1	2	2	2	5	5
AMHS* availability	99.0%	99.5%	99.8%	99.8%	99.8%	99.9%	99.9%
Process and Equipment Control							
# Test wafers/# product wafers	33%	28%	23%	15%	10%	6%	5%
# Predictive fails/# total fails	5%	10%	20%	30%	40%	60%	80%
Manufacturing Information and Execution Systems							
Software integration costs (multiplier of software cost)	3–10×	3–5×	2–4×	1×	0.5×	0.5×	0.5×
Minimum system function points	7,000	9,000	12,000	15,000	22,000	30,000	40,000
Shop floor bandwidth (Mbps)	10	100	200	500	1,000	1,000	1,500
Software Improvement							
# Software fails/# total fails (new equipment)	32%	25%	20%	16%	13%	10%	8%
Size of equipment software (lines of code)	600,000	750,000	1,000,000	1,250,000	1,500,000	2,000,000	2,500,000
Modeling and Simulation							
Model development—data collection (labor hours)	15:1	14:1	12:1	8:1	4:1	2:1	1:1
Modeling data requiring manual management (%)	0.8	0.7	0.5	0.25	0.1	0.05	0.05

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *AMHS—Automated material handling systems*

POTENTIAL SOLUTIONS

PRODUCTIVITY ANALYSIS

Productivity analysis through cost modeling and simulation provides valuable understanding to improve productivity, leading to optimized investment and operating cost in the following key areas.

CAPITAL PRODUCTIVITY

Tool performance requirements need to be established for all feature size and wafer diameter generations. Industry efforts and methodology must also be expanded for tracking and driving these improvements to ensure the industry remains on the historic improvement trend.

INVESTMENT RISK REDUCTION

Tool lead time reduction and synchronizing it with construction time is a significant solution to reduce risk. Tool lead time can be improved by designing tools that utilize standard components, subassemblies, software, and platforms. Suppliers must provide more capable standard and pre-qualified tools, and adopt standard installation configurations. Enhanced product design tools must reduce yield learning cycles to first pass success. Construction time can be improved by developing and adopting standard modules and prefab elements of the factory infrastructure.

CAPACITY AND COST SCALING

Excess tool capacity is an extra cost in new factories and a cost penalty for smaller or modular factories. Surplus capacity also has a negative impact on productivity because of the need to manage the output of nonbottleneck tools. Mismatch between tool throughputs and the necessity to add tools in whole units results in excess capacity and capital investment. Potential solutions include designing tools based on standard increments of capacity; providing more versatile tools that perform multiple processes; and providing modules of optimized cost and capacity.

VARIABILITY REDUCTION

Full factory single-wafer processing provides the potential to reduce variability and thus reduce work in process (WIP) and cycle time. Enhanced simulation tools described in the Operational Modeling and Simulation section will provide capability to understand and manage sources of variability. Figure 27 presents potential solutions to improve productivity and optimize investment cost.

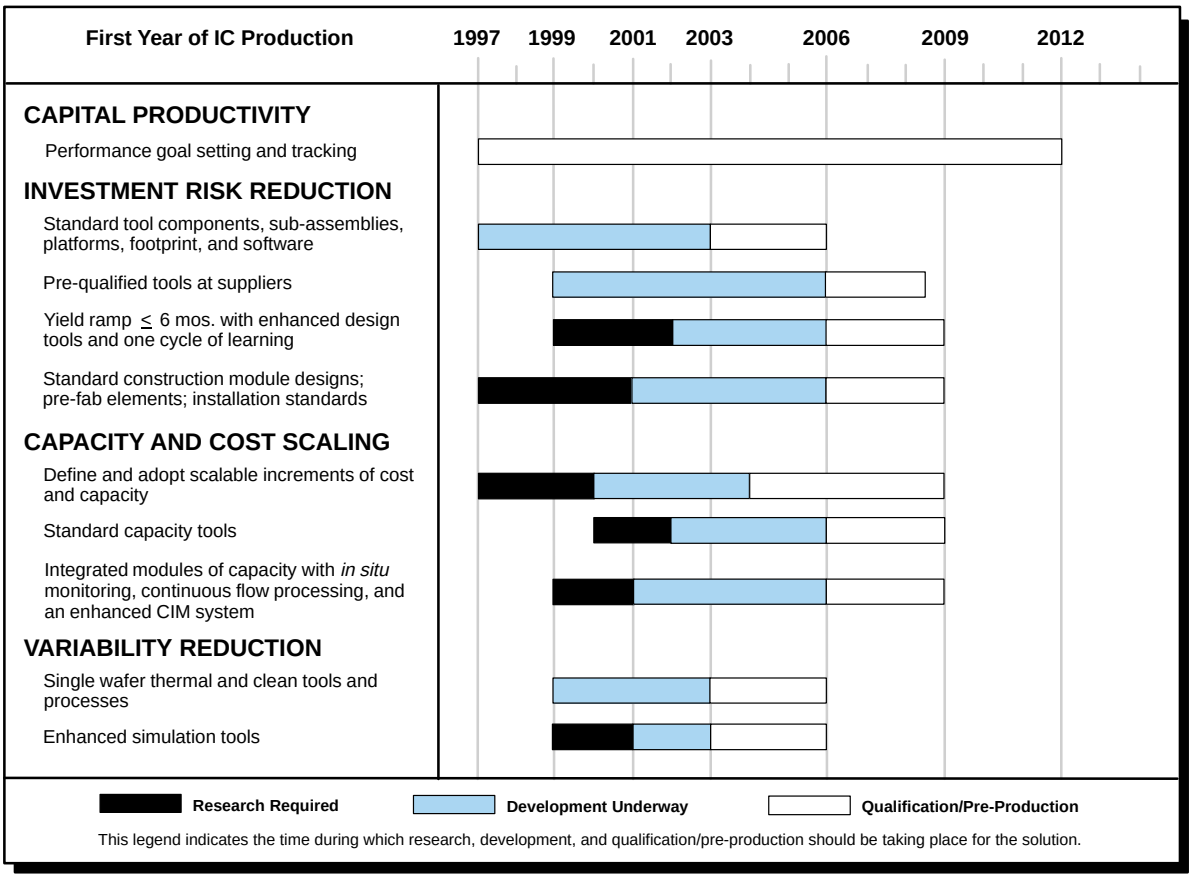


Figure 27 Productivity Analysis Potential Solutions

FACILITIES INFRASTRUCTURE

Reductions in process fluid, water, and energy consumption will become key elements of cost-effective factory operations. As process tool cost and thus factory capital requirements escalate, rapid tool installation and qualification become critical to achieving revenue and time-to-market goals. Replacing existing regionalized building codes with a national or even global code will facilitate rapid replication of successful factory designs to new locations, lowering factory cost and increasing time to market. Conditions in the factory that directly affect the wafer must be specified and controlled in cost-effective ways. This includes systems for control of environmental conditions and delivery of facility services. See Figure 28.

New paradigms are needed in tool and factory design efforts with respect to conservation of limited resources. Without these advances, natural resource consumption will increase, driven by greater tool complexity and the need for more tools to handle an increasing number of process steps. To maximize future benefits, strategies for reuse, recycle, and reclaim must be evaluated and included in the early stages of tool and factory design.

Opportunities exist with 300 and 450 mm factories for international standardization of key facilities service interfaces, components, procedures, and performance specifications. Standards reduce customization and increase both process tool and facility modularity, thus reducing the time and cost associated with procurement, installation, operation, repair, and replacement.

Building codes can influence many attributes of the wafer factory. These codes are often based on outdated system capabilities or nonsemiconductor applications. Active involvement by industry professionals is needed to modernize code language and maximize factory design options. Additionally, new insurance or asset loss containment strategies will be required to maximize options for next generation factories.

The industry must quantify the direct effect of facilities performance specifications on semiconductor processing and on systems reliability to avoid costly over specification in future facilities.

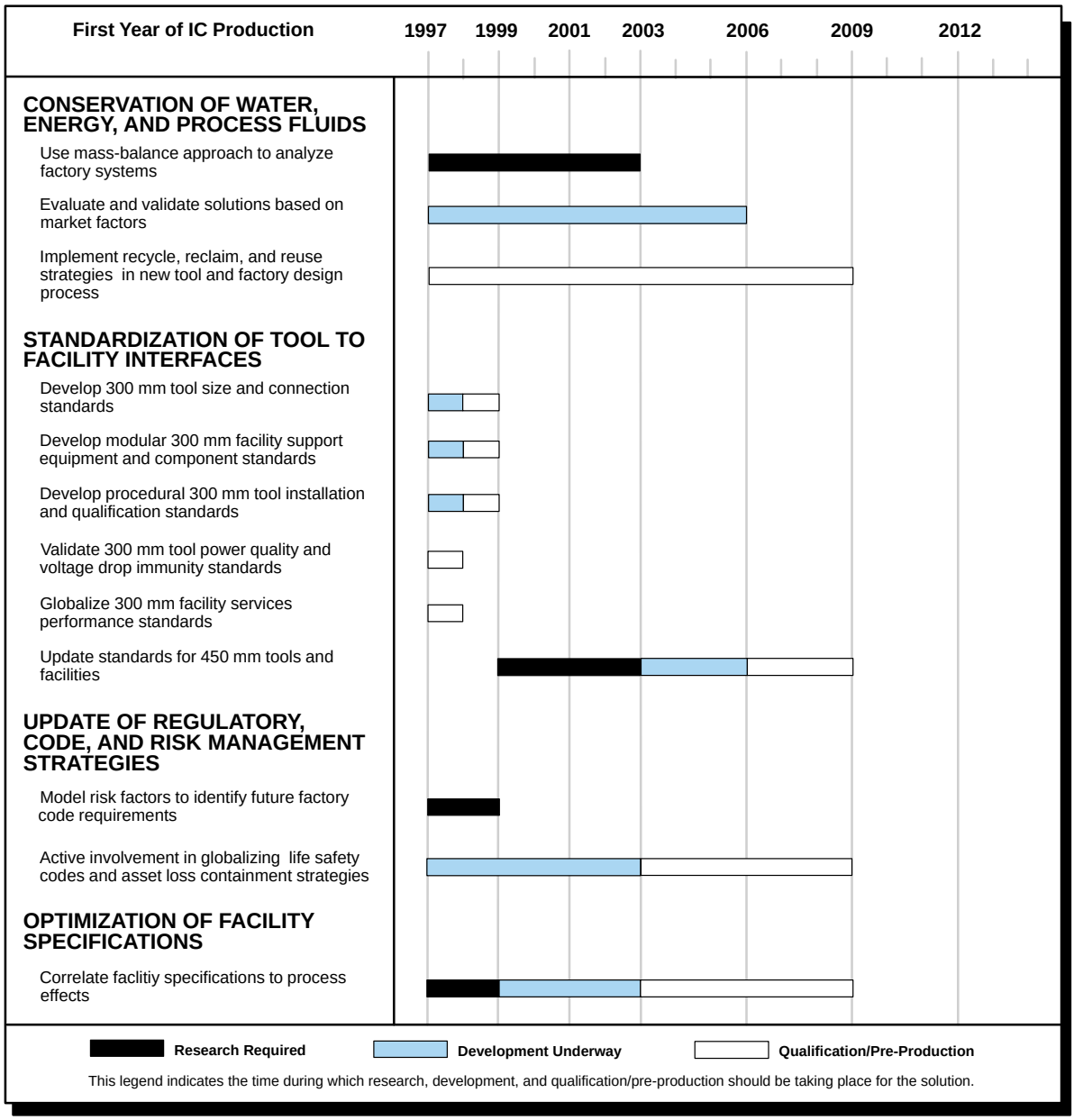


Figure 28 Facilities Infrastructure Potential Solutions

PRODUCT AND MATERIAL HANDLING

This section addresses the solutions to reduce idle no-operator and idle no-production impacts on OEE. IC manufacturers need to increase their tool utilization by having a factory system schedule and deliver products to the tools. See Figure 29.

FULLY AUTOMATED TOOL-TO-TOOL PRODUCT HANDLING

Automation reduces operational variability, increases factory safety, and reduces cleanroom space requirements (footprint). Full realization of these benefits requires tool-to-tool product and material handling automation systems. The economics and ergonomics of 300 mm factories demand that automation systems have very small footprints and be capable of moving heavy, extremely valuable loads. Standard mechanical and data interfaces must be used to shorten system installation cycles. Bay-to-bay automation is used in most new factories while automated or manually assisted tool loading will be needed in 300 mm factory installations by 2001.

MATERIAL CONTROL SYSTEM

Larger, more complex factories, with longer, more complex process routings and larger wafers demand higher levels of functionality from automation control systems. The material control system (MCS) must provide fault tolerance, standard communication/data interfaces, enhanced computing performance, enhanced scheduling capability, application interchangeability, multi-site/multi-system integration features, tool interfaces, resource dispatching, unified graphical user interfaces (GUI), automated self-diagnostics, standard interfaces to manufacturing execution systems, automated error recovery capability, and resource allocation prediction.

PRODUCT TRACEABILITY

Maintaining detailed information about each wafer as well as data about individual chips on each wafer will become necessary. Automated product traceability requires that detailed information about each wafer and the area on each wafer be sensed, mapped, and provided to higher level information systems.

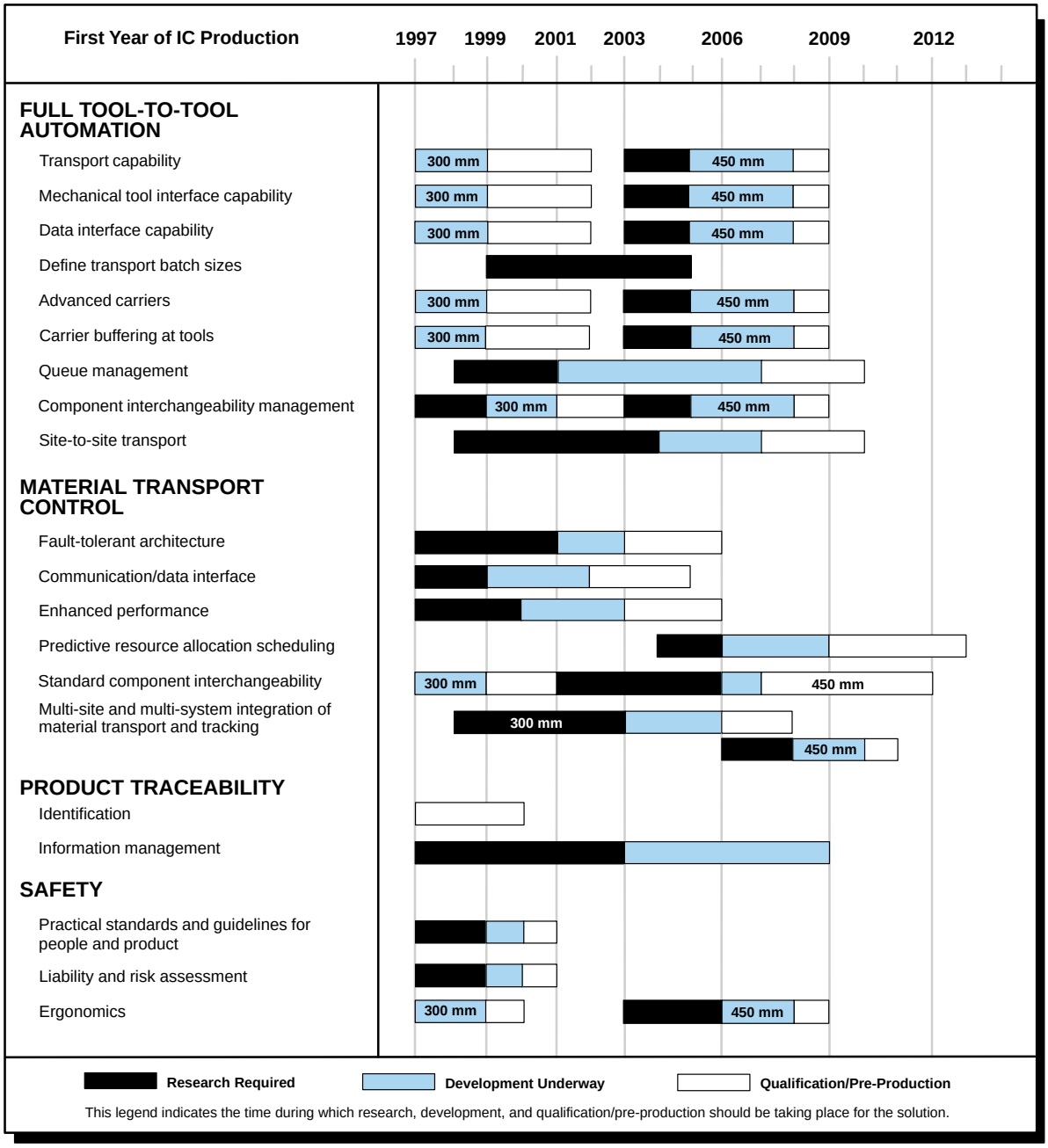


Figure 29 Product and Material Handling Potential Solutions

PROCESS AND EQUIPMENT CONTROL

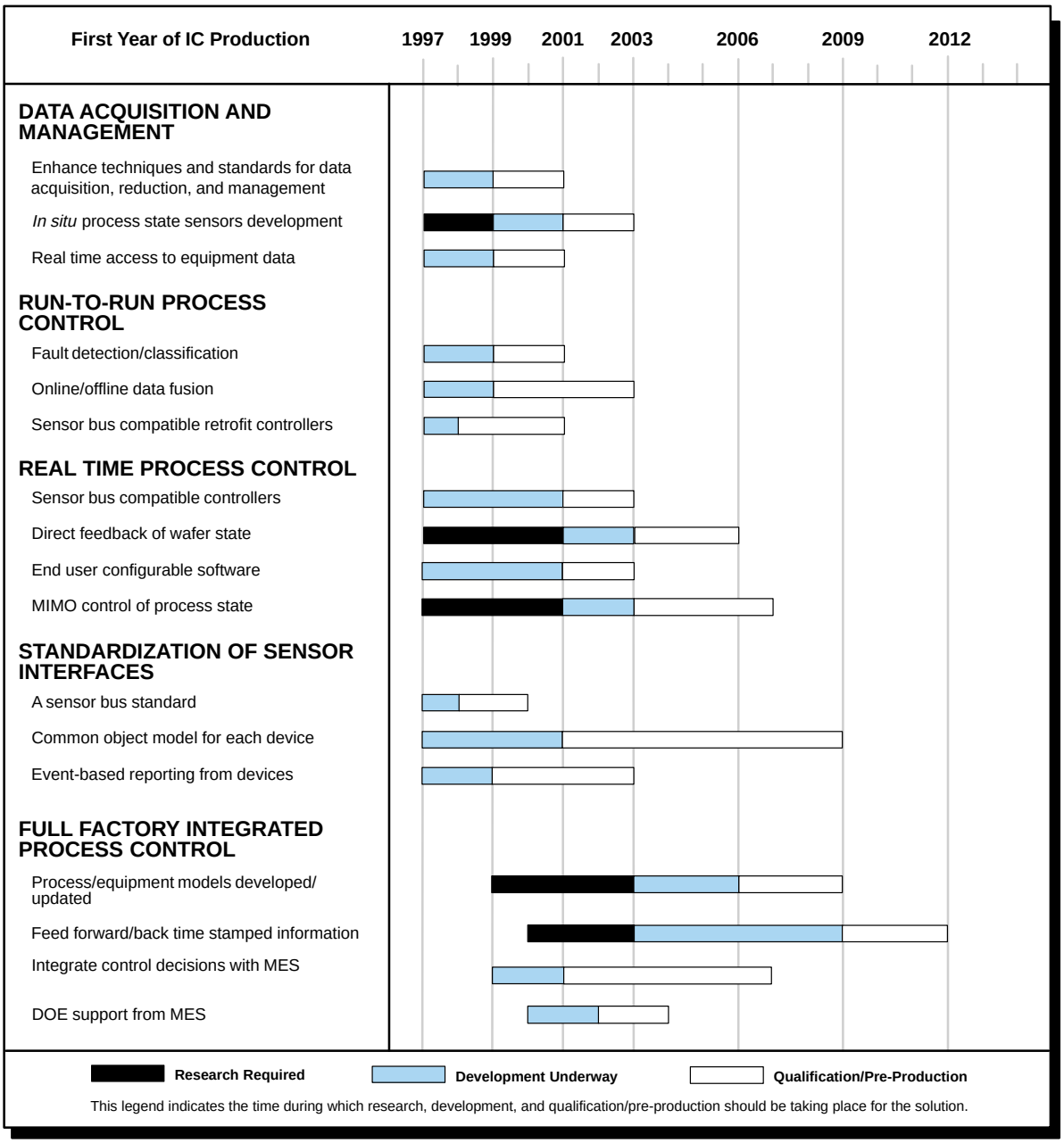
In situ process control is a critical solution for the future factory as conventional metrology becomes less reliable, expensive, and can only identify process excursions after significant yield loss. (Figure 30 presents the potential solutions set.)

Data must be readable on demand with several time scales from tens of milliseconds for critical endpoint signals to batch summaries for tracking tool drifts. This ability, with standardized format for data storage and reduction, provides a solution to the data overload problem that exists in the factory today. Model and data structures must be developed to deal with these large time differences as well as the unique challenge of integrating offline metrology with *in situ* data. An additional complexity is the extraction of data from cluster tools and linking that data to the correct chamber. In the immediate future retrofit controllers must handle this functionality for run-to-run control. Real time closed-loop control incorporating *in situ* sensors and model-based control algorithms within the advanced embedded controllers will allow deterministic processing so that product performance specifications (e.g., device speed or power) can be met.

The deployment of advanced process control requires a standardized sensor bus architecture for easy addition of sensors, bidirectional data, and information transfer protocols among the tool controller, sensors, computational algorithms, and the CIM system. A solution is being defined by the Semiconductor Equipment and Materials International (SEMI) Sensor Bus Subcommittee, object-based equipment model (SEMI standards), the National Institute of Standards and Technology/Advanced Micro Devices Advanced Process Control (APC) Framework Initiative,[12] and the SEMATECH CIM Framework.[13] Full factory integrated process control will build on elements developed for equipment information management, *in situ* metrology, closed-loop product control, and process/equipment models for model-based control that are fully integrated into an advanced process control framework. These models and connectivity embedded in the framework will also provide the basis for a virtual factory and the ability to simulate process capability for implementation in the real factory.

12. SEMATECH. *Advanced Process Control Framework Initiative (APCFI) 1.0*, 97063300A–ENG. Austin, TX:SEMATECH, June 28, 1997.

13. SEMATECH. *Computer Integrated Manufacturing (CIM) Framework Specification Version 1.5*, 93061697I–ENG. Austin, TX:SEMATECH, August 12, 1997.



MIMO—multi-input/multi-output
MES—manufacturing execution system
DOE—design of experiment

Figure 30 Process and Equipment Control Potential Solutions

HUMAN RESOURCES

Future semiconductor factories will be increasingly complex, and decisions made by managers and operators will have costly consequences. Effective management of highly complex factory systems will require a highly educated, well-trained workforce. Management of these integrated factory systems will be largely supported by sophisticated data collection and decision-support tools. Hence, information management will be a predominant element of the factory worker's job assignment. Decisions that are most effectively made by humans will be more clearly defined and supported by methods and decision support tools that improve the speed and accuracy of the human decision making process.

Human decision making capabilities require improvement in two ways—1) better education and training for the decision makers, and 2) better human/machine interfaces to improve presentation of data required to make rapid, accurate decisions. To improve education and training, a joint academia/government/industry effort to develop open-domain, easily implemented curricula for secondary, community college, and university education is needed. The curricula is required for engineers and all workers in the fabrication facility that make critical decisions, many of whom do not have four-year technical degrees. Development of an industry-wide method to share industry- or academe-developed learning materials, especially semiconductor manufacturing-specific curricula will facilitate continual improvement of the human decision making skills. Especially important will be the wider incorporation of industry-developed adult education in public and proprietary training programs.

Extensive research and development of improved methods to present large sets of highly interrelated data is needed to provide improvements in rapid human decision making. This effort must include fundamental studies of human assimilation of data and of machine data presentation methods. Methods must also be developed that use computers to improve the accuracy of human decisions. Examples of such methods are automated decision assistance and automated decision evaluation techniques.

Finally, the semiconductor industry must aggressively compete with other industries to attract and retain qualified, well-trained employees. This is especially true in the software and controls engineering fields, where shortages have become commonplace. As factory integration becomes better defined as a unified technology, technologists will emerge who have both breadth and depth in all of the factory integration technological elements. Retention and continued training of these individuals will be a key component in the success of future semiconductor factories. See Figure 31.

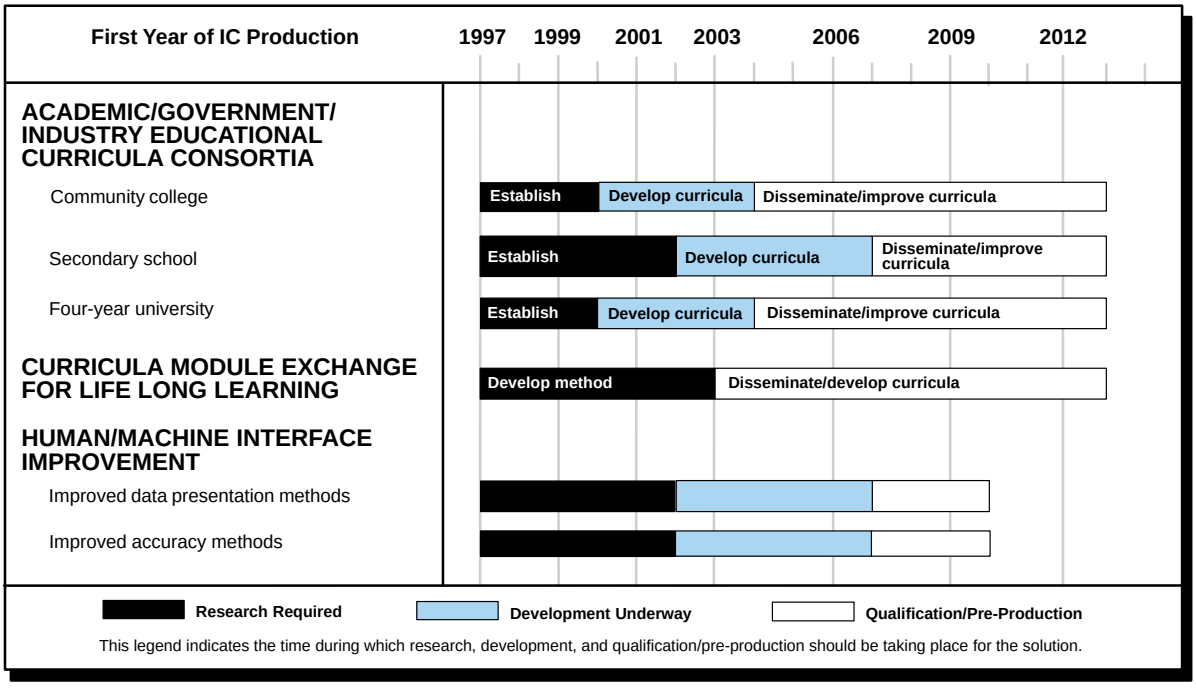


Figure 31 Human Resources Potential Solutions

SOFTWARE IMPROVEMENT

The industry needs significant OEE improvement to keep on its historic cost learning curve. This improvement cannot be realized without solving the software infrastructure problem. Current software development practice has led to significant reliability problems and late or unpredictable software delivery. Software is seen as the cause of 30% of the failures in new equipment.

Software is pervasive throughout the semiconductor industry. The amount of software embedded in a piece of semiconductor equipment is increasing by greater than 25% per year. Software is used in process and factory design, equipment and factory operation, and business planning and control. Yet software is the least perfected engineering discipline. Correcting an organization's deficient ability to produce high-quality software requires a fundamental and broad-based change in its engineering culture. Making such a change throughout an industry is a formidable task. The challenge is to orchestrate such a cultural change.

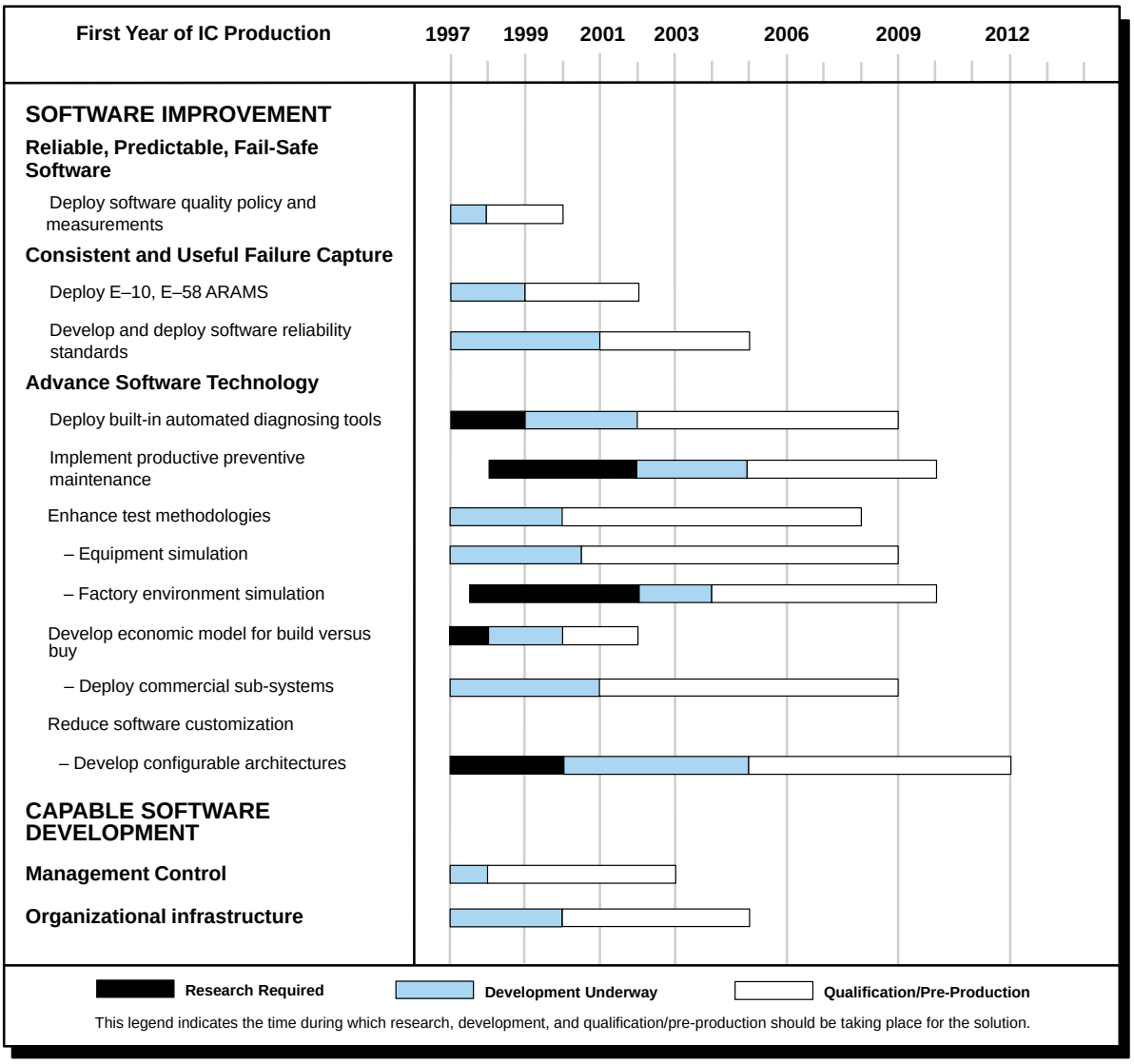
The semiconductor industry will accomplish reliability improvement through the capture of actual failure data[14] and deploying a software quality policy with measurement that drives equipment procurement.[15] As these actions drive software capability improvement, progress is measured using the Software Engineering Institute's Software Capability Maturity Model.[16] The expectation is that supplier software development will be operating at Level 2 on this scale by end of 1998, and at Level 3 by the year 2000.

There are several areas where the industry's application of software technology needs to advance to meet the OEE improvements. These include automated diagnosing of failures; implementing predictive maintenance tools to reduce down time; and improving test and simulation techniques to enhance verification. In addition, the industry demands custom software applications, but current software solutions are not able to support this need without significant development effort and risk. During this Roadmap's timeframe, system architectures must be developed and deployed that allow ease of customization. Refer to Figure 32.

14. SEMI. E10–96 Standard for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM). Mountain View, CA:SEMI.

15. SEMATECH. *Software Process Improvement (SPI) Guidelines for Improving Software: Release 5.0*, 96103188A–ENG. Austin, TX:SEMATECH, May 6, 1997.

16. Paulk, M.; Curtis, B.; Chrissis, M.; and Weaver, C. *Capability Maturity Model for Software, Version 1.1*, CMU/SEI–93–TR–024. Pittsburgh, PA:Software Engineering Institute, 1993.



ARAMS—automated reliability, availability, and maintainablity standard

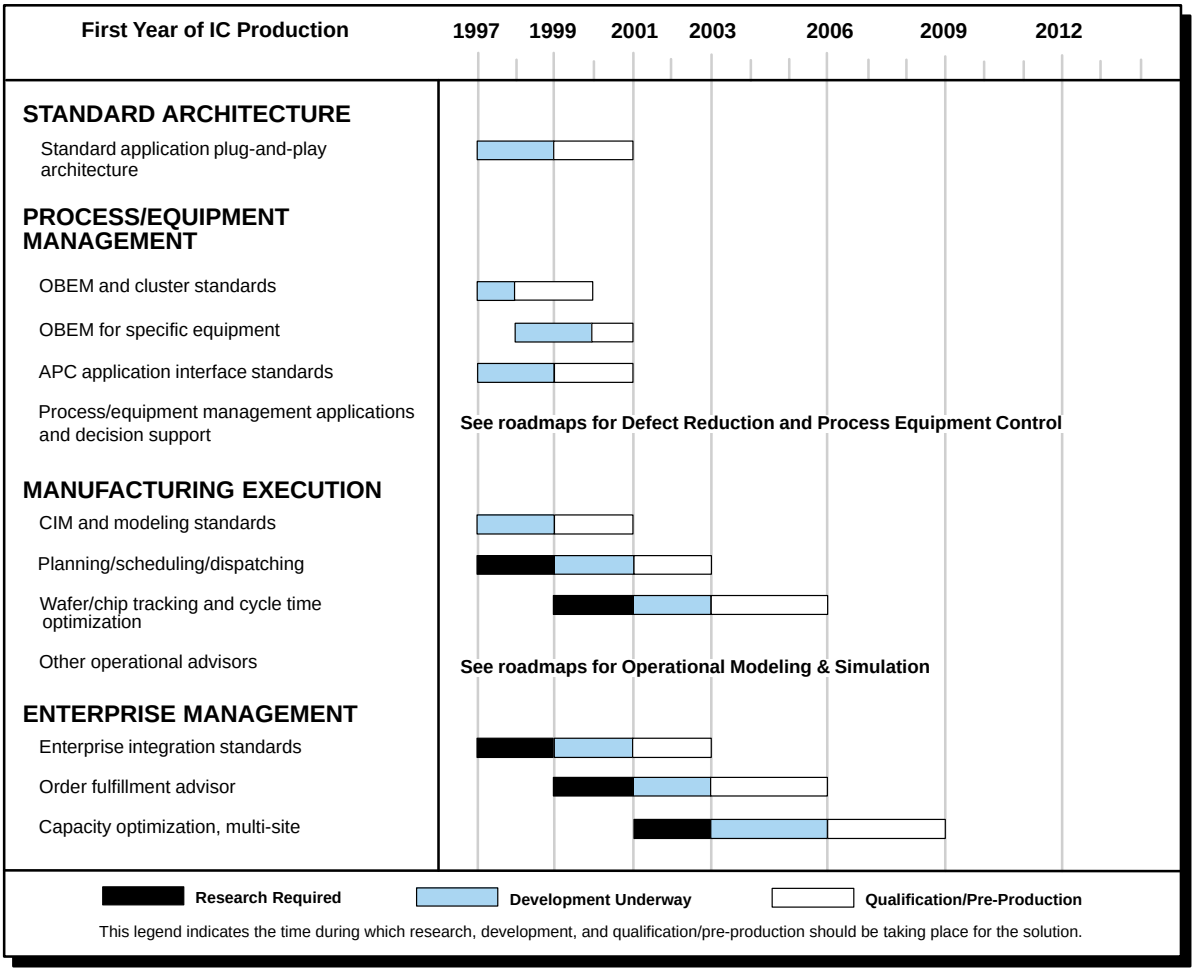
Figure 32 Software Improvement Potential Solutions

MANUFACTURING INFORMATION AND EXECUTION SYSTEM

A manufacturing information and execution system (MIES) delivers essential functionality to reduce factory operational cost, maximize product yield and factory effectiveness, and reduce system complexity. At the tool level, MIES services include data collection and reduction, recipe management, process modeling, advanced process control, fault detection, preventive maintenance, material handling, and experiment design support. At the manufacturing execution level, MIES services include material logistics, planning/scheduling/dispatching, lot/wafer/chip tracking, process history management, and factory modeling. At the enterprise level, MIES services integrate and organize information for customer order fulfillment, capacity modeling and planning, factory loading, and supply chain management.

Today, these MIES functions are fragmented and isolated, if they exist at all. The cost and time to deploy operational improvement applications and decision support systems is prohibitive. Those systems that are deployed often operate on redundant, incomplete, inconsistent information. Next-generation integrated MIES will be based on comprehensive, open, plug-and-play architecture and

data standards. These standards enable modular, partitioned systems to behave as a single integrated whole, and allow these systems to be quickly and cost-effectively developed and extended. An integrated architectural approach needs to be applied to all levels of factory information and execution systems and to modeling and simulation systems. Other system and software technology that will enable these functions and their integration include high reliability/availability systems, legacy evolution/migration, web-based computing, data visualization, active agents (e.g., data mining), and knowledge-based systems. With these technologies and sound engineering methodologies, factory systems can be built that proactively collect and analyze data, direct human and automated workflow, recommend operational decisions and automatically implement authorized decisions. See Figure 33.



OBEM—object-based equipment model

Figure 33 Manufacturing Information and Execution Systems Potential Solutions

MODELING AND SIMULATION

Modeling and simulation tools will continue to be used to contain increasing factory cost and risk, to speed yield ramps, and to improve operational effectiveness. Modeling will also assure that factories are appropriately sized in modular increments; process equipment is optimally utilized; and equipment, processes, and products are correctly designed and maintained at optimum performance. Additionally, as factories increase in size and complexity, model-based decision support tools are necessary to effectively manage highly complex processing tools as well as massive manufacturing facilities. These tools help clarify factory complexity and ensure that data is effectively used to make high quality decisions. Advanced modeling capabilities from the equipment level through the manufacturing execution level to the enterprise level will be crucial for maintaining the industry's overall productivity.

Advanced data management tools that automatically sense, collect, handle and transform data can reduce both data collection and conversion effort, and will increase model fidelity. Highly developed and widely deployed standards will be the critical foundation for these data management tools. Modeling and analysis tools that provide easier and faster model creation, calibration, validation, and update will make possible broader and more frequent application of models. Tools for creating models with computational efficiency are needed to allow use of models for real time decision support. Modular model design, modeling component reuse, and standard data management methods are key to improvements in model construction and function. As modeling modules become linked and integrated, accurate modeling of complex factory systems behaviors and phenomena such as new production line ramp-up and incremental capacity expansions will be possible. These models can provide solution information abstracted for use by all interested users, including operators, engineers, and operations managers. The target for these advanced, integrated modeling tools is to provide automated decision support for factory systems that benefit by closed-loop feedback control including the full range of activities from process tools control to high level enterprise management.

The solution areas outlined in Figure 34 pertain to both Factory Integration operational modeling and simulation, and the crosscut equipment, process, and product (TCAD and ECAD) modeling and simulation. The potential solutions outlined in this table result in an overall factory model that reflects current actual performance. While the two modeling areas are very similar in needs, they each have certain unique conditions and applications described below.

Advanced operational modeling and simulation tools will provide an integrated view of the factory including detailed design and management information about investment risk and capacity analysis for new factories, refurbished factories, and new product introduction. Such tools will also allow for the simulation of the total manufacturing enterprise at multiple levels of analytical abstraction. Advanced operational simulation/analysis tools will also be integrated with operational decision support tools, such as the manufacturing execution systems to provide model-based decision support. Such capabilities will allow improved factory operations management as well as improved enterprise management. One of the main enablers for such capabilities is a standard for the data employed by the models. This enabler will also provide for the linkage between operational models and equipment/process models, thereby resulting in inclusion of operational considerations in process design and use of current accurate process performance results in operational decisions.

Advanced equipment, process, and product modeling and simulation tools will provide an integrated view of predicted factory results, including process and product yields and equipment performance. This information will in turn be used for applications from real time equipment control to device design to achieve lower cost, higher throughput, faster ramping equipment, processes, and products. The enablers for effective applications include connecting the data to the appropriate models that creates requirements for chip, wafer, lot, and batch tracking from factory through assembly/test, whether it be production or special experimental runs, for the MIES. In addition, links in the various databases, from design to final test/probe, will be required to obtain needed information. The ability to link ECAD, TCAD, and equipment/process models with the data and database information will allow for a paradigm shift with respect to how inline specifications are made and yield ramp is achieved. For control applications, the ability to simplify models for real time use while also achieving predictability will be necessary. Empirical models, such as response surface as well as other functional representations, and phenomenological models need to be designed in the natural coordinates of the process/equipment to effectively capture the process and disturbance dynamics. The application of soft (virtual) sensors to replace off-tool metrology will be particularly attractive due to the benefits of decreased cycle time, increased throughput, and reduced factory costs. This application will drive the need for multivariate statistical methods and traditional control observability techniques. For details on fundamental model creation, see the *Modeling & Simulation TWG section* in this Roadmap document. The MIES system must be capable of carrying out the decisions as supplied by the equipment, process, and product modeling and simulation tools. Therefore, the MIES will accept feedback and feed-forward information and instructions from the modeling and simulation tools.

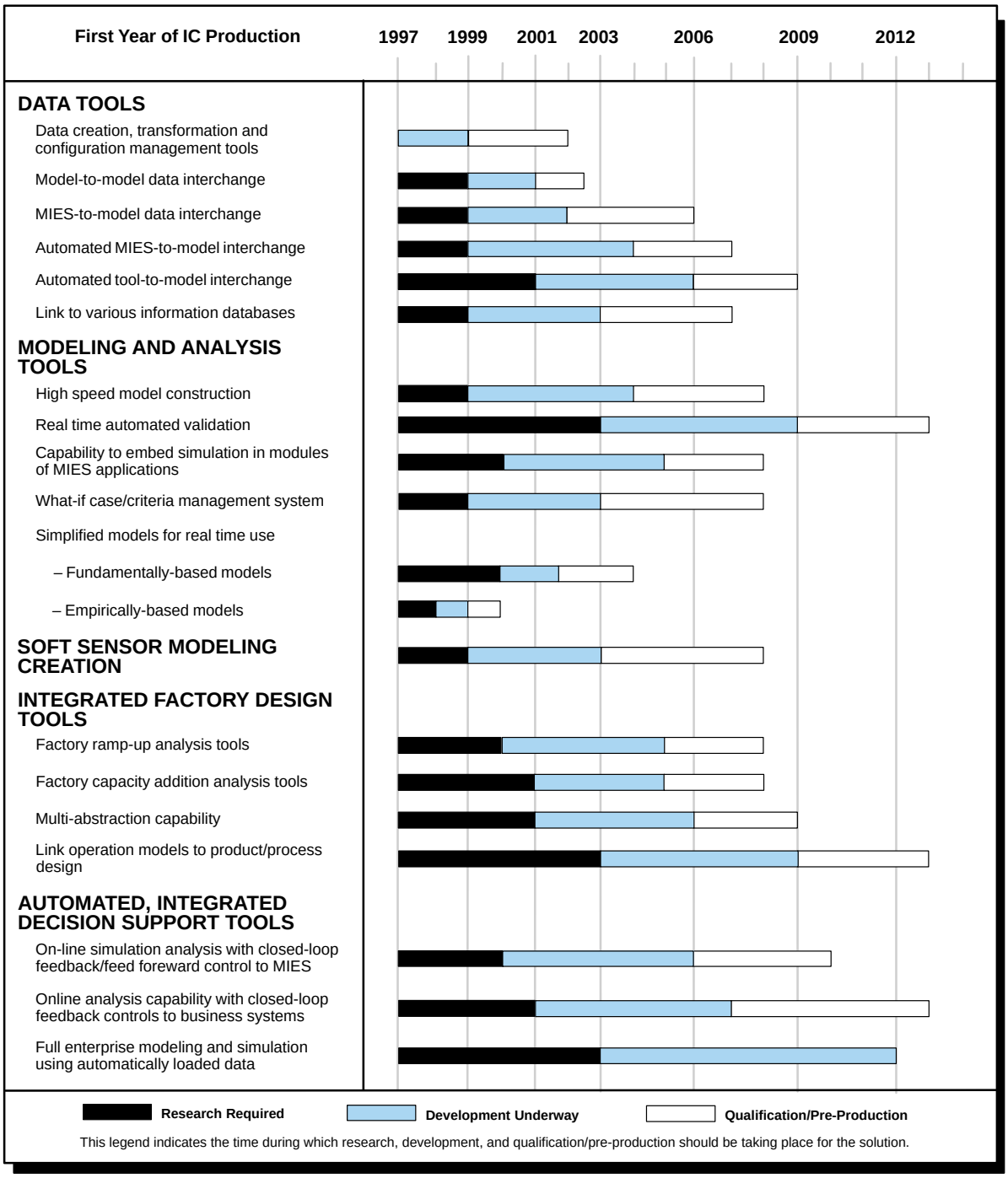


Figure 34 Modeling & Simulation Potential Solutions

CROSSCUT NEEDS

ENVIRONMENT, SAFETY, & HEALTH

Factory design defines the systems that deliver process materials to tools, manage by-products, and control work place environments. Future factory design must employ balanced programs of resource conservation, reduction, and management. These conservation and reduction programs are driven by increasing competition for limited water and energy resources, pollution concerns, and industry consumption. Table 40 presents the ESH issues.

While much of the responsibility for reduction in use of limited resources and waste minimization rests with the tool suppliers and process technologists, application of advanced resource management programs to factory systems will have a significant impact. The goal of these future programs is to build factories that minimize resource consumption and reuse, recycle, or reclaim by-products to produce near-zero effluent factories. Key factory-related ESH programs require water reuse in both process and nonprocess applications, energy efficient facilities equipment, improved facilities system design, and new facilities operating strategies.

The safety issues associated with factory processing support systems must also be aggressively improved in future factories. As more is known about potential impacts of the work environment on health and safety, worker protection improvements must be incorporated into factory systems. A thorough understanding of the potential safety risks associated with automated equipment will drive development of standards that assure safe working conditions for both people and product. Additionally, product and workplace contamination resulting from chemicals exposure must focus attention on technologies that completely isolate personnel from equipment and product, as well as advanced environmental monitoring and tool maintenance procedures.

As factories increase in size the industry faces increasing permit, code, and emissions limitations. Since changes in government regulations and codes can take as long as three years to implement, coordinated effort is needed to drive code and regulatory changes that reflect advancements in the technology of tools and factories.

Table 40 Factory Integration ESH Crosscut Issues

KEY ISSUES		POTENTIAL SOLUTIONS
Natural Resources	Water use reduction (30 to 4 gal/in^2 by 2012)	Conserve and reuse water Reduce net demand for incoming water Reclaim and recycle water at factory level Optimize process water use at tool level
	Power/energy use reduction (9 to 4 kWh/in^2 by 2012)	Design energy efficient tools and factories Increase HVAC* efficiency Reduce exhaust and makeup air requirements Reduce volume of environmentally controlled space Increase use of mini-environments Optimize energy use by tools
Chemical Management	Factory effluent/emissions reduction	Cost-effective point-of-use abatement Increase exhaust and scrubber efficiency Improve chemical and by-product reuse Investigate “clean and green” alternative chemicals Optimize process chemical use at tool level
Worker Protection	Product and workplace contamination Chemical exposure Equipment safety and ergonomics	Separate chemicals from general work area Improve monitors and sensors Improve maintenance procedures Isolate tools from operators and work environment Use mini-environments to control process critical areas Reduce noise levels from tools and air flows Develop AMHS system safety requirements
Regulatory and Risk Management	Permitting and zoning requirements Building, electrical, and fire code restrictions Regulatory emissions limits Insurability/asset loss containment	Develop modular fab designs complying with regulations Identify regulatory changes required for future factories Consolidate and simplify regulations and codes Design smaller modular factories

** HVAC—heating ventilation and air conditioning*

DEFECT REDUCTION

The goal for a new factory is to rapidly ramp yield to the highest possible level. Consequently, the development of sound defect reduction strategies plays a pivotal role in meeting the factory integration need to reduce costs and investment risks. Since yield loss results from excursions from the ideal process, the need is to understand and model how to prevent excursions and to identify the process parameters that must be controlled to achieve high yield. The factory defect reduction yield model should define typical operational performance and permit a Pareto of performance detractors that lead to defects and yield loss. A factory model based on experimental mapping of process parameter space will guide sensor integration, advanced process control strategies, and reduce the need for separate metrology tools and monitor wafers. The most critical needs are determining the variation tolerance of critical process parameters and the interaction between processes that could lead to better automated process control and reduced reliance on end-of-line inspection. Data on the threshold at which impurities in critical process fluids impact process (e.g., etch rate, film uniformity) and device performance (e.g., threshold voltage, gate oxide integrity) can be used to guide *in situ* sensor development and help reduce the time to high yield by eliminating the source of defects in advance. Refer to Table 41.

Many of the inputs needed for defect reduction during yield ramp are necessary for a factory model that comprehends the most efficient factory design for rapid construction, rapid yield ramp, efficient equipment utilization, and extendability to future generations of technology and products. For example, the defect targets allocated to each process can be used to guide process development at equipment suppliers and can be used in the development of factory models that permit a comparison of process interactions and tradeoffs between yield ramp, factory cost, and complexity.

Table 41 Defect Reduction

KEY ISSUES	POTENTIAL SOLUTIONS
Variation Tolerance of Critical Process Parameters	
Process control enablers and extendability Root cause analysis of performance detractors	Experimental mapping of the parameter space for each process and correlcation to device performance
Process Interactions	
Wafer state analysis Initial equipment state consistency Impact of contamination on OEE	Short loop modeling and experimental mapping of parameter state variations Component wear and lifetime studies
Process Critical Fluids and Materials Purity Requirements	
POU contamination monitoring Materials reliability and consistency	Industry test structure for each node on roadmap Process parameter studies
Reduce End Of Line Inspection And Monitor Wafers	
Nonvisual defect detection Metrology for <.08 μm defects	Inline inspection tools *In situ* sensors for advanced process control
Rapid Yield Ramp	
Process specific yield models Process control	Inline inspection metrology Correlation of parameter space variation and defects
Factory Performance Metrics to Prevent Defects	
Electromagnetic interference Vibration Molecular contamination	Short loop models Data/metrics standards

METROLOGY

Process equipment monitoring and control using sensor-driven, model-based integrated manufacturing (SDMBIM) are critical to increasing operational efficiency and decreasing the wafer cost in future semiconductor factories. This will lead to the development of enhanced sensors and improved decision support tools through cooperative efforts in the following areas:

- Robust, intelligent sensors complete with calibration and diagnostics capability that are compliant with sensor bus standards and the necessary algorithms for turning raw data into actionable information
- Process tools that are sensor bus compliant and that utilize both wafer-level information and time-series sensor data provided by internal sensors/actuators and/or external sensors
- Factory-wide implementations of sensor-driven, model-based manufacturing systems based upon integrated sensors and sensor buses (such systems will be first utilized in unit process control, and then migrated to factory-level optimization and control)
- Enhanced manufacturing information and execution systems (MIES) that support data acquisition and bi-directional data and information transfer protocols among the tools, the appropriate sensors, the computational algorithms, and the decision-making components

Adoption of standard communication protocols will enable the integration of new sensors into process tools. Approved sensor bus standards (through SEMI) are being used by some, but not all process tool and sensor suppliers. Widespread implementation of these standards by the semiconductor industry will reduce both the time and cost of integration. Adherence to these standards will also facilitate the integration of new sensors by semiconductor manufacturers even after process tools have been purchased and installed. Two important technological issues in support of advanced metrology systems will continue to be researched—1) communications bus bandwidth, and 2) communications bus speed. A fully capable metrology data communication bus will simultaneously transmit very large data volumes from multiple sensors, and transmit that data fast enough for time-critical sensors to provide real time process control.

A CIM architecture will provide the necessary data transfer, control strategy, model links, and communication capabilities. Through this CIM architecture, factory wide feed-forward and feedback information will be provided using advanced sensors incorporated into the process tools. The SDMBIM will provide the capability for the following:

- Fault detection, classification, and interdiction to detect and analyze faults for enhanced yield and faster tool repair, thereby eliminating the continued misprocessing of wafers
- Fault prognosis capability to convert from scheduled maintenance to preventive maintenance, which will reduce future misprocessing and generate higher equipment availability
- Model-based process control to increase yield by keeping process on target and reducing test wafer usage

These features will provide enhanced equipment and process reliability and control, which will directly translate into increased product control, reliability, and yield.

MODELLING & SIMULATION

This section has been combined with the *Factory Integration Modeling and Simulation* section.

ASSEMBLY & PACKAGING

SCOPE

Assembly & Packaging is the bridge between silicon and the electronics system. Package design and fabrication is increasingly important to system applications. Consideration of factors affecting waveform integrity for both power and signal (i.e., timing, crosstalk, and ground bounce) will affect device layout on the chip, chip layout on the package, and interconnect. Packaging capabilities that are as advanced as those used in IC design and fabrication must become available in packaging to provide the cost-performance advances needed. This Assembly & Packaging roadmap addresses proposed activities needed to develop materials, processes, and designs. If successfully implemented, it will contribute to the increased competitiveness of packaged electronic products consistent with the goals of the National Roadmap.

The scope of the Assembly & Packaging roadmap includes the following:

- Multi-Chip Packaging (MCP)
- Single Chip Packages (SCP)
- Bonding/Chip/Package/Substrate Design
- Packaging Substrates
- Flip Chip Interconnect (Direct Chip Attach [DCA])
- Assembly
- Thermal/Power/Ground Management
- Electrical/Performance Characterization

Burn-in and known good die (KGD) testing are needs that are important to Assembly, Packaging and Test but are not addressed in detail in this roadmap. Crosscut technology requirements are highlighted in this roadmap for the following categories: ESH, Metrology, and Modeling & Simulation.

Many of the Assembly & Packaging roadmap attributes are driven by the electronics products and board/substrate industries, and many of the challenges have system solutions. As a result, the solutions to certain packaging challenges are outside of the scope of this roadmap. However, to ensure that the needs of the semiconductor community are met and to better understand system needs, the Assembly & Packaging Technical Working Group (TWG) has taken the following proactive measures:

- The membership of the TWG has been expanded to include representatives from electronic systems and board/substrate industries.
- Partnerships have been formed with organizations developing roadmaps for systems with the National Electronics Manufacturers Initiative (NEMI) and board/substrate industries with The Institute for Interconnecting and Packaging Electronic Circuits (IIPC) and the span of these respective roadmaps has been identified.
- Cross-validation of the systems, board/substrate, and packaging roadmaps has been conducted.

Assembly and packaging technology is driven more by market application requirements than by chip technology used for the integrated circuit. The following market applications categorize the information in this roadmap:

- Commodity—<$300 consumer products, microcontrollers, disk drives, displays
- Hand-held—<$1000 battery-powered products; mobile products, hand-held cellular telecommunications, other hand-held products
- Cost-performance—<$3000 notebooks, desktop personal computers, telecommunications
- High-performance—$3000 high-end workstations, servers, avionics, supercomputers, most demanding requirements
- Automotive—under-the-hood and other hostile environments
- Memory—DRAMs, SRAMs

These application areas encompass the majority of the product stream of the semiconductor industry. The technology addressed in the Roadmap provides at least 80% of the revenue in each application area (i.e., the revenue center of gravity) with the exception of high-performance.

DIFFICULT CHALLENGES

The most difficult challenges facing the assembly and packaging industry are presented in Table 42. These challenges are intended to provide a mechanism to allow the research community to focus resources in the areas of greatest need.

Table 42 Assembly & Packaging Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Improved organic substrates for high I/O area array flip chip	T_g compatible with eutectic solder processing ε_r approaching 2.0 Increased wireability at lower cost Lower CTE* approaching 6.0 ppm / °C Lower moisture absorption
Improved underfills for high I/O area array flip chip	Improved manufacturability (fast dispense/cure), better interface adhesion, lower moisture absorption, flow for dense bump pitch Reliability above 150°C for automotive
Reliability limits of flip chip on organic substrates	Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump**)
Integrated design tools and simulators to address chip, package, and substrate complexity	Thermal/thermo-mechanical Electrical (power disturbs, EMI†, signal integrity associated w/higher frequency/current, lower voltage) Commercial EDA‡ supplier support
DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Close the gap between the substrate technology and the chip	ε_r approaching 1.0 CTE of 3.0 ppm / °C Cost/unit area constant (cost/layer decreasing) Interconnect density scaled to silicon
"System level" view of integrated chip, package, and substrate needs	Commercial EDA supplier support

* *CTE—coefficient of thermal expansion*
** *UBM—under bump metallurgy*
† *EMI—electric magnetic interference*
‡ *EDA—electronic design automation*

TECHNOLOGY REQUIREMENTS

Packaging technology continues to change rapidly. Assembly and packaging needs are driven as much by market application requirements as by silicon technology. Cost will drive technology tradeoffs for all market segments. The key technology requirements have been updated by the TWG as shown in Table 43. Although assembly and packaging costs are expected to decrease over time on a cost per pin basis, the chip and package pin count is increasing more rapidly than cost per pin is decreasing. This explosion in pin count is increasing not only the absolute cost of assembly and packaging on a per chip basis, but also the substrate and system-level costs. To satisfy the requirements for the increasing numbers of pins needed to leverage silicon productivity more fully, the industry must implement affordable new assembly and packaging technologies independent of pin count.

Table 43 Assembly & Packaging Technology Requirements

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*	*2006* / *100 nm*	*2009* / *70 nm*	*2012* / *50 nm*
Cost (Cents/Pin) (A)							
Commodity	0.60–0.80	0.54–0.72	0.49–0.65	0.44–0.59	0.38–0.51	0.33–0.43	0.28–0.37
Hand-held	0.70–1.40	0.63–1.26	0.57–1.14	0.52–1.03	0.44–0.89	0.38–0.76	0.33–0.65
Cost-performance	1.40–2.80	1.27–2.52	1.14–2.28	1.03–2.06	0.89–1.77	0.76–1.52	0.65–1.30
High-performance	5.00	4.52	4.09	3.68	3.16	2.71	2.33
Automotive	0.66–0.88	0.59–0.79	0.54–0.72	0.49–0.65	0.42–0.56	0.36–0.48	0.31–0.41
Memory	0.50–1.20	0.45–1.08	0.41–0.97	0.39–0.88	0.35–0.76	0.32–0.65	0.29–0.56
Power: Single-Chip Package (Watts) (B)							
Commodity	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Hand-held	1.2	1.4	1.7	2	2.4	2.8	3.2
Cost-performance	28	48	61	75	96	104	109
High-performance	70	88	108	129	160	170	174
Automotive	12	14	14	14	14	14	14
Memory	0.5	0.8	1.1	1.5	2	2.5	3
Chip Size (mm^2) (C)							
Commodity	50	53	56	59	65	70	77
Hand-held	50	53	56	59	65	70	77
Cost-performance	300	340	385	430	520	620	750
High-performance	300	340	385	430	520	620	750
Automotive	50	53	56	59	65	70	77
Memory	280	400	445	560	790	1120	1580
I/O Bus Widths (Bits)							
Commodity	32	32	64	64	128	128	256
Hand-held	32	64	64	128	128	256	256
Cost-performance	64	64	128	128	128	256	256
High-performance	128	128	256	256	256	512	512
Automotive	16	32	32	32	64	64	128
Memory	16	32	32	32	64	64	64
Performance: On-Chip (MHz) (D)							
Commodity	200	300	415	530	633	840	1044
Hand-held	200	300	415	530	633	840	1044
Cost-performance	350	526	727	928	1108	1468	1827
High-performance	600	958	1570	1768	2075	2574	3081
Automotive	132	150	150	200	200	250	250
Memory (D/SRAM)	75/175	100/263	100/362	125/464	125/554	150/734	150/913
Performance: Chip-to-Board for Peripheral Buses (MHz)							
Commodity	66	75	75	100	100	125	125
Hand-held	66	75	75	100	100	125	125
Cost-performance (E)	75/175	100/263	100/362	125/464	125/554	150/734	150/913
High-performance (F)	250	479	785	884	1037	1287	1540
Automotive	66	75	75	100	100	125	125
Memory (D/SRAM) (E)	75/175	100/263	100/362	125/464	125/554	150/734	150/913

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Table 43 Assembly & Packaging Technology Requirements (continued)

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Core Voltage (Volts)							
Commodity	2.5	1.8	1.8	1.5	1.2	0.9	0.6–0.9
Hand-held	1.8–2.5	1.5–1.8	1.2–1.5	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6
Cost-performance	2.5	1.8	1.8	1.5	1.2	0.9	0.6–0.9
High-performance	2.5	1.8	1.8	1.5	1.2	0.9	0.6–0.9
Automotive	5.0	3.3	3.3	2.5	2.5	2.5	2.5
Memory	2.5	1.8	1.8	1.5	1.2	0.9	0.6–0.9
Junction Temperature Maximum (°C) (G)							
Commodity	125	125	125	125	125	125	125
Hand-held	115	115	115	115	115	115	115
Cost-performance	100	100	100	100	100	100	100
High-performance	100	100	100	100	100	100	100
Automotive	150	175	175	180	180	180	180
Memory	100	100	100	100	100	100	100
Operating Temperature Maximum: Ambient (°C) (G)							
Commodity	55	55	55	55	55	55	55
Hand-held	55	55	55	55	55	55	55
Cost-performance	45	45	45	45	45	45	45
High-performance	45	45	45	45	45	45	45
Automotive	140	165	165	170	170	170	170
Memory	45	45	45	45	45	45	45
Package Pin Count (H)							
Commodity	40–208	40–236	40–277	40–325	40–413	40–524	40–666
Hand-held	100–256	117–300	137–352	161–413	205–524	260–666	330–846
Cost-performance	256–600	300–732	352–895	413–1093	524–1476	666–1992	846–2690
High-performance	1089	1493	1824	2228	3008	4060	5480
Automotive	40–208	40–236	40–277	40–325	40–413	40–524	40–666
Memory	28–70	30–82	34–96	36–113	40–143	44–182	48–231
Chip Pad Count (Chip-to-Package) (H)							
Commodity	40–208	40–236	40–277	40–325	40–413	40–524	40–666
Hand-held	100–295	117–400	137–469	161–551	205–699	260–888	330–1128
Cost-performance	256–800	300–976	352–1193	413–1458	524–1968	666–2656	846–3587
High-performance	1452	1991	2432	2970	4010	5412	7308
Automotive	40–208	40–236	40–277	40–325	40–413	40–524	40–666
Memory	28–70	30–82	34–96	36–113	40–143	44–182	48–231
Package Thickness (mm)							
Commodity	1.0	1.0	0.8	0.65	0.5	0.5	0.5
Hand-held	1.0	0.8	0.65	0.5	0.5	0.5	0.5
Cost-performance	2.0	1.5	1.5	1.2	1.2	1.0	1.0
High-performance	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Automotive	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Memory	0.8	0.5	0.5	0.5	0.5	0.5	0.5

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Table 43 Assembly & Packaging Technology Requirements (continued)

A. All costs do not include silicon, heat sinks, or test; substrate cost should not exceed 50–70% of total cost

B. Solutions are being pursued for cost-performance ≥ 50 W and for high-performance ≥ 120 W due to cost-driven thermal management issues. Cost-performance data is for desktop applications; notebook applications are limited to 6 W maximum in 1997.

C. Significant technology issue from Si/package or substrate CTE mismatch for cost-performance and memory; significant cost issue for high-performance

D. > 400 MHz reflects need for improved impedance control

E. xx/yyy refers to system memory and peripheral bus speed (xx) and to processor cache memory data transfer bandwidth (yyy) for high end of cost-performance category. Memory performance must match the requirements of processor buses and may require new architectures at the device or array level, such as reduced-width multiplexed buses that run at the on-chip frequency.

F. > 1000 MHz reflects need for improved impedance control

G. Uncertain materials solutions

H. Reflects package/substrate cost issues

PACKAGE DESIGN REQUIREMENTS

Package design complexity (chip-to-module and chip/module-to-board) and scope are continuously increasing while the market intensifies the demand for design cycle reduction and high design confidence. Physical, electrical, thermal, mechanical, assembly and manufacturability considerations, in addition to cost and availability, confront the package designer. The package design process requires continuous improvements in design and analysis tools. The tools for layout, wiring, electrical, mechanical, and thermal design tasks must enhance usability and minimize interface incompatibilities if design cycle reductions are to be realized. The goal is an integrated design system within the next decade.

PACKAGE RELIABILITY REQUIREMENTS

As the complexity of package technology continues to increase, new materials will be needed to meet design and performance challenges. There is a critical need to understand the fundamental physical and chemical properties of these materials, as well as their ability to form reliable interfaces with other package materials. A critical need also exists to understand fundamental failure mechanisms. Interfacial delamination will continue to be a critical reliability issue.

POTENTIAL SOLUTIONS

INTEGRATED DESIGN ENVIRONMENT

Figure 35 shows potential solutions for an integrated design environment. Many of these solutions involve modeling and simulation capabilities that will be embodied in packaging computer aided design (CAD) systems. Design tools are required to manage the complexity of packaging that is being pushed to its performance limits. In the short term a major focus of these tools will involve flip chip/area array substrates. In the long term an integrated design system with expert capabilities is the solution. The time required for these features to migrate from concept to commercially viable tools must be shortened significantly. This acceleration of the tool development cycle will require close partnerships between the universities and the electronic design automation (EDA) suppliers. The long range implementation of the integrated design environment will drive the packaging tools into the chip design solutions.

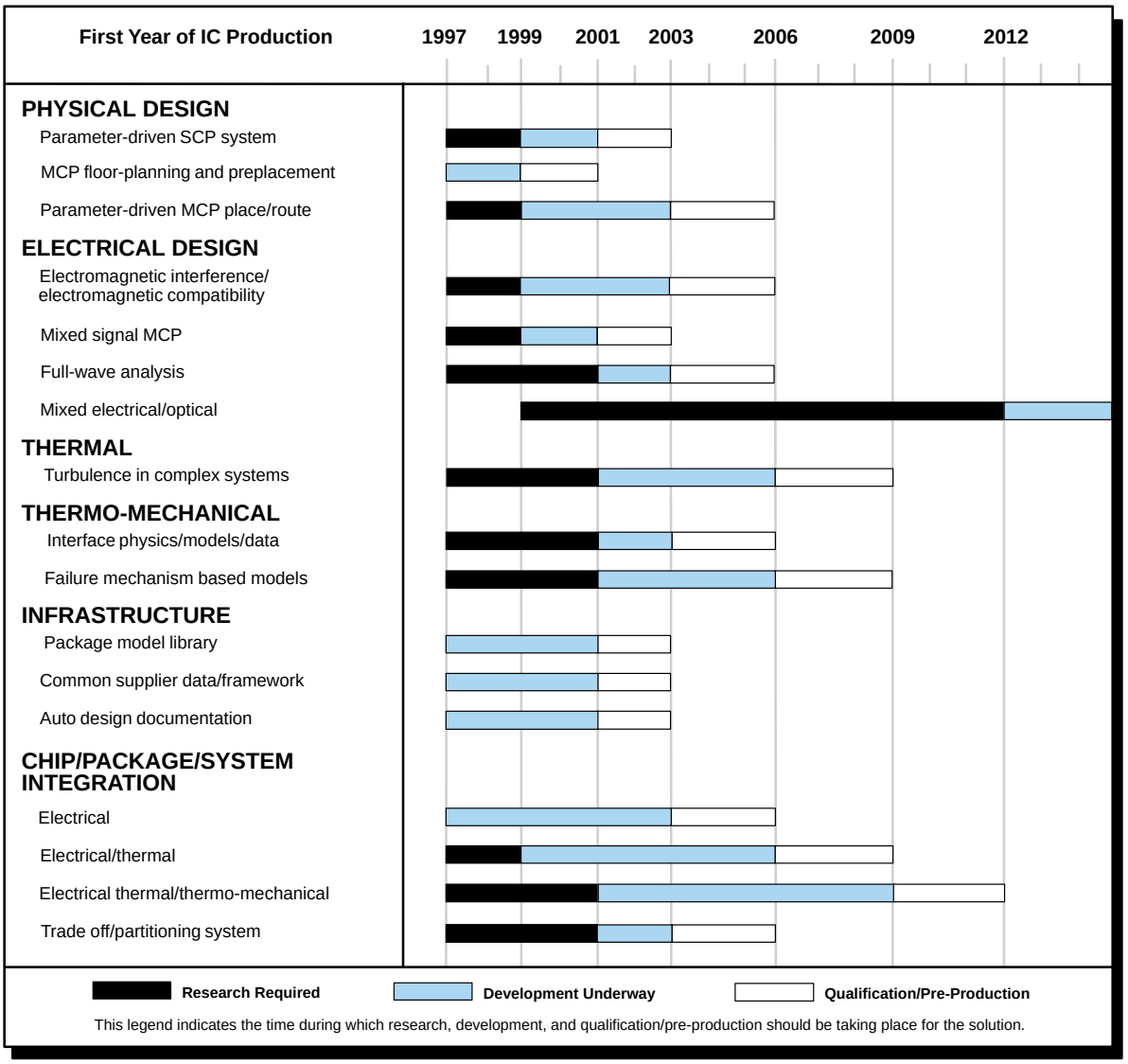


Figure 35 Integrated Design Environment Potential Solutions

THERMAL MANAGEMENT

The task of dissipating the heat from integrated circuit chips while maintaining acceptable junction temperature is a significant challenge for semiconductor and systems manufacturers. Power and wattage requirements by market segment are shown in Table 43.

The hand-held market segment power availability is limited by battery power, and power dissipation is limited by the user (the heat sink is the hand). The cooling is usually accomplished without using forced air. The challenge for heat dissipation will be in efficient, uniform reduction of internal thermal resistance from the chip to the surface of the hand-held product. The development of higher thermal conductivity materials and innovations and advancements in heat pipes could be needed beyond 2.5 Watts per chip.

Desktop processors for the cost-performance market requires forced air cooling for the system and represents a wide spectrum of electronic products. With area array flip chip the backside of the chip provides a direct efficient heat path from the chip to the heat sink for forced air cooling. Existing technology solutions in cooling and heat sink design could become insufficient beyond 50 Watts per chip in applications where air cooling capabilities are limited, such as acoustic noise limits. Significant

development and innovations will be needed for many applications in this market (e.g., telecommunications and notebook computers) including reduction of internal thermal resistance, more advanced/efficient air cooling, engineered surfaces, and boundary layer control.

The high-performance market sector has experienced an exploding increase in power over the different generations. Air cooling is still the only option to keep cost within bounds. With chip power at 60–70 Watts, internal hot spots are of concern. Significant engineering development will be needed for power increases at each technology generation. It is expected that at approximately 110–120 Watts per chip, the heat sink sizes will become intolerable, and major alternate innovations and solutions will be needed. Capabilities equivalent to closed-loop cooled systems, which are acceptable to the end use customers, will be needed.

WAFER BUMPING

Wafer bumping is a key element to the successful implementation of flip chip technology as required by the Roadmap. Eutectic Sn/Pb bumps on organic substrates represent the target against which potential solutions should be benchmarked. There are several challenge areas to implementation and proliferation including: cost, density, manufacturability, availability, and compatibility with on-chip Cu/low κ materials. Potential solutions to reduce soft error upset from alpha particle emmissions could include moving to low alpha Pb and Pb-free solders during the timeframe of this roadmap. Cost for bumping a wafer (on a per chip basis, including the under bump metallurgy and the bump deposition) needs to decrease continuously over the period through process simplification. Any lower cost process must preserve reliability, quality, and yield. Bump pitch will decrease from 250 μm or greater today, to 50 μm by the end of the period, increasing the wireability requirements for the substrate significantly. Bumped wafers and chips must become generally available at a cost below packaged devices but at an equal quality level.

Test has the greatest technical challenge to achieve the quality goal. Test contactor reliability must be achieved at elevated temperatures without inducing bump damage. The flip chip must be, and be perceived to be, equivalent to a packaged device. Achieving this perceived equivalence is the greatest short term challenge and needs greater industry focus for success.

CHIP-TO-NEXT LEVEL INTERCONNECT

Table 44 and Figure 36 show the chip-to-next level interconnect needs and potential solutions. The values for wire bond in this table are for inline pad pitches, although a staggered bond pad configuration could achieve an effective pitch denser than the value shown. The flip chip connection requires fan-out wiring on the package. Signal leads are usually placed on the outer several rows together with many of the voltage and ground leads for easy fan-out and minimum package inductance. The inner regions of the area array may be used for voltage and ground connection to minimize the on-chip resistive voltage drop across the IC chip. The flip chip interconnect technology must provide for 200 mA/connection while maintaining a low voltage drop.

Table 44 Chip-to-Next Level Interconnect Needs

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Chip Interconnect Pitch (μm)							
Wire bond—ball	**70**	**50**	**50**	**50**	**50**	**50**	**50**
Wire bond—wedge	**60**	**45**	**45**	**45**	**45**	**45**	**45**
TAB*	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Flip chip (area array)	**250**	**180**	**150**	**130**	**100**	**70**	**50**

* *TAB—tape automated bonding*

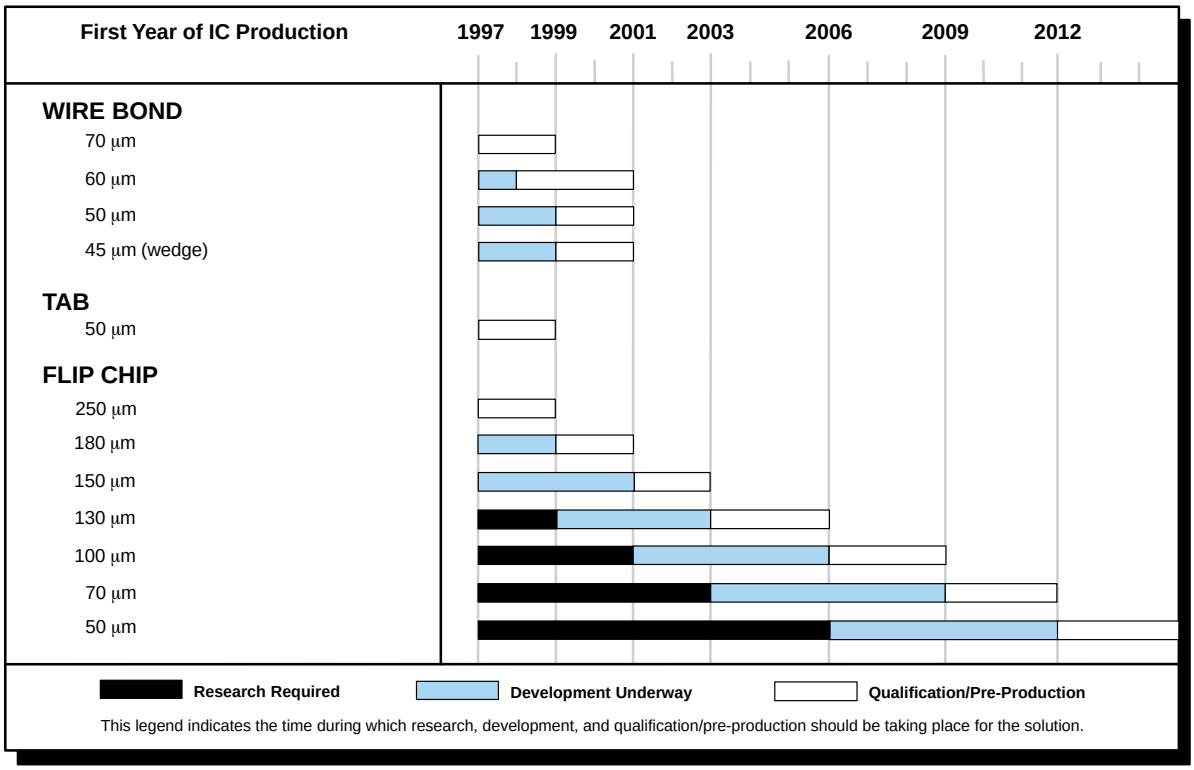


Figure 36 Chip-to-Next Level Interconnect Potential Solutions

To satisfy the high pin count and performance requirements in the 1997 Roadmap, flip chip will become the predominant technology for chip-to-next level interconnect. Wire bond technology will continue to evolve and will be the dominant interconnect for commodity products until flip chip costs become favorable. Size, weight, and performance driven products will need flip chip interconnect with area array I/O at a pitch of 250 μm or less. This interconnect approach will require compatible underfill and substrate technologies to be available at the necessary performance and cost. A level of interconnect can be eliminated with this technology. Material, process development, and metrology technology improvements will also be required to support flip chip implementation. Flip chip interconnect technology at area array pitches ≤ 250 μm will put extreme pressure on substrate density for I/O escape beneath the chip site. Substrate redesign is usually necessary to accommodate flip chip interconnect chip shrinks.

ENCAPSULATION AND UNDERFILL

To achieve rugged, low-cost packaging and meet electrical and thermal requirements, quad flat packages (QFP) and ball grid array (BGA) packages will need lower cost, low-stress, low-viscosity, high T_g mold compounds. To address the CTE mismatches between the chip and substrate, flip chip interconnect on organic substrates will require underfills that exhibit improved reliability, manufacturability (faster dispense/cure), better interface adhesion, and lower moisture absorption. Underfill solutions must be compatible with standard surface mount processes and equipment without increasing cycle time.

SINGLE-CHIP PACKAGES (SCPS)

QUAD FLAT PACKAGES (QFPS)

QFPs offer solutions for lower pin count, surface mount applications. QFP lead pitches are expected to level off at 0.5 mm due to the increased complexity of the surface mount technology (SMT) component assembly process below 0.5 mm. QFP pin count will be limited to 304 leads as body sizes approach 40 mm. Although QFP usage below 0.5 mm will certainly occur, it will likely be limited to lower pin counts (≤ 208 leads), smaller body sizes (≤ 28 mm), and selective applications.

BALL GRID ARRAY (BGA) PACKAGES

For many applications in the 200+ pin count range, BGA packages will provide potential solutions. Many BGAs will utilize a wire bond interconnect on the periphery of the ICs. Area array flip chip connections to BGAs will be needed for high I/O or high power chips. Plastic ball grid arrays (PBGAs) will require the use of liquid encapsulants as underfills to reduce the shear stress load on the flip chip interconnections, due to the large difference in the CTE between the silicon IC and the organic substrate. The bending of the encapsulated flip chip on PBGAs may become excessive for large chip sizes and could impact the thermal cooling path. Due to board assembly yield considerations, QFPs with body sizes beyond 28 mm could also migrate to PBGA, provided that the cost of the PBGA can approach that of the QFP. The space transformation between the tight pad pitch on the IC chip and the relatively large pitch between the plated through hole (PTH) on the substrate is totally contained in the PBGA package. The area array solder balls beneath the BGA package have the same pitch as that of the PTH or PTH pad on the substrate. To minimize the number of signal layers on the substrate, the signal leads can be confined to the outer several rows. The inner rows are taken by the IC chip and wire bond interconnections for the cavity-down BGA. For the cavity-up BGA, the inner rows are either not used or are restricted for voltage and ground connections. Table 45 shows the maximum possible pin count for potential BGA package solutions with respect to package size and ball array pitch. The inner one third of solder ball rows are excluded from the pin count calculation in this table. If necessary, these inner rows may be used for voltage and ground connections without adding substrate complexity.

Table 45 Single Chip Packages—Ball Grid Array (BGA) Packages

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*	*2006* / *100 nm*	*2009* / *70 nm*	*2012* / *50 nm*
BGA Package Size (mm)							
Commodity	**21**	**23**	**23**	**23**	**23**	**23**	**23**
Hand-held	**23**	**23**	**23**	**23**	**23**	**23**	**23**
Cost-performance	**35**	**35**	**35**	**35**	**35**	**35**	**37.5**
High-performance	**37.5**	**42.5**	**42.5**	**42.5**	**42.5**	**45**	**45**
Automotive	**21**	**23**	**23**	**23**	**23**	**23**	**23**
BGA Array Array Pitch (mm)							
Commodity	**1.27**	**1.27**	**1.0**	**1.0**	**0.8**	**0.8**	**0.65**
Hand-held	**1.27**	**1.0**	**1.0**	**0.8**	**0.8**	**0.65**	**0.65**
Cost-performance	**1.27**	**1.0**	**1.0**	**0.8**	**0.8**	**0.65**	**0.65**
High-performance	**1.0**	**1.0**	**0.8**	**0.8**	**0.65**	**0.65**	**0.5**
Automotive	**1.27**	**1.27**	**1.0**	**1.0**	**0.8**	**0.8**	**0.65**
BGA Possible Pin Count							
Commodity	**220**	**240**	**420**	**420**	**648**	**648**	**968**
Hand-held	**288**	**448**	**448**	**684**	**684**	**1056**	**1056**
Cost-performance	**648**	**1056**	**1056**	**1624**	**1624**	**2448**	**2654**
High-performance	**1152**	**1568**	**2380**	**2380**	**3612**	**4232**	**7200**
Automotive	**220**	**240**	**420**	**420**	**648**	**648**	**968**
A = integer (BGA size/pitch); R = integer (A/3); pincount = (A–R) × R × 4; body sizes rounded to nearest JEDEC size							

FINE PITCH BGA /CHIP SCALE PACKAGES

Fine pitch BGA/chip scale packages (CSP) provide a potential solution where low weight and small size are requirements. These packages are only slightly larger than the chip itself, and are available in a variety of configurations and materials combinations. Table 46 shows two examples of the maximum possible pin count for depopulated area array fine pitch BGA/CSP solutions with respect to package size, array I/O pitch, and number of rows. For these packages the solder ball pitch is a fraction of that of the PTH on the substrate. Fan-out wiring connections are required on the substrate to reach the PTH. To minimize the fan-out requirements, only a few of the outer rows of the area array connections are

used. Fine pitch BGA/CSPs at 0.5 mm pitch will put pressure on the substrate interconnect density for I/O escape to reach the inter-level vias or the PTH in the substrate. These packages are used today primarily in low pin count applications where they provide potential advantages of higher performance, higher density, and chip shrink transparency. For applications where fine pitch BGA/CSPs are redesigned to the minimum size possible each time the chip size is reduced, this redesign will drive a corresponding redesign of the substrate onto which the packages are assembled.

Table 46 Single Chip Packages—Fine Pitch BGA/CSP

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
CSP size (mm/side)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
CSP area array Pitch (mm)	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.25**	**0.25**
# Rows/# leads	**3/204**	**3/264**	**3/264**	**3/360**	**3/360**	**3/444**	**3/444**
# Rows/# leads	**3/204**	**3/264**	**4/336**	**4/464**	**5/560**	**5/700**	**6/816**
A = integer (CSP size/pitch); R = # rows, # leads = (A–R) × R × 4							

Figure 37 illustrates Single Chip Packaging BGA and Fine Pitch BGA/CSP solutions as a function of area array pitch.

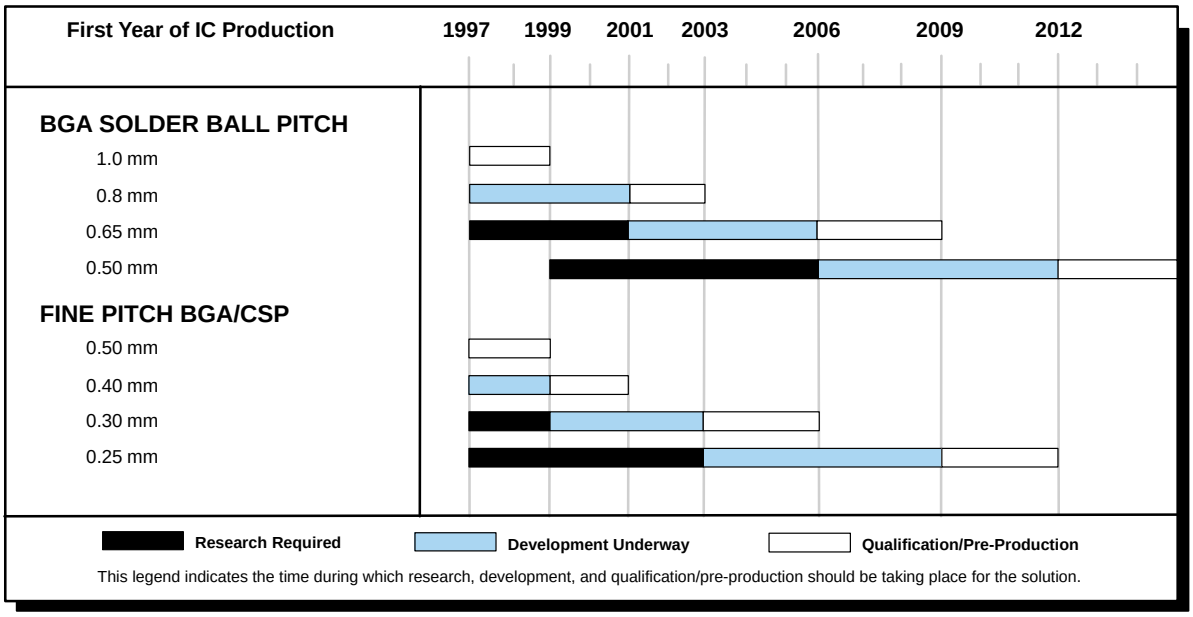


Figure 37 Single Chip Packaging—BGA and Fine Pitch BGA/CSP Potential Solutions

MULTI-CHIP PACKAGES / MODULES

Several enabling technology solutions must be available commensurate with the performance and cost noted in the *Assembly & Packaging Technology Requirements* (Table 43) to facilitate flip chip interconnect implementation for multi-chip packages/modules:

- Design tools/simulators (integrated design environment section)
- Flip chip interconnect (chip-to-next level interconnect section)
- Underfill (encapsulation and underfill section)
- High density substrates (high density substrates section)
- Low cost known good die

These enabling technologies are interdependent and must be selected to be compatible to provide an integrated multi-chip solution. Bare chips must provide the same reliability, quality, and performance as packaged chips to be considered "known good." Multi-chip packages containing 2–3 chips are in volume production today, and could evolve over the next five years to include 3–5 chips. The evolution of these multi-chip packages into multi-chip modules with more than five chips will be driven by performance and cost requirements at the sub-system and system level. Chip reworkability and module testing are important considerations for these multi-chip modules. The implementation and proliferation of multi-chip packages and modules will continue to be constrained by the availability of high density substrates and "known good" die commensurate with the necessary cost and performance. Multi-chip modules will be driven by densification and cost reduction for low end products and densification and performance for high end products.

HIGH DENSITY SUBSTRATES

To accommodate BGA packages in 1997 for the high-performance market segment, the substrate should have PTH at 1.00 mm pitch, with a sufficient number of signal layers to access 12 outer rows underneath the BGA substrate. The PTH pitch should reduce with time as indicated in Table 47 and Figure 38.

Table 47 High Density Substrates—BGA Compatible Substrates

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
PTH pitch (mm)	**1.00**	**1.00**	**0.8**	**0.8**	**0.65**	**0.65**	**0.5**
# Rows accessed	**12**	**14**	**17**	**17**	**21**	**23**	**30**

To accommodate fine pitch BGA/CSP solutions in 1997, the metal wiring on the top layer of the substrate needs to access the three outer rows. This means that the substrate should be capable of placing two signal lines between the two adjacent pads at 0.5 mm pitch. Alternatively, build-up layers may be used to access the third and higher rows should the pad pitch reduce, as indicated in Table 48 and Figure 38.

Table 48 High Density Substrates—Fine Pitch BGA/CSP Compatible Substrates

Year of First Product Shipment Technology Generatoin	*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
CSP pad pitch (mm)	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.25**	**0.25**
Pad size (μm)	**200**	**170**	**170**	**130**	**130**	**100**	**100**
Line width (μm)	**50**	**40**	**40**	**30**	**30**	**25**	**25**
Line spacing (μm)	**65**	**50**	**50**	**35**	**35**	**33**	**33**
# Rows accessed	**3**	**3**	**3**	**3**	**3**	**3**	**3**

The most stringent needs are for substrates that are compatible with flip chip solutions. Table 49 illustrates key substrate features for both PWB and thin film-based solutions shown as a function of the flip chip pad pitch, pad size, and line width/spacing. For a PWB-based substrate, one line between two adjacent pads is assumed, and two outer rows of pads connected to the IC chip can be accessed. The 100 μm pad size required in 1997 to support the pad pitch, line width, and spacing is cost-prohibitive for PWB-based solutions, and successful implementation often requires the depopulation of a significant number of pads. This challenge is exacerbated as pad sizes decrease, and requires high priority focus by the PWB infrastructure. Automotive pin count requirements are satisfied without the need for build-up layers, while additional build-up layers are needed for other market segment applications. For thin film fine line substrates, two cases are given: two lines between pads and four lines between pads (capable of accessing three and five outer rows in one fan-out layer respectively).

Shown in Table 49 are the example chip sizes and the maximum area array sizes (number of pads on one edge) for four of the market segments. All of the signal I/O pads and some of the voltage and ground pads are assumed to locate on a few of the outer rows, as shown in the table. Each of these outer row pads requires a fan-out redistribution wire on the substrate to reach a through via or PTH on the substrate for eventual connection to the global wiring in the few chip packaging substrate or a solder ball underneath a BGA package. The numbers of leads shown in Table 49 are equal to or greater than the pin count, but very often less than the pad count numbers in Assembly & Packaging Technology Requirements, Table 43. These additional voltage and ground pads needed are located in the inner rows, and connected to voltage and ground pads in the outer rows. When the IC chip size is shrunk to optimize wafer productivity, substrate redesign is usually necessary to accommodate chip shrink.

To facilitate high volume flip chip implementation, flip chip pitch must scale with silicon feature size to support chip shrinks, and substrate technology must decrease cost/layer while scaling wiring density with flip chip pitch reduction. PWB and thin film-based technologies are expected to converge during the time frame of this Roadmap. Table 49 addresses substrate escape wiring only. Global wiring solutions are addressed in the "*National Technology Roadmap for Electronic Interconnections*" (available from the IIPC)[17] and in the "*National Electronics Manufacturing Technology Roadmap*" (available from NEMI).[18] These wiring geometries are not sufficiently dense to support moving on-chip wiring onto the substrate. Substrate cost should not exceed 50–70% of the total assembly and packaging cost (cents/pin) shown in Table 43.

17. The Institute for Interconnecting and Packaging Electronic Circuits (IPC). *National Technology Roadmap for Electronic Interconnections*. Northbrook, Illinois:IPC, 1995.

18. National Electronic Manufacturing Initiative, Inc. (NEMI). *National Electronic Manufacturing Technology Roadmaps*. Herndon, VA:NEMI, 1996.

Table 49 Flip Chip Substrate Fan-out Requirements

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*	*2006* / *100 nm*	*2009* / *70 nm*	*2012* / *50 nm*
Flip Chip Pad Pitch (µm)	**250**	**180**	**150**	**130**	**100**	**70**	**50**
Pad Size (µm)	**100**	**70**	**60**	**52**	**40**	**25**	**18**
Chip Size (mm/side)							
Hand-held	**7**	**7**	**7**	**7**	**7**	**7**	**7**
Cost-performance	**12**	**12**	**12**	**12**	**12**	**12**	**12**
High-performance	**17**	**17**	**17**	**17**	**17**	**17**	**17**
Automotive	**7**	**7**	**7**	**7**	**7**	**7**	**7**
Array size = maximum # pads along chip edge							
Hand-held	**28**	**38**	**46**	**53**	**70**	**100**	**140**
Cost-performance	**48**	**66**	**80**	**92**	**120**	**171**	**240**
High-performance	**68**	**94**	**113**	**130**	**170**	**242**	**340**
Automotive	**28**	**38**	**46**	**53**	**70**	**100**	**140**
# Outer Rows Accessed (will determine # fan-out layers needed)							
Hand-held	**3**	**3**	**2**	**2**	**2**	**2**	**2**
Cost-performance	**4**	**3**	**3**	**4**	**4**	**3**	**3**
High-performance	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Automotive	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Effective Total Wiring Density for Fan-out Need (cm/cm^2)							
Hand-held	**120**	**127**	**134**	**154**	**200**	**286**	**400**
Cost-performance	**160**	**167**	**200**	**308**	**400**	**429**	**600**
High-performance	**200**	**278**	**334**	**385**	**500**	**715**	**1000**
Automotive	**80**	**112**	**134**	**154**	**200**	**286**	**400**
PWB Based Substrate (One line between pads—accessing two rows per fan-out layer)							
Line width (µm)	**50**	**34**	**30**	**26**	**20**	**15**	**10**
Line spacing (µm)	**50**	**38**	**30**	**26**	**20**	**15**	**11**
Thin Film-based Substrate (Two lines between pads—accessing three rows per fan-out layer)							
Line width (µm)	**30**	**22**	**18**	**15**	**12**	**9**	**6.1**
Line spacing (µm)	**30**	**22**	**18**	**16**	**12**	**9**	**6.6**
Thin Film-based Substrate (Four lines between pads—accessing five rows per fan-out layer)							
Line width (µm)	**16.2**	**11.7**	**9.5**	**8.2**	**6.2**	**5**	**3**
Line spacing (µm)	**17**	**12.6**	**10.4**	**9**	**7**	**5**	**4**
# Leads Accessed							
Hand-held	**300**	**420**	**352**	**408**	**544**	**784**	**1104**
Cost-performance	**704**	**756**	**924**	**1408**	**1856**	**2010**	**2844**
High-performance	**1260**	**1780**	**2160**	**2500**	**3300**	**4740**	**6700**
Automotive	**208**	**288**	**352**	**408**	**544**	**784**	**1104**
A = array size, R = # rows, # leads = (A–R) × R × 4; via pitch must be ≤ pad pitch							

Figure 38 illustrates the BGA, fine pitch BGA/CSP and flip chip interconnect compatible high density substrate solutions as a function of pitch, line width, and line spacing.

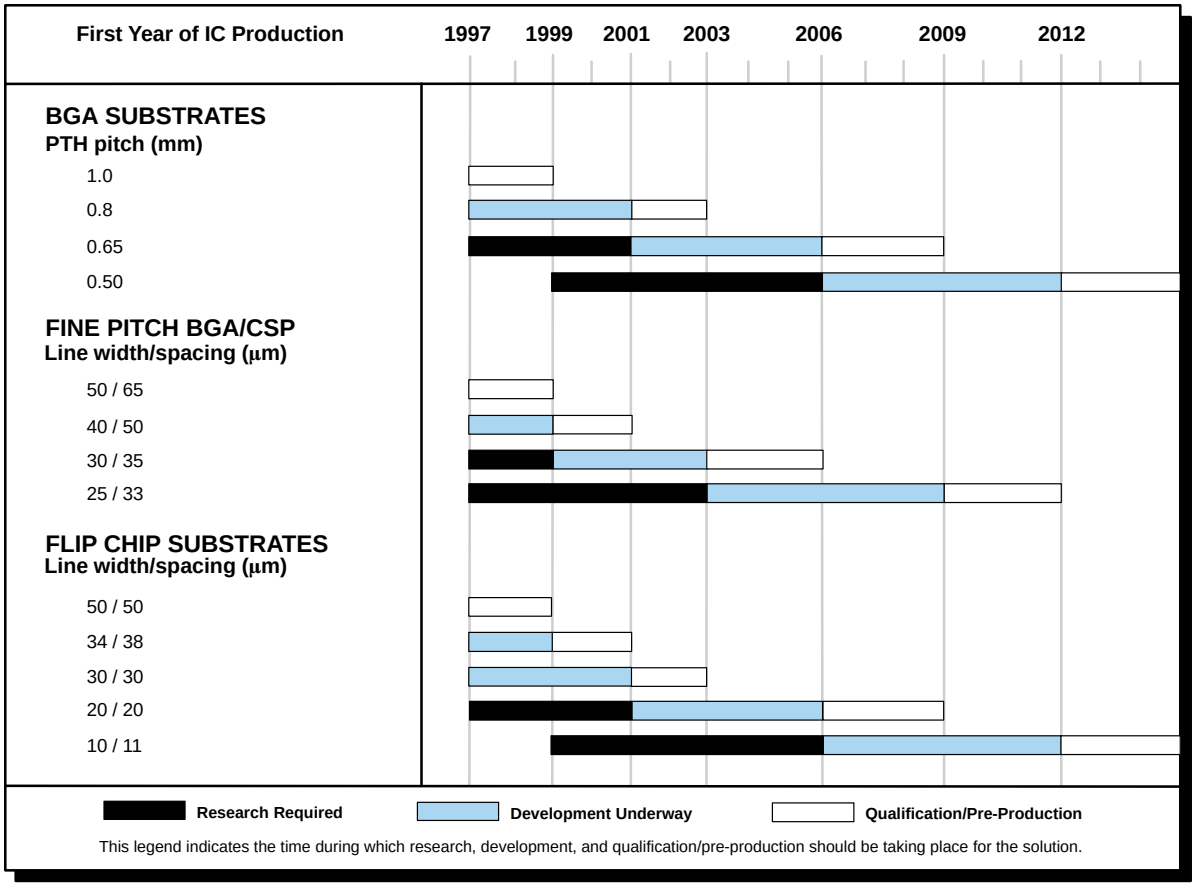


Figure 38 High Density Substrate Potential Solutions

RADIO FREQUENCY (RF) AND MIXED SIGNAL PACKAGING

Microwave packages are presently regarded as separate elements that are wrapped around the device/circuit *after* it is designed. Advances in BGA packages, fine pitch BGA/CSP packages, and flip chip interconnect will eliminate the package as a separate element. Special developments, such as hermetic coatings at the junction level applied during wafer processing, will speed the transition from ceramic packages to plastic and flip chip techniques. The performance basis for selecting ceramic over plastic laminate will be reduced as improvements in high-performance plastic materials exhibit cost advantages over ceramics. Process-oriented manufacturing and increasing levels of integration in both the active and passive areas will make possible the one-chip RF front end, and show the way to the one-chip radio, progress necessary for low cost high volume wireless applications. Integration of antenna structures into the package and control of unwanted electromagnetic radiation and absorption will pose significant packaging challenges.

RELIABILITY ISSUES

Standard methods and acceptance criteria for interfacial adhesion are lacking. Fundamental work is needed to establish adhesion strength and degradation rate versus environmental factors (temperature, relative humidity) all as a function of interfacial physical (roughness, composition, etc.) and chemical (van der Waals, dipole, covalent) properties. New materials (organic passivations, underfills, copper metalization/low κ [ε_r] dielectrics on the chip) are being added to an already complex, poorly understood interfacial adhesion reliability issues. It is essential that materials characterization be

increased and that data be available when new materials are introduced. Also lacking are the empirical and theoretical data and mathematical framework to model response versus "What if?" and versus environmental stress.

New package designs, materials, and technologies will not be capable of reliable performance in all market applications. A uniform set of environmental expectations for each market application segment would facilitate package development aimed at specific markets' applications and help ensure consistent reliability performance among suppliers as well as between suppliers and customers. Low alpha materials need to be considered during the timeframe of this roadmap to reduce alpha particle emission induced soft error upset. The CTE mismatch between the chip and the substrate should be reduced during the time frame of this roadmap in order to mitigate large chip packaging-related reliability issues. Improved handling solutions for bare chip and packaged devices will help reduce electrostatic discharge (ESD) related reliability issues.

CROSSCUT NEEDS

ENVIRONMENT, SAFETY, & HEALTH

Assembly and Packaging must consider potential risks or challenges that may be passed onto the interim buyer and the final consumer. Materials used should allow for hazard-free handling and eventual disposal or recycling. Because the majority of assembly and packaging is located offshore, multiple jurisdictions and regulatory bodies must be considered.

Table 50 Assembly & Packaging ESH Crosscut Issues

ISSUES AND CHALLENGES	*POTENTIAL SOLUTIONS*		
	1–5 YEARS	*5–10 YEARS*	*10–15 YEARS*
Regulatory pressure to reduce use of Pb in lead finish and flip-chip solder bump application by 20% (elimination for European automotive application)	Ensure that alternative material does represent overall improvement from ESH perspective	Reduce use of Pb in lead finish and flip chip solder bump application by 80%	Elimination of Pb for lead finish
Several chemicals currently used in assembly/packaging processes represent potential risks to workers and the environment	Improved management of current set of hazardous chemicals used in plating processes to reduce potential risks to workers, including plating baths for: – Cu – Ni – Au – Co – Pb	Ensure that all hazardous chemicals used in flip chip and bump technology (and other new packaging technologies) undergo evaluation through application of DFESH* tools to ensure continuous improvement in ESH maintains pace with new process developments and effectively screens out undesirable chemicals and processes	Identify and implement processes that use ESH-benign materials
Eliminate use of Kr–85 for fine leak tests	Replace with processes using He or other inert material		
Need to integrate ESH considerations into equipment design	SEMI S2/S8 applied to assembly/packaging tools; tool ESH evaluations ensure that no single point failure may result in life threatening risk	SEMI S2/S8 applied to 100% of all assembly/packaging tools performed by 3rd party evaluation	

** DFESH—design for ESH*

Table 50 Assembly & Packaging ESH Crosscut Issues (Continued)

ISSUES AND CHALLENGES	POTENTIAL SOLUTIONS		
	1–5 YEARS	*5–10 YEARS*	*10–15 YEARS*
Eliminate use of cadmium (e.g., rust protector)	Find suitable alternative		
Eliminate use of antimony-trioxide as flame retardant in mold compound	Find suitable alternative		
Elimination of brominated flame retardants	Find suitable alternative		
Elimination of beryllium as substrate material			Find suitable alternatives
Pressure to reduce water consumption in plating and other processes	Implement water recycling/reuse programs reducing overall consumption by 20%	Implement water recycling/reuse programs reducing overall consumption by 50%	
Pressure to reduce energy consumption	Improve efficiency of mold presses, furnaces, and other high energy consumption equipment to reduce overall energy uses by 20%	Improve efficiency of mold presses, furnaces, and other high energy consumption equipment to reduce overall energy uses by 50%	
Pressure to reduce chemical usage and consumption	Improved recycling of chemicals in plating operations; reduce overall usage by 20%	Improved recycling of chemicals in plating operations; reduce overall usage by 50%	Improved recycling of chemicals in plating resulting in zero-discharge operation
Minimize waste mold compound material		Thermo-plastic versus thermo-set to optimize use of mold compound (reduce unused trim material or runners	
Product take back			ESH benign chip packages that can be returned to manufacturer or reprocessor for reuse

METROLOGY

SCOPE

Assembly and packaging will continue to play a significant and increasing role in the size, performance, and cost of future electronic systems. This section summarizes the metrology challenges associated with assembly and packaging. This is not an exhaustive summary; it attempts to highlight the most critical areas of interest.

CURRENT TECHNOLOGY STATUS AND FUTURE NEEDS

Table 51 Assembly & Packaging Metrology Crosscut Issues

ASSEMBLY AND PACKAGING METROLOGY NEEDS	SUMMARY OF ISSUES
Electrical simulation models of packages and systems (modeling system of chips pushing the practical limits of cost and time effectiveness)	Improvement needed for coupling between components, mixed signal simulation, power disturbs, and EMI Parameter extractions of 3-dimensional interconnect and power delivery structures Integrated electrical (architecture), mechanical, thermal, and cost modeling tools needed for cost and cycle time reduction
Accelerated stress methods tests representative of application	Improved accelerated stress test techniques needed to qualify manufacturing processes, and to improve the lifetime and successful operation of the product Research needed on failure modes and mechanisms for finding accelerated stress techniques that mimic "real life"
Measurement and modeling of interfaces (thermal performance, reliability, yield, and cost are driven by understanding of interfaces)	Need to measure, design, and control the basic mechanisms (physical, chemical, mechanical) for interface bond strength (adhesion)
Thermal and mechanical simulation models of packages and assemblies	Comprehensive thermal and mechanical model tools fully supported by "real life" materials data Measurement of *in situ* properties, location, and characterization of defects and failures
Material parameters	Measurement, collection, and dissemination of materials properties of packaging materials for the sizes, thicknesses, and temperatures of interest
Material application and assembly process control	Improvements in the online measurement of solder systems, solder alternatives, underfills, encapsulants, attachment materials, etc., in the manufacture of packages and bumped chips

MODELING & SIMULATION

Assembly & Packaging technologies are driven to simultaneously meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. Therefore, advanced modeling tools are needed that cover electrical, thermal, and mechanical aspects.

These phenomena can no longer be described independently. Major advances are needed in the individual tools and in their integration to achieve a self-consistent solution. To move to 1.5 GHz chip-to-board speeds, the modeling of electrical signal propagation needs to be improved substantially from approximate RLC modeling to full transmission line modeling. Mechanical stresses need to be coupled between chip and package level. The introduction of low κ dielectrics with low thermal conductivity will increase the need for accurate thermal simulation, which needs to be solved consistently with electrical behavior given the higher power dissipation levels.

ELECTRICAL SIMULATION MODELS OF PACKAGES AND SYSTEMS

Modeling the electrical behavior of systems of chips packaged individually or collectively in single or multi-chip packages is pushing the practical limits of what can be done in a cost and time effective manner. Refinement and validation of modeling tools on circuit and system performances are needed, including coupling between components, mixed signal simulation, power disturbs, and EMI. Parameter extraction of the three dimensional interconnect and power delivery structure, and experimental study and validation of those parameters, will also require further research and development. Integrated electrical (architecture), mechanical, thermal, and cost modeling tools will be useful tools for integrated design and manufacturing teams with potential for cycle time reduction.

THERMAL AND MECHANICAL SIMULATION MODELS OF PACKAGES AND ASSEMBLIES

The industry continues to increase power dissipation, junction temperature, and reliability expectations that push the cooling and mechanical strength limits of electronic products. More comprehensive thermal and mechanical model tools fully supported by "real life" materials data correlated with physical measurements are needed. Examples include fluid and solid models for air flow characteristics, stress predictions in accelerated tests and power cycles, micro-models for interface fracture behavior, and macro structure models for package dynamics behavior including vibration and mechanical shock. These model methods are also being applied to manufacturing and assembly processes such as adhesive/underfill flow or BGA rework. Better experimental capability for measurement of *in situ* properties, location, and characterization of defects and failures are needed. Key is development of *in situ* model mechanism elucidation and validation tools such as micro-Moire, nano indentation techniques, and interface fracture toughness techniques.

MEASUREMENT AND MODELING OF INTERFACES

Assembly and packaging thermal performance, reliability yield, and cost are driven by the understanding of interfaces and ability to characterize, control, and strengthen them. The ability to accurately qualify, and perhaps design and control the interface performance, will remain crucial to future cost-effective development and manufacturing. The key is to fully characterize the basic mechanisms (physical, chemical, mechanical) for interface bond strength (adhesion) between metal/polymer, polymer/polymer, and metal/inorganic dielectric materials, as well as to quantitatively qualify the very low levels of complex organics present at these interfaces through manufacturing processes. This understanding will be crucial to improve the interface integrity.

The Technology Roadmaps

Crosscut Technology Working Groups

ENVIRONMENT, SAFETY, & HEALTH

SCOPE

During the strategic period of this Roadmap, the regulatory environment in all aspects of Environment, Safety, & Health (ESH) will continue to refine command and control requirements. Additionally, there is a growing component of voluntary ESH management in specific areas.

There are international guidance and regulations developing in environmental management (ISO 14000) and specific chemical use and waste management areas that have a growing implication on world-wide manufacturing flexibility and marketing.

Continuous improvement in ESH characteristics of semiconductor manufacturing to meet local, national, and international needs must be accomplished, over the long term, with positive impact on cost, performance, and schedule. The leading role for these changes must be assumed by process and facilities engineers in partnership with ESH professionals, equipment and chemical suppliers, and university researchers.

The roadmap chapters on Lithography, Interconnect, Front End Processes, Factory Integration, and Assembly & Packaging should be studied for their specific ESH challenges and potential solutions.

DIFFICULT CHALLENGES

The ESH technology challenges, needs, and potential solutions in this roadmap are divided into four categories that are all essential to a synergistic ESH strategy. *Chemical Management* must provide the means to select ever "better" chemicals for function and ESH improvement. Early information to users on the environmental and health characteristics of potential new process materials will minimize the "showstopper" affect a wrong choice can have later. *Natural Resource* use reduction (water and energy) will grow in importance with respect to cost reduction and manufacturing location flexibility. *Worker Protection* is always a top priority. As more is known world-wide about potential impacts of the work environment on health and safety, technology improvements need to be made in facilities, tools, personal protective equipment, and training. To address the above issues in a cost-effective and timely way, improved ESH *Design Tools* are needed to enable a broader set of people to make trade-offs and decisions.

The three most imminent difficult technical challenges are—1) early distribution of chemical and material toxicity and safety information to users; 2) water and energy use reduction; and 3) perfluoro-compound (PFC) emissions reduction. Table 52 includes the ESH challenges. Table 53 lists the ESH technology requirements.

Table 52 ESH Difficult Challenges

FOUR DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
New chemical qualification	Need to conduct thorough, new chemical reviews and ensure that new chemistries can be utilized in manufacturing without jeopardizing human health or the environment or delaying process implementation
Reduce PFC emissions	These gases are used in plasma processing. There are no known alternatives. International regulatory scrutiny is growing.
Reduce energy and water use	Limits fab location/size in certain geographic regions
Integrated ESH impact analysis capability	No integrated way to evaluate and quantify ESH impact of process, chemicals, and process tools
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Eliminate PFC emissions	No known alternatives and international regulatory pressure
Know detail chemical characteristics before use	Need to document toxicity and safety characteristics because of international regulatory pressure
Lower feed water use 10× and purification cost by 2×	Lower use and cost to reduce impact to productivy curve and for factory location flexibility
Lower energy usage per unit of silicon 2×	Reduce global warming impact of energy use. Energy availabiity in market area.
Integrated ESH impact analysis capability for new designs	No integrated way to make ESH a design parameter in development procedures for new tools and processes

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

CHEMICAL MANAGEMENT

The major ESH challenge for development of new semiconductor process technologies is to select chemicals that minimize risks to safety, public and employee health, and the environment. Concern over the industry's ability to utilize new chemicals for manufacturing (e.g., toxicity issues regarding new metal and dielectric film precursors, and resist materials) requires a robust selection process. Figure 39 shows the set of potential solutions.

An ESH chemical assessment must become an integral part of the overall technology assessment for new process chemical selection. This inclusion of an ESH chemical assessment will require a more cooperative and concerted approach between process and ESH professionals and engineers. It will also require closer interactions between researchers, chemical suppliers, tool suppliers, and semiconductor manufacturers to ensure that the new chemicals needed for manufacturing are available when new processes must be implemented. This integrated methodology, in turn, becomes part of the ongoing process improvement cycle.

Table 53 ESH Technology Requirements

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Chemical Management						
Chemical assessment	**Methods developed**	**Data**				
PFC emissions minimization		**Improved by-product use/mgmt**			**Eliminate**	
Metal/dielectric precurser chemicals			**By-product use/mgmt**		**Use/replace**	
HAPs* precursors			**By-product use/ mgmt/ replace**			
Solvents			**By-product use/mgmt**	**Solvents use/replace**		
CMP† materials			**By-product use/mgmt**	**Use/replace**		
Natural Resources						
Decrease net feed water use (Gal/in^2 silcon)	**30**	**10**	**6**	**5**	**2**	**2**
Decrease UPW** use (Gal/in^2 silicon)	**22**	**10**	**7**	**6**	**5**	**5**
Lower water purification cost	×	**90%**×	**80%**×	**70%**×	**60%**×	**50%**×
Decrease energy consumption (KWh/in^2 silicon)	**9**	**8**	**7**	**5**	**5**	**4**
300 mm energy consumption (KWh/in^2 silicon)			**4**	**4**	**4**	**3**
Worker Protection						
Equipment/facility safety improvements		**Suppliers full imple-mentation of SEMI S2, S8 guidelines**				
Reduced chemical exposure	**Improved toxicity risk assessment tools/data**	**Reduced toxicity/ quantity of chemicals**	**Reduced protective equipment dependency**			
Ergonomic improvement			**Improved work environment**	**Reduced reliance on garments**		

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *HAP—hazardous air pollutants*
** *UPW—ultrapure water*
† *CMP—chemical mechanical polish*

Requirement data for 1997 are based on industry data. Requirements beyond 1997 are best estimates by TWG consensus.

Table 53 ESH Technology Requirements (Continued)

Year of First Product Shipment Technology Generation	*1997 250 nm*	*1999 180 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Design Tools						
Software design tool development	**Tool benefits and barriers determined**	**Cost and relative risk models refined**	**Mass-energy balance model available**	**Integrated tools and evaluation method-ology**		
Design tool integration in work practice	**Used by ESH profes-sionals**	**Used by key process engineers**	**Used by integrated process/ ESH design teams**			
No barriers to market access	**Abridged life cycle assessment**		**Analysis tool for market risks and barriers**	**Full life cycle assessment method-ology**		
Source data	**Faster access to toxicology data**	**Individual process simulation models**	**Common database for process and ESH**	**Source data used by process and equipment design teams**		
Absolute risk determination				**Improved method-ology and data**	**Results for key processes**	

Solutions Exist *Solutions Being Pursued* *No Known Solution*

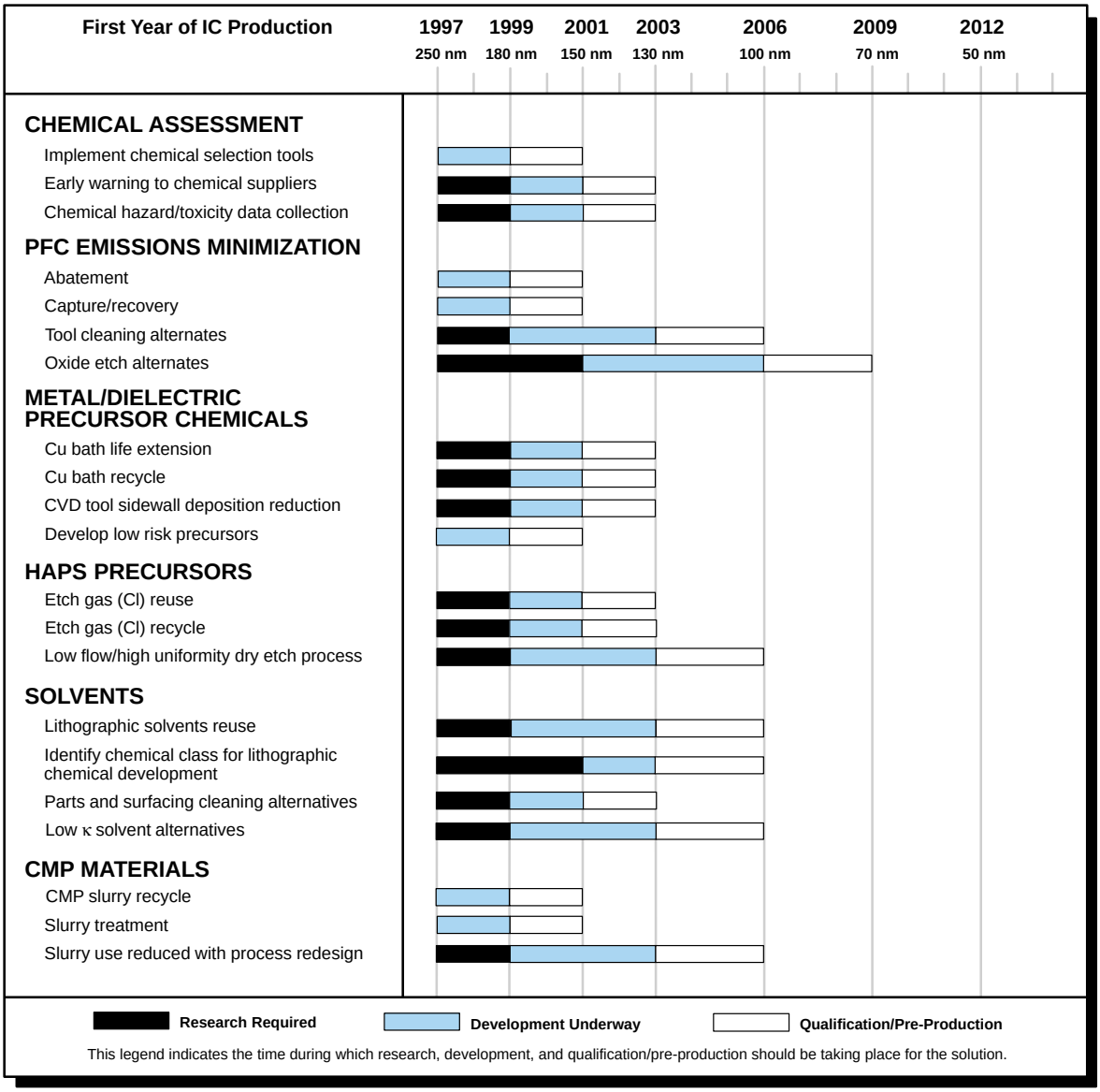
ESH chemical assessment consists of a four-step process as follows:

1. Data Collection
   - Environmental characterization
   - Political, regulatory, public factors
   - Health effects
   - Hazard analysis
2. Chemical Assessment
   - Integrated data review
   - Conclusions on risk and environmental impact potentials
   - Resolution of issues limiting use
3. Process Integrated Use Assessment
   - Employee health and safety analysis
   - Chemical selection hierarchy

     Chemical selection minimizes risk by using the following hierarchy: 1) uses more benign materials (replacement); 2) uses the least amount of chemical possible (reduction); 3) reuses the chemical to the greatest extent possible (capture and reuse); 4) utilizes the used chemical's remainders in other commercial applications (reclaim); and 5) converts the discarded chemical to a more benign form (abatement). Existing use of chemicals from a number of high concern categories (HAPs, PFCs, CMP slurry materials, and organic solvents) will also utilize this framework for reducing risks.

4. Decision to Use/Continue Use of the Chemical
   - Revisit steps 1, 2, and 3 periodically or as needed.

In addition to chemical selection the industry must develop ways to reduce the overall chemical use. *In situ* sensors must be developed to aid in optimizing process and elimination of test wafers.



CVD—chemical vapor deposition

Figure 39 Chemical Management Potential Solutions

NATURAL RESOURCES

The increase in wafer size, the need for higher water purity, and the increase in process steps indicate a potential trend for higher water usage per wafer. This trend can be reversed by a combination of strategies including development of higher efficiency rinse processes; recycling of higher quality water for process applications; and reuse of lower quality water for nonprocess applications. Figure 40 illustrates the ESH Natural Resources potential solutions. Process simulation and cost optimization tools are required to determine the optimum balance of these measures at different factories and different locations. To successfully operate future water systems with recycle and reuse capabilities, reliable and fast response sensors are needed for online monitoring of key contaminants. System simulation tools and advanced control strategies are needed to design and operate the future UPW plants as well as the future water distribution and wastewater collection systems. New high efficiency water purification methods are needed to reduce energy and chemical usage. New factories designed with the idea of matching the water purity supplied with the purity required are critical; this will reduce the waste and minimize the environmental impact of water usage.

In 1995, electricity consumption by the U.S. semiconductor industry totaled 8.4 billion kWh,[19] [20] the largest amount in the industry's history. Electrical energy comprises approximately 11% of cost of consumables used in manufacturing 6-inch ASIC wafers. Based on SEMATECH data, the electric bill is often the largest or second largest expense item, at 25–40% of a facilities operating budget (excluding capital and construction). Each dollar savings in operating costs saves a company from having to generate five dollars of revenue. Reducing these costs helps the industry stay competitive.

The efficient use of energy is at its historic best at 9 kWh/square inch silicon. While this trend in increased efficiency has been growing in the past decade, in the past few years the efficiencies have begun to level off. The historical efficiencies are mainly driven by more energy-efficient facilities equipment, improved facility designs, wafer size increases, and to some extent, productivity and yield improvements. Without further technology developments, energy efficiency may not improve much below 9 kWh/square inch silicon.

While new generations of facilities equipment are becoming more energy efficient due to supplier investments in R&D, more attention focused at the source—the manufacturing equipment—is critical. Minimal efforts have been undertaken to reduce manufacturing equipment's energy consumption. Equipment systems such as plasma generating systems and vacuum pumps offer opportunities for investigation and improvements. Equipment utility requirements such as exhaust, process cooling water, UPW, and electricity must be re-examined with conservation in mind. Careful examination is required of utility setpoints such as chilled water ranges for tolerance requirements. Since etch and thin film processes consume 50% of the electricity, efforts start with this equipment first. Facility design models incorporating more energy conservation considerations need to be developed.

19. 1990–1994 Annual Surveys of Manufacturers, U.S. Department of Commerce, Bureau of Statistics.

20. Dataquest Incorporated. *1996 Silicon Wafer Market Share Estimates, Market Statistics*. SEMM–WW–MS–9702. San Jose: Dataquest Incorporated, July 21, 1997.

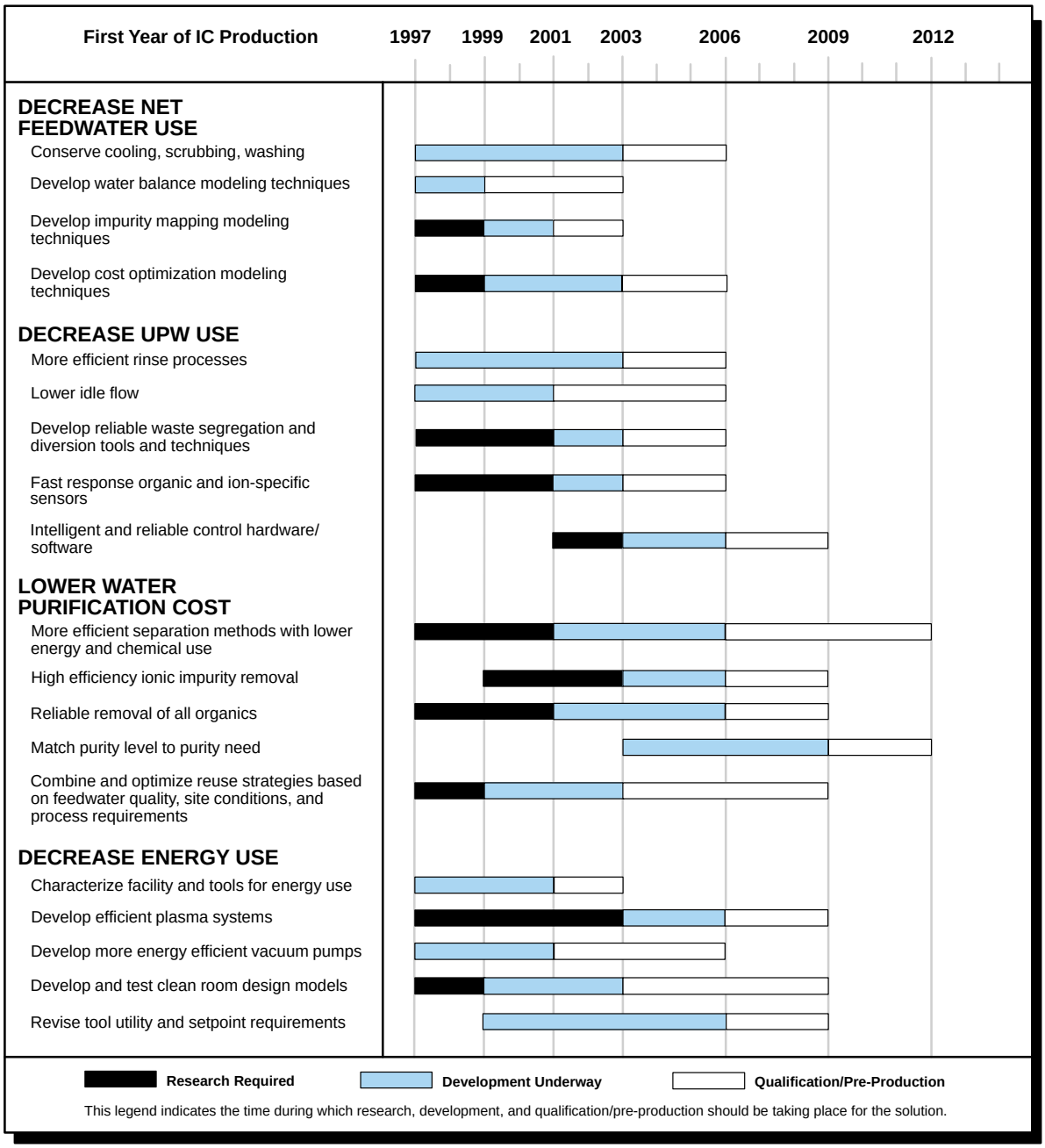


Figure 40 Natural Resources Potential Solutions

WORKER PROTECTION

A number of issues loom as potential showstoppers. Included among these are the use of known extremely toxic chemicals; the use of new chemicals for which the toxicology is unclear; the use of materials that are not on the Toxic Substance Control Act (TSCA) inventory or that are not covered by a Significant New Use Rule (SNUR); and the use of HAPs. In the future, more attention will be focused on both the manufacturing equipment for semiconductors and the process chemicals. Ergonomic design will become the norm. In particular, documents such as SEMI S2[21] and S8[22] will find increased use by equipment suppliers and must become a routine business practice. The risk associated with changing

21. SEMI, S2–93A, *Safety Guidelines for Semiconductor Manufacturing Equipment.*

22. SEMI, S8–95, *Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Equipment.*

chemicals or using new chemicals will be evaluated using risk assessment and risk management procedures. Along with deployment of risk assessment methodology, there is still an ongoing need to identify more reliable, cost-effective tools to monitor work areas for potential exposure to toxic chemicals.

Other issues related to worker protection that must be considered include identification and use of cost-effective, noncombustible wet deck construction materials; improved information flow at worksites to ensure that accurate, appropriate information is disseminated to all employees; increased attention to maintenance operations; and understanding the risks and implications of physical hazards in the workplace. Figure 41 presents the potential solutions.

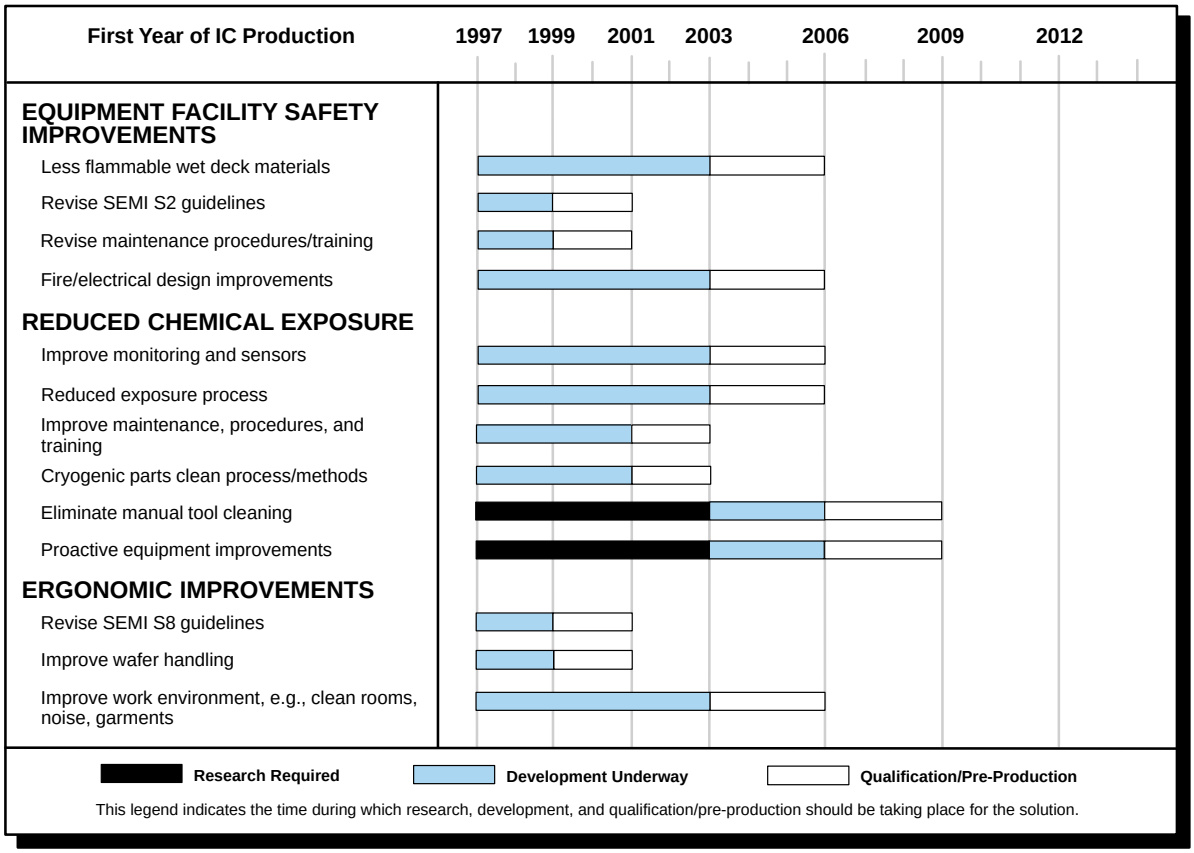


Figure 41 Worker Protection Potential Solutions

DESIGN TOOLS

Semiconductor manufacturers tend to focus on cost, yield, and logistics as the primary factors in product and process selection. However, because of the costs associated with ESH risks, these impacts are also becoming important drivers in design and operational decision-making. ESH issues have resulted in major post-installation changes to processes and increased operational costs because these issues were not considered initially. To reduce ESH-related costs, risk factors must be evaluated and counteracted at an early stage in product/process design. The early consideration of ESH risks and costs represents a paradigm shift within the industry. Only with close collaboration between the design and process engineers and ESH professionals will it be possible to maintain ESH priorities consistent with other business performance goals. Design tools are needed to assist process engineers and ESH professionals in making these tradeoff decisions. The ESH design tools potential solutions are shown in Figure 42.

Although the current suite of ESH design tools (e.g., safety checklists, risk assessment, life-cycle analysis, material/energy flow modeling, and cost accounting) serve the industry well, a next-

generation refinement is required. Country-specific regulatory requirements and consumer demand for low-ESH impact products will limit the industry's ability to manufacture and market products. Assessment tools must focus on the ESH factors that may impact the access to manufacturing resources and markets. The value of such tools can best be conveyed through a history of case studies that demonstrates the risk and indicates the cost reductions that can be achieved. For design and process engineers to use ESH design tools, the tools must be robust, easy to use, and have low maintenance requirements for data collection, upkeep, and interpretation. In addition, technology transfer of ESH design tool technology and implementation strategies must be refined to be congruent with the high rate of change within semiconductor manufacturing.

A key to the successful use of ESH design tools is the availability of data on process by-products, human toxicology, and environmental effects. A typical Materials Safety Data Sheet (MSDS) provides inadequate information to estimate the relative ESH costs and risk for process alternatives. Needed are methodologies to quickly estimate the human toxicology and environmental fate of new process chemistries, and more detailed empirical studies and modeling techniques to estimate plasma process by-products.

While risks of major incidents (fire, explosion, etc.) are very low in the semiconductor industry, it may be desirable to apply absolute risk methodologies to assess and further reduce the risks associated with critical process tools and facility systems. These calculations require that data on component reliability and human error rates be gathered over a sufficient length of time.

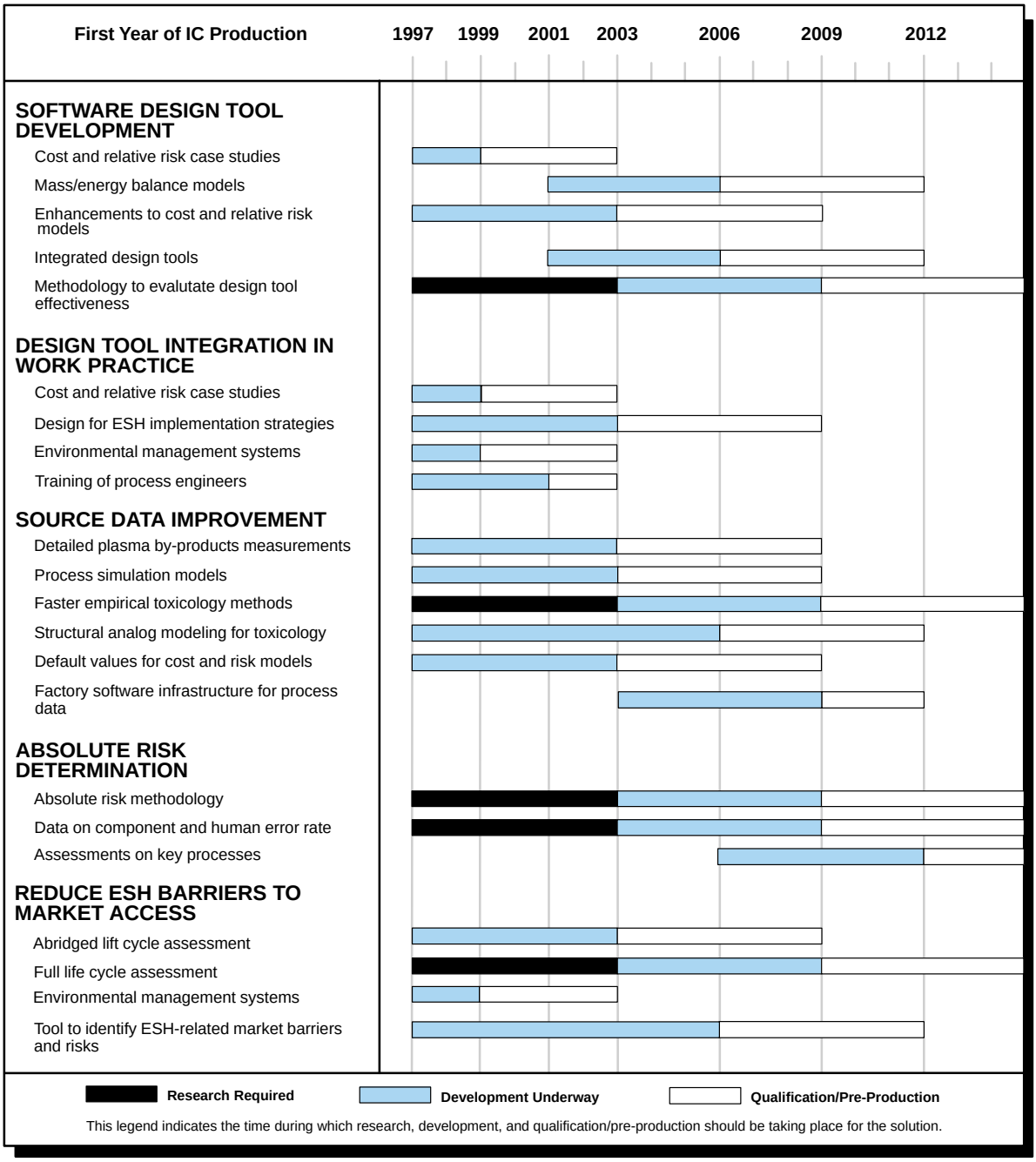


Figure 42 ESH Design Tools Potential Solutions

DEFECT REDUCTION

SCOPE

The scope of defect reduction has been greatly expanded to address the entire yield learning process, including impact on device performance and reliability. As such, the *Defect Reduction* section has been partitioned into four focus topics; *Yield Model and Defect Budget*, *Defect Detection*, *Defect Sources and Mechanisms*, and *Defect Prevention and Elimination*. These topics correspond with the learning cycle typical of yield engineering and defect reduction. Key business metrics rely on the success of rapid yield improvement and the associated competencies of defect allocation, formation, transport, deposition, detection, characterization, reduction, and elimination. These competencies crosscut packaging and all process technologies, as well as the facility infrastructure, device design, and process integration. Key messages of this revision include the importance of continued development and availability of defect detection, review, and classification technologies where much greater sensitivity and throughput is necessary. Reduction of process/equipment generated defects is paramount to meet defect targets for 60% first year yield and expected 85%–95% yield in mature products. Order of magnitude improvements in process critical fluid impurity levels are not believed to be necessary well into the sub-100 nm regime. Defect to fault transformations, kill ratios, and isolation techniques are also believed to be critical challenges as physical device dimensions and corresponding defect dimensions continue to shrink.

DIFFICULT CHALLENGES

The difficult challenges for defect reduction technologies are summarized in Table 54. Defect budgets will require frequent revalidation and updates as information about future processing technologies becomes available. Yield models need to better consider complex integration issues and parametric yield losses for future technology nodes. Future defect models must consider electrical characterization information, with reduced emphasis on visual inspections and analysis. Detecting defects associated with high aspect ratio contacts, and combinations of canals and vias in dual-Damascene structures will continue to be among the most difficult defect detection challenges. Exacerbating this challenge is the need to couple high sensitivity with high throughput—a tradeoff typically accepted today for optimization of tool performance for either baseline yield learning or production line monitoring. Fault isolation complexity is expected to grow exponentially and represent an extremely difficult task of defining both horizontal plane and vertical layer fault location dimensions. Circuit failures that leave no detectable physical remnant present an extremely difficult task in establishing root cause. Statistical means of accurately dealing with near zero defect adder data that frequently exhibit high coefficients of variation is a fundamental data reduction challenge. Through the use of advanced test structures and modeling techniques, the fundamental challenge in the area of process critical materials is to understand the correlation between impurity concentration and device yield, reliability, and performance. This correlation will determine whether increasingly stringent contamination limits are truly required and to provide early warning of needs for tighter specifications. Process tools must have capability to automatically self-monitor so as to predict yield excursions, failures, and faults, and to initiate corrective actions.

Table 54 Defect Reduction Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Development, validation,and use of accurate defect budget models	Development of test structures for new technology nodes Correlated process-induced defects (PID), particles per wafer per pass (PWP), product inspections, and *in situ* measurements Sampling and statistical issues with ultra-small populations Impact of within-wafer variations on yield predictions
Inspection of high-aspect ratio contacts/vias/trenches	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Correlation/validation of trace impurity specifications within process critical materials	Test structures and advanced modeling needed to determine impact of trace metallics, ions, organics on device performance, reliability, and yield
Fault isolation	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed.
Defect-free, intelligent equipment	Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Budgeting defect targets to new tools and processes	Parametric yield loss models Modeling complex integration issues Ultra-thin film integrity modeling Better methods of scaling front end process complexity that considers increased transistor packing density
Ability to rapidly detect defects, residues, and particles at critical size	Existing techniques tradeoff throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity.
Minimize inspection costs in high-volume production environments	Equipment must effectively utilize real time process and contamination control through *in situ* sensors. Inspection must occur during yield ramp and by exception only in a production environment.
Ability to accurately characterize defects	Defect characteristic data will be necessary to enable continued yield learning. Inline defect detection data must include size, shape, composition, etc., all independent of location and topology.
Failure analysis of nonvisual defects	Techniques are needed to enable sourcing of defects where no physical remnant is detected

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

The defect budget technology requirements are based on the negative binomial yield model where Y is the defect-limited yield, A is the critical area of a device, D_0 is the defect density and α is the cluster factor. For this revision, $\alpha = 2$ and Y = 60%, or the yield expected in the first year of manufacturing production. Requirements for the 1997 250 nm technology node use the results of a 1996 study of current process-induced defects (PID) at SEMATECH member companies. The defect budget technology requirements were extrapolated from the median PID value of each process module by considering increase in area, increase in complexity, and shrinking feature size. Considering increase in complexity is new to this revision.

$$Y = \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha}$$

$$PID_n = PID_{n-1} \times \frac{F_n}{F_{n-1} \left(\frac{S_{n-1}}{S_n} \right)^2}$$

The extrapolation uses the equation where PID is the particle induced defect density per square meter, F is the average faults per mask level, S is the minimum defect size, and n refers to the technology node. Each entry in Table 56 refers to a typical tool within the process zone. Since the actual tools and processes are not known, this roadmap assumes that no new process, material, or tool will be acceptable with a larger PID budget than prior methods. This assumption needs periodic validation. This defect budgeting method tends to be a worst case model since all process steps are assumed to be at minimum device geometry. Many processes allow process zones with more relaxed geometries. However, manufacturing uses tools at both minimum and relaxed geometries. Thus a worst case defect budgeting model is prudent. As the number of defects per square meter shrink with technology improvement, the metric, defects per square meter, becomes less meaningful. Thus the Defect Reduction TWG proposed a new defect metric—mean wafers between defects (MWBD). This metric recognizes that defectivity is moving away from the random defect statistics and toward reliability statistics. Table 55 shows MWBD for handling defects. Table 56 presents the tool defect targets necessary to meet the overall 60% first year yield indicated in the Overall Roadmap Technology Characteristics (Table B1).

Table 55 Mean Wafers Between Handling Defects

Year of First Product Shipment Technology Generation	*1997 250 mm*	*1999 180 mm*	*2001 150 mm*	*2003 130 mm*	*2006 100 mm*	*2009 70 nm*	*2012 50 nm*
Wafer Handling (Defects/Meter^2)	**30**	**13**	**8**	**5**	**2**	**1**	**1**
Wafer Size	**200**	**300**	**300**	**300**	**300**	**450**	**450**
Mean Wafers Between Handling Defects	**1.06**	**1.08**	**1.76**	**2.73**	**5.81**	**6.78**	**11.2**

Table 56 Yield Model and Defect Budget Technology Requirements

Year of First Product Shipment Technology Generation		*1997 250 nm*	*1999 180 nm*	*2001 150 nm*	*2003 130 nm*	*2006 100 nm*	*2009 70 nm*	*2012 50 nm*
Critical Defect Size (nm)		**125**	**90**	**75**	**65**	**50**	**35**	**25**
Electrical D_0/m^2 60% Yield†		**1940**	**1712**	**1512**	**1353**	**1119**	**939**	**776**
Microprocessor Area (mm^2)		**300**	**340**	**385**	**430**	**520**	**620**	**750**
Mask Levels		**22**	**23**	**23**	**24**	**25**	**27**	**28**
Faults per Mask Level		**88**	**74**	**66**	**56**	**45**	**35**	**28**
PID Budget (defects/m^2) at 60% Yield (1st Year of Production)								
FEOL*	Doping	**860**	**376**	**231**	**149**	**70**	**27**	**11**
	Interconnect	**1076**	**471**	**289**	**186**	**87**	**33**	**14**
	Surface Prep	**1642**	**718**	**441**	**284**	**133**	**51**	**21**
	Thermal/Thin Film	**850**	**372**	**228**	**147**	**69**	**26**	**11**
BEOL**	Interconnect	**605**	**265**	**162**	**105**	**49**	**19**	**8**
	Planarization	**1418**	**620**	**380**	**245**	**115**	**44**	**18**
	Surface Prep	**1718**	**751**	**461**	**297**	**140**	**53**	**22**
FEOL/BEOL	Lithography	**648**	**284**	**174**	**112**	**53**	**20**	**8**
	Metrology Inspection	**1195**	**523**	**321**	**207**	**97**	**37**	**15**
	Wafer Handling	**30**	**13**	**8**	**5**	**2**	**1**	**0.4**

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *FEOL—front end of line*
** *BEOL—back end of line*
† *Calculated as negative binomial yield model with a cluster factor of 2, using the microprocessor area from ORTC Table B1.*

DEFECT DETECTION

Technology requirements for defect detection technology change throughout the life cycle of a semiconductor process and its associated products. There are three generic phases of the semiconductor manufacturing—1) process research and development, 2) yield ramp, and 3) volume production.

Technology requirements are separated into unpatterned wafer inspection, patterned wafer inspection, and high aspect ratio inspection, as shown in Table 57. The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. The most stringent requirements come earlier in the process stages. The wafer backside requirements are not scaled with the critical dimension, but rather are based on lithography depth-of-focus considerations. The throughput improvement of ~300× for patterned wafer detection exhibits the most dramatic change when a semiconductor process moves from research and development, through the yield ramp, to volume production. The respective tools must be ready for use by the chip manufacturers just-in-time for each phase of the process development cycle. Early inspection tools are typically required up to four years before the first year of production. Tools that can accelerate the yield ramp must be characterized before the yield ramp occurs. Thus they must be available about 18 months before production begins. Tools that monitor yield excursions in volume production must be available in the first year of production, because volume production typically occurs within one year of the manufacturing release. Post chemical mechanical planarization (CMP) is considered part of patterned wafer inspection. The effects of the buried patterning in CMP wafer inspection make the challenges more like that of patterned wafer inspection than unpatterned for the purposes of this roadmap. High aspect ratio inspection is treated separately from patterned wafer inspection due to special sensitivity requirements described in the *Difficult Challenges* section.

Table 57 Defect Detection Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Patterned Wafer Scan Speed (cm^2/hr)							
Process research and development	300	300	300	300	300	300	300
Yield ramp	3000	3000	3000	3000	3000	3000	3000
Volume production	10000	10000	10000	10000	10000	10000	10000
Patterned Wafer Nuisance Defect Rate (%)							
Process research and development	20	20	20	20	20	20	20
Yield ramp	10	10	10	10	10	10	10
Volume production	5	5	5	5	5	5	5
High Aspect Ratio Feature Inspection, Via Residue, Equivalent Sensitivity (nm)							
Process research and development	83	59	50	43	33	23	17
Yield ramp	83	59	50	43	33	23	17
Volume production	83	59	50	43	33	23	17
Patterned Wafer Inspection, PSL spheres at 90% capture, Equivalent Sensitivity (nm)*							
Process research and development	83	59	50	43	33	23	17
Yield ramp	165	119	99	86	66	46	33
Volume production	250	180	150	130	100	70	50
Unpatterned Wafer Detection Tool							
Throughput (wfr/hr)	150	150	150	150	150	150	150
Nuisance defect rate (%)	5	5	5	5	5	5	5
Unpatterned, PSL spheres at 90% capture, Equivalent Sensitivity (nm)							
Wafer backside	200	200	200	200	100	100	100
Metal film	125	90	75	65	50	35	25
Nonmetal films	83	60	50	43	33	23	17
Bare Si	83	60	50	43	33	23	17
In Situ Particle Monitoring							
Sensitivity (nm) (@2:1 signal/noise ratio)	250	180	150	130	100	70	50
Automatic Defect Classification							
Resolution (nm)	125	90	75	65	50	35	25
Detectibility (% redetection)	95	97	98	99	99	99	99
Accuracy (% of expert classification)	85	90	90	95	95	95	95
Repeatability (%)	95	97	98	99	99	99	99
Reproducibility (COV%)	5	4	4	3	2	2	2
Speed—optical (sec/defect)	3	2	2	1	1	1	1
Speed—SEM (sec/defect)	20	10	10	5	5	5	5
Speed—SEM w/elemental (sec/defect)	35	25	20	15	10	10	10
Defect Review							
Resolution (nm)	125	90	75	65	50	35	25
Coord. accuracy @ max sensitivity (μm)	3	3	2	2	1	1	1

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *PSL—polystyrene latex*

DEFECT SOURCES AND MECHANISMS

To achieve the roadmap defect density, defect isolation on product chips must be accomplished more rapidly than is done now. Table 58 presents the technology requirements for defect sources and

mechanisms. Learning must proceed at an accelerated rate and the cycle time, from when a defect is detected on a representative device until it is isolated on a circuit, must be appreciably shortened. This will enable the failure analysis function to give timely feedback to manufacturing to find and eliminate the root cause of the problem and continue defect density improvements. To source defects more quickly, all data sources must be used to pinpoint the system or systems that cause the defect. An integrated suite of data analysis software tools, using validated algorithms, is needed to accomplish this. These software tools must be both modular and extensible to future factories and technologies.

Table 58 Defect Sources and Mechanisms Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Fault Isolation Complexity							
# transistors in microprocessor (10^6)	11	21	40	76	200	520	1400
# process steps	350	380	420	450	500	550	600
Fault isolation complexity factor (10^9)	3.8	8.0	17	34	100	290	640
Defect sourcing complexity trend	1×	2.1×	4.3×	8.9×	26×	74×	170×
Data Analysis for Rapid Sourcing							
Time required to source problems	days	days	days	hours	hours	hours	hours
Time required to recognize trends	weeks	days	days	hours	hours	hours	hours
Information sources for automatic data analysis	spatial analysis	time analysis	time analysis	merge	improve	improve	improve
Standardization of defect data output formats	extend	extend	extend	new	new	new	new
Standard architecture for data transmission/storage	proprietary architec-ture	develop standards	develop standards	adopt	apply	apply	apply
Fuse/integrate process and defect data from different tools	single inline tools	in/offline tools	in/offline tools	extend	extend	extend	extend
Feedback for automatic process control	manual	open-loop	open-loop	mixture	closed-loop	closed-loop	closed-loop

Solutions Exist *Solutions Being Pursued* *No Known Solution*

DEFECT PREVENTION AND ELIMINATION

Defect prevention and elimination requirements are categorized by manufacturing materials or environment, as shown in Table 59.

Wafer Environment Control—There is now consensus that as device geometries approach 180 nm and beyond, wafer isolation may prove to be an enabling technology. The percentage of process steps affected by nonparticulate or molecular contamination is expected to increase. Because of this trend, the ability of wafer isolation technology to facilitate factory automation, increasing use of tool minienvironments and closed carriers (pods) is needed. The wafer environment control (WEC) technology requirements also indicate target levels of ambient acids, bases, condensables, and metals for specific process steps. Other exposure times and sticking coefficients may be scaled linearly. The calculations do not account for localized differences in surface terminations, changes in the sticking coefficient over time, or chemical/kinetic interactions of analytes in the air or on the surface.

Process Critical Materials—Little understanding exists today regarding impurity specifications in novel materials such as sputter targets, plating solutions, CMP slurries, and chemical vapor deposition (CVD) precursors, and future focus on this is required. Particle levels per volume have been held constant at critical particle size. Assuming an $x^{-2.7}$ power law relationship, this means a cleanliness increase of approximately 2× per generation or ~80× from the 250 to the 50 nm technology node. Measurement of particles at the critical size is inferred, but monitoring of larger size particles is possible with requirements scaling according to the power law.

Ultrapure Water (UPW)—The technology requirements for ultrapure water stress the importance of low particle, silica, and ionics. The dissolved oxygen content needs to be controlled for rinsing after HF last cleans on bare silicon. Until tools operate in N_2 environment, control of oxygen below 1 ppb is unlikely to prove practical. Levels of F^- below 10 ppb may not be possible in PVDF piping. The industry will require that recycled water be equal to or better than single-pass water.

Liquid Chemicals—For process chemicals, pre-diffusion cleaning requirements drive the most aggressive impurity levels. These levels have been relaxed compared with the 1994 SIA Roadmap to correspond with the specification of surface levels of metallics (see *Surface Prep in Front End Processes section*). This evolution shows only a 10× improvement required over the next 15 years. Importantly, liquid particle counting technology is a critical challenge below 90 nm. For HF last or SC-1 last cleans, use of novel chemistry (e.g., complexants, pH adjustments) may be required to meet the surface preparation requirements.

Bulk / Specialty Gases—While major changes are not expected for bulk ambient gases such as nitrogen, oxygen, argon, and hydrogen, inline non-intrusive particle measurements at the critical size in these and specialty gases will be a significant challenge. Although current technology can be extended to meet the measurement requirements at point of use (POU) continuous particle monitoring in each specialty gas line would add substantial costs to factory infrastructure. For specialty gases the sensitivity to contamination may vary significantly by process. POU filters, and in some cases purifiers and generators, can be utilized to meet the most stringent requirements. Cost-effective rapid response detection of molecular impurities is required.

Novel Materials—Impurity specifications for novel materials used in processing will be increasingly important. Specifications for critical materials such as sputter targets, oxides, CMP slurries, low/high dielectric materials, and novel barrier and conductor metals (e.g., Cu, Ta) are required. Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications which meet technology requirements.

Design-to-Process Interactions—The need for standard test structures is critical in determining defect sources and mechanisms. Once the design process interactions are understood, device design ground rules may be established and communicated that decrease process sensitivity. Cycles of process sensitivity analysis and reduction will be critical to advancing device design and yield. Additionally, sensitivities of designs to various levels of random defects need to be considered in the design process.

Process-to-Process Interactions—Interactions that result in defect formation (e.g., thickness of photoresist and contact density can affect the level of residue inside a via/contact) between process steps may drive particular requirements to a tool or process upstream or downstream that are not necessarily germaine to that tool or process. Cluster tools and wet sinks are two examples of tools that must be carefully designed to ensure that their modules do not transfer any contaminants that degrade the performance of adjacent modules. To detect, to understand, and to eliminate unwanted process interactions, process monitoring will play a key role. The appropriate sensors and data must be available, along with an appropriate information management system to correlate process parameters to upstream/downstream parameters and yield and provide smart, intertool and intratool statistical process control (SPC).

Table 59 Defect Prevention and Elimination Technology Requirements

Year of First Product Shipment / *Technology Generation*	*1997* / *250 nm*	*1999* / *180 nm*	*2001* / *150 nm*	*2003* / *130 nm*	*2006* / *100 nm*	*2009* / *70 nm*	*2012* / *50 nm*
Wafer Environment Control							
Critical particle size (nm) (A)	125	90	75	65	50	35	25
Particles ≥ crit size ($/m^3$) (B)	27	12	8	5	2	1	1
Airborne Molecular Contaminants (pptM) (C)							
Litho—Bases (as amine)	1000	1000	1000	1000	1000	1000	1000
Gate—Metals (as Cu, $E=2 \times 10^{-5}$)	0.7	0.3	0.3	0.2	0.1	0.07	<0.07
Gate—Organics (as MW=250, $E=1 \times 10^{-3}$)	300	200	200	100	100	70	50
Sal/Cont—Acids (as Cl^-, $E=1 \times 10^{-5}$)	10	10	10	10	10	10	10
Sal/Cont—Bases (as Na^+, $E=1 \times 10^{-6}$)	80	40	30	20	10	4	<4
Process Critical Materials							
Critical Particle Size (nm) (B)	125	90	75	65	50	35	25
Ultrapure Water							
Total oxidizable carbon (ppb)	< 10	< 7	< 5	< 4	< 3	< 2	< 1
Bacteria (CFU/ liter)	< 1	< 1	< 1	< 1	< 1	< 1	< 1
Silica (ppb)	0.1	0.05	0.05	0.01	0.01	0.01	0.01
Dissolved oxygen (ppb)	10	10	1–10	1	1	1	1
Particles ≥ critical size (/ml)	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2
Critical cation, anion, metals (ppt, each)	< 25	< 20	< 15	< 10	< 5	< 1	< 1
Liquid Chemicals (D)							
Particles ≥ crit size (/ml)	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5
HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	< 500	< 250	< 200	< 150	< 100	< 50	< 50
Other metals (ppt, each)	< 1000	< 500	< 400	< 300	< 200	< 100	< 100
HF-only TOC* (ppb)	< 90	< 60	< 40	< 30	< 20	< 15	< 10
HCl, H_2SO_4: All impurities (ppt)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
BEOL Solvents, Strippers K, Li, Na (ppt, each)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
Bulk Ambient Gases							
N_2, O_2, Ar, H_2: H_2O,O_2,CO_2,CH_4 (ppt,each)	100–1000	100–1000	< 100	< 100	< 100	< 100	< 100
Particles ≥ critical size (liter)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
Specialty Gases							
POU Particles ≥ crit size (/liter)	2	2	2	2	2	2	2
Corrosives—metal etchants							
O_2 (ppbv)	< 500	100–500	< 100	< 100	50–100	< 50	< 50
H_2O (ppbv)	500–1000	< 500	< 500	100–500	< 100	50–100	< 50
Inerts—Oxide/PR Etchants/Strippers							
O_2 (ppbv)	1000–5000	< 1000	500–1000	500–1000	< 500	100–500	< 100
H_2O (ppbv)	< 1000	500–1000	< 500	< 500	100–500	< 100	< 100
SiHx(Cly)							
Total metallics (pptwt)	< 500	100–500	< 100	< 100	50–100	< 50	< 50

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *TOC—total oxidizable carbon*

Table 59 Defect Prevention and Elimination Technology Requirements (continued)

A. *Critical particle size is based on 1/2 design rule. All defect densities are 'normalized' to critical particle size. Critical particle size does not necessarily mean 'killer.'*

B. *Airborne particle requirements are based on deposition velocity of 0.01 cm/sec. resulting in 1 particle/m^2/hr. for a ambient concentration of 3 particles/m^3. Values are back-calculated assuming: the 'wafer handling' defect target, 300 process steps (increasing by 10 per generation), and a wafer exposure time of 1000 hours. As an example, the 250 nm requirement is calculated as: (30 particles/m^2/step) × (300 steps)/(1000 hrs.) × [(3 particles/m^3)/(1 particle/m^2/hr.)] = 27 particles/m^3.*

C. *Ion indicated is basis for calculation. Exposure time is 60 min. with starting surface concentration of zero. Basis for lithography is defined by lithography roadmap. Gate metals and organics scale as surface preparation roadmap metallics and organics respectively. Salicidation and contact acids and bases scale as surface preparation BEOL anions and metal respectively. All airborne molecular contaminants calculated as S=E*(N*V/4); where S is the arrival rate (molecules/cm^2/sec), E is the sticking coefficient (between 0 and 1), N is the concentration in the air (molecules/cm^3), and V is the average thermal velocity (cm/sec).*

D. *Particle targets apply at POU, not incoming chemical. Point-of-tool connection chemical metallic targets are based on Epi starting material, sub-ppb contribution from bulk distribution system, 1:1:5 standard clean 1 (SC-1) and elevated temperature 1:1:5 standard clean 2 (SC-2) final clean step. 'HF last' or 'APM last' cleans would require ~10× and ~100× improved purity HF (mostly Cu) and APM chemicals respectively*

POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

The validation information provided by SEMATECH has significantly improved the quality of the defect budgets. This validation effort must continue with each new revision of the roadmap. Researching into better yield modeling techniques is required to address future modeling challenges. The increasing dominance of nonvisual defects will further complicate yield modeling and defect budgeting. Thus defect models will need to better consider electrical characterization information, and reduce emphasis on visual analysis. This will require research into new characterization devices and methods and a better understanding of systematic and parametric impacts on device yield. Interconnect process layers are a particular challenge and have been so identified in the technology requirements. Some issues include modeling the yield impacts of ultra-thin film integrity, increased process complexity, and interconnect speed and transmission characteristics. This research is complicated by the lack of state-of-the-art semiconductor processing capabilities in universities and other research sources.

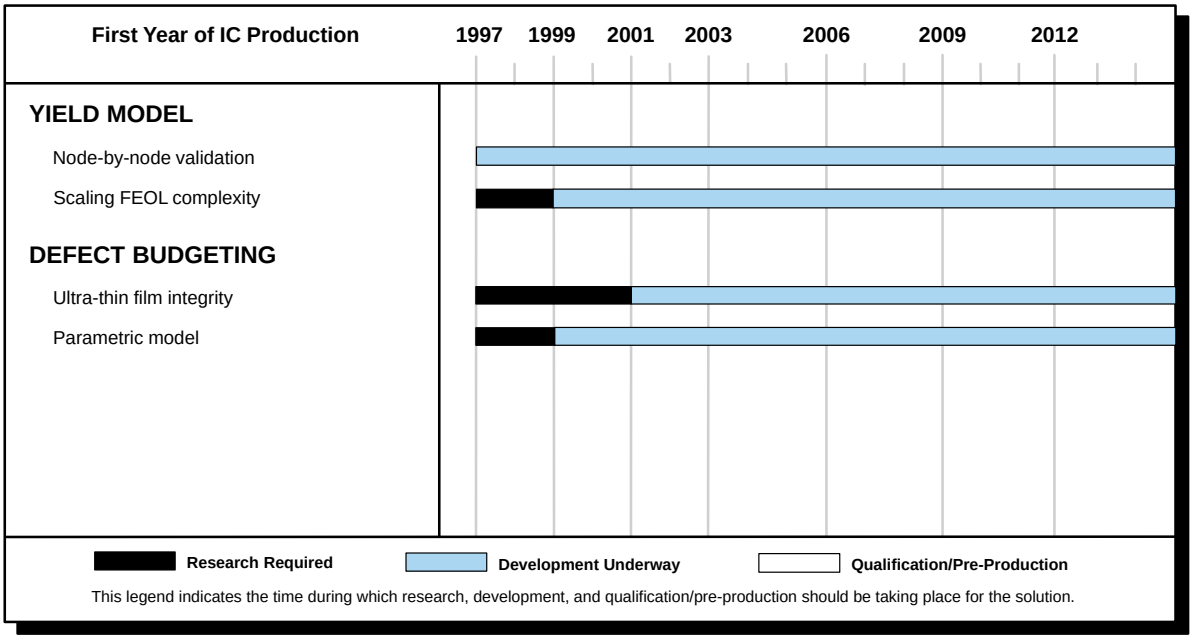


Figure 43 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION

To meet the technology requirements for advanced defect detection tools, a considerable amount of research and development is necessary. Figure 44 indicates the known set of potential solutions for defect detection. For increased sensitivity on patterned wafer inspection systems, light scattering and optical imaging solutions will continue to address needs in the yield ramp and volume production yield phases for the next 2–3 technology nodes. Advancements associated with shorter wavelength lasers and novel detection strategies (e.g., multiple detectors and/or adjustable angles) are needed to meet the high aspect ratio defect sensitivity for yield and defect budgets requirements for all yield phases. Novel solutions such as holography, E-beam, or X-ray may also bridge the sensitivity gap. Regardless of detection strategy, it is expected that major breakthroughs will be necessary to achieve the required throughputs at roadmap sensitivities (especially throughputs for yield ramp and volume production). Software development will also play a key role in detection technology for both sensitivity by algorithm development for background noise reduction and throughput by extremely fast pixel-to-pixel and image-to-image data processing and comparison. SEM-based systems will provide sensitivity capability in the process development yield phase, but will require major breakthroughs in speed to be usable in other yield phases. These solutions must also comprehend the need for greater amounts of defect-related data, such as composition, shape, etc., and the need for greater intelligence and rapid decision making. Both inline and offline automated defect classification, spatial defect signature analysis, adaptive sampling, yield impact assessment, and other artificial intelligence will play a key role in reducing time to decisions and product at risk. Software development will be key to these capabilities. Defect detection must evolve closer to the defect source and as such, development to integrate defect detection into process equipment must be accelerated. Process tools that accommodate on-wafer defect detection and characterized *in situ* process control sensors are expected to be necessary for cost-effective, high-volume, large wafer (≥ 300 mm) manufacturing.

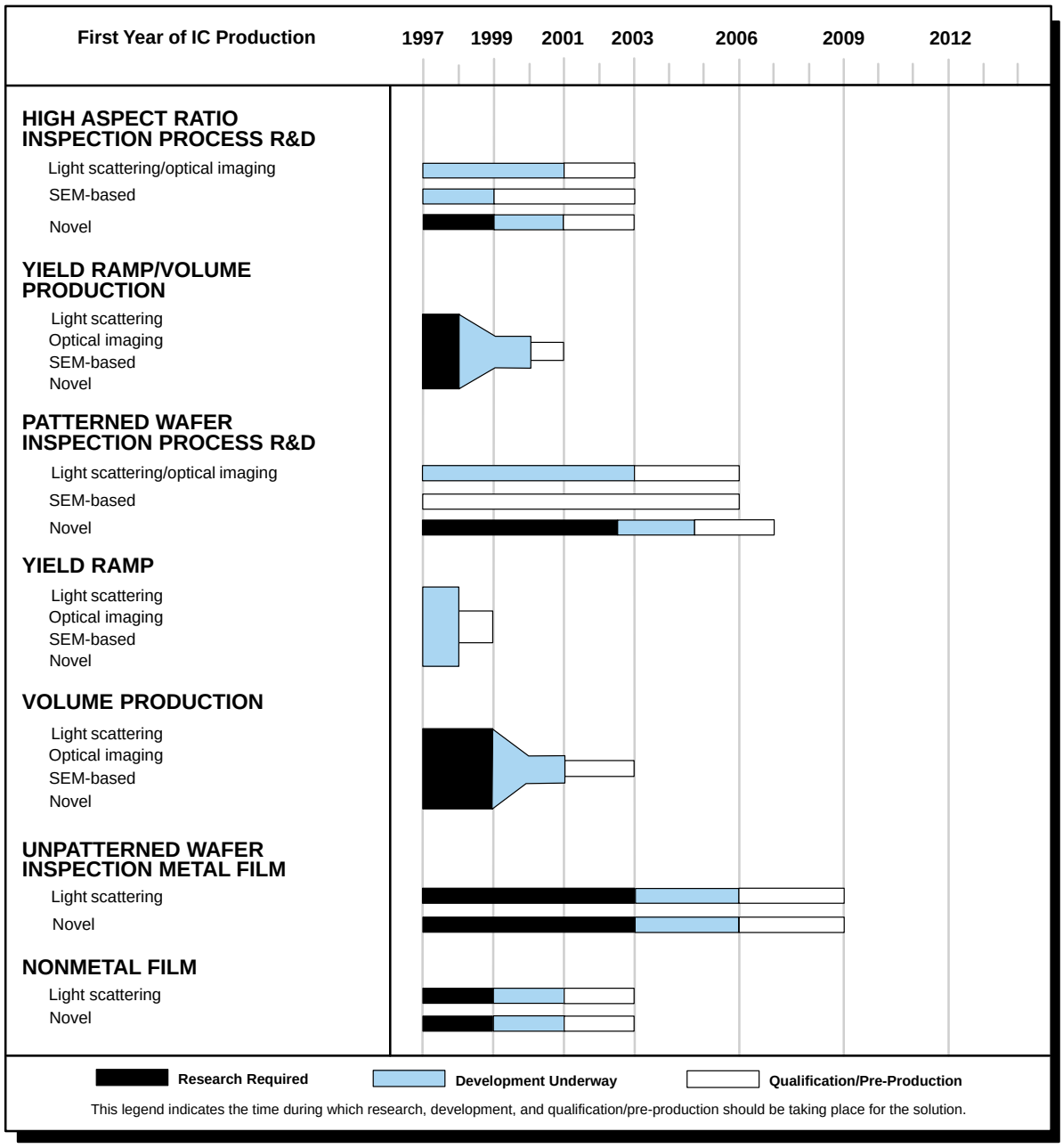


Figure 44 Defect Detection Potential Solutions

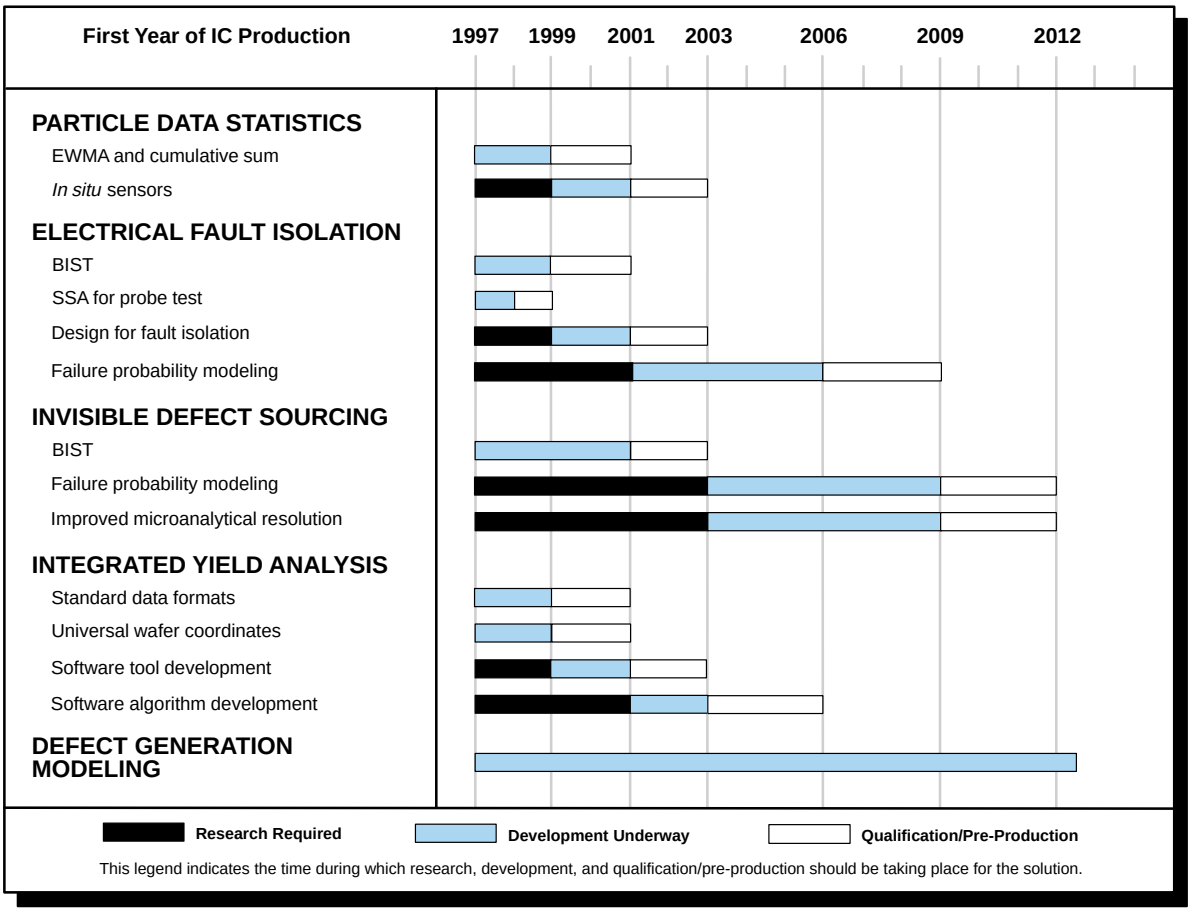
DEFECT SOURCES AND MECHANISMS

Statistical Methods for Controlling PWP—In situ particle sensors may be the only way to provide the resolution and timeliness necessary to detect equipment and process deviations. In the intermediate term, the use of exponentially weighted moving average (EWMA) and cumulative sum techniques can provide more accurate results than traditional Shewhart methodology for PWP data. EWMA and cumulative sum techniques are more robust to violations of the underlying assumption of normality; however, sampling frequency must be increased to achieve the same timeliness in response that Shewhart charts typically provide when data is continuous and normally distributed. All potential statistical solutions will require tradeoffs to be made between timeliness of detecting a shift and the frequency of false alarms.

Fault Isolation—Presently memory array test chips and memory arrays within microprocessors are used to quickly isolate faults and is likely to continue for non-arrayed devices. Future products must be designed so that the test process can isolate failures. Built in self test (BIST) is one method that can aid in defect isolation. The BIST failure pattern must map to a physical location on a circuit. Other test programs are needed to save failure pattern information so that it can be analyzed based on pre-determined (modeled) failure mode probabilities. This will allow yield engineers to more quickly and precisely determine the location and causes for circuit failures.

Invisible Defects—Saving more parametric data as measured on circuit testers will aid in sourcing "invisible defects." This will allow for correlation to process data, through a variety of techniques, including Spatial Signature Analysis. Modeling the probabilities of factors that can lead to "invisible defects" can also reduce the time it takes to source their causes. BIST techniques should be developed to identify race conditions and other failure modes that are a function of parametric variation or mis-match. Also, development of failure analysis that can extend the range of detectable defects down to the atomic level will also reduce the level of "invisible defects."

Integrated Yield Analysis Capabilities—Solutions to this challenge lie in the ability to develop "smart" software tools that quickly and automatically access multiple databases and establish correlations between data of different types. Some data sources will be time-based, others will be wafer-based. Still others will be chip-based. On-wafer coordinates must be unified and data formats must be standard-ized. Automated data reduction algorithms to source defects from multiple data sources must be developed to reduce defect sourcing time. Spatial and timed-based signature analysis, and multivariate statistical methods are examples of these analysis tools.



SSA—spatial signal analysis

Figure 45 Defect Sources and Mechanisms Potential Solutions

DEFECT PREVENTION AND ELIMINATION

Process Critical Materials—Figure 46 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities. Inline trace impurity analytical technology for process critical materials is needed to better understand purity levels at the POU. Ultrapure water particle levels are easily achieved with existing design and filtration practice and verified with available particle metrology. However, these systems are not sterile systems and analytical technology is needed to characterize ultra-trace levels of bacteria (both viable and nonviable). Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water. Demonstration of the effectiveness and efficiency of particle filters in specialty gases is needed to increase the confidence that the filters are performing adequately without continuous monitoring. The requirements to measure particles at POU for specialty gases below 100 nm can be met by the development of an inline condensation nucleus counter (CNC) or novel techniques compatible with oxidizers, corrosives, and flammable and toxic gases.

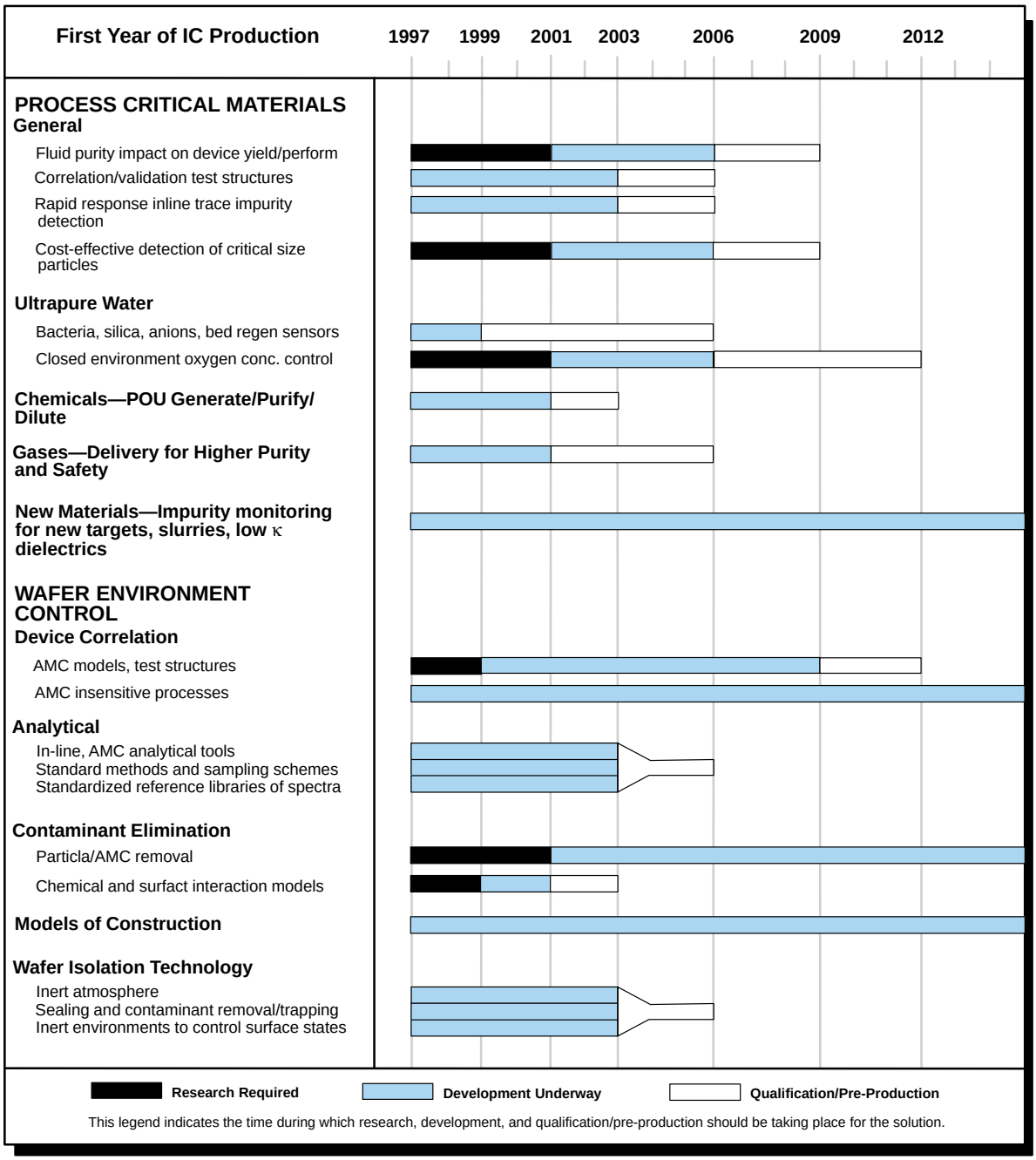


Figure 46 Defect Prevention and Elimination Potential Solutions

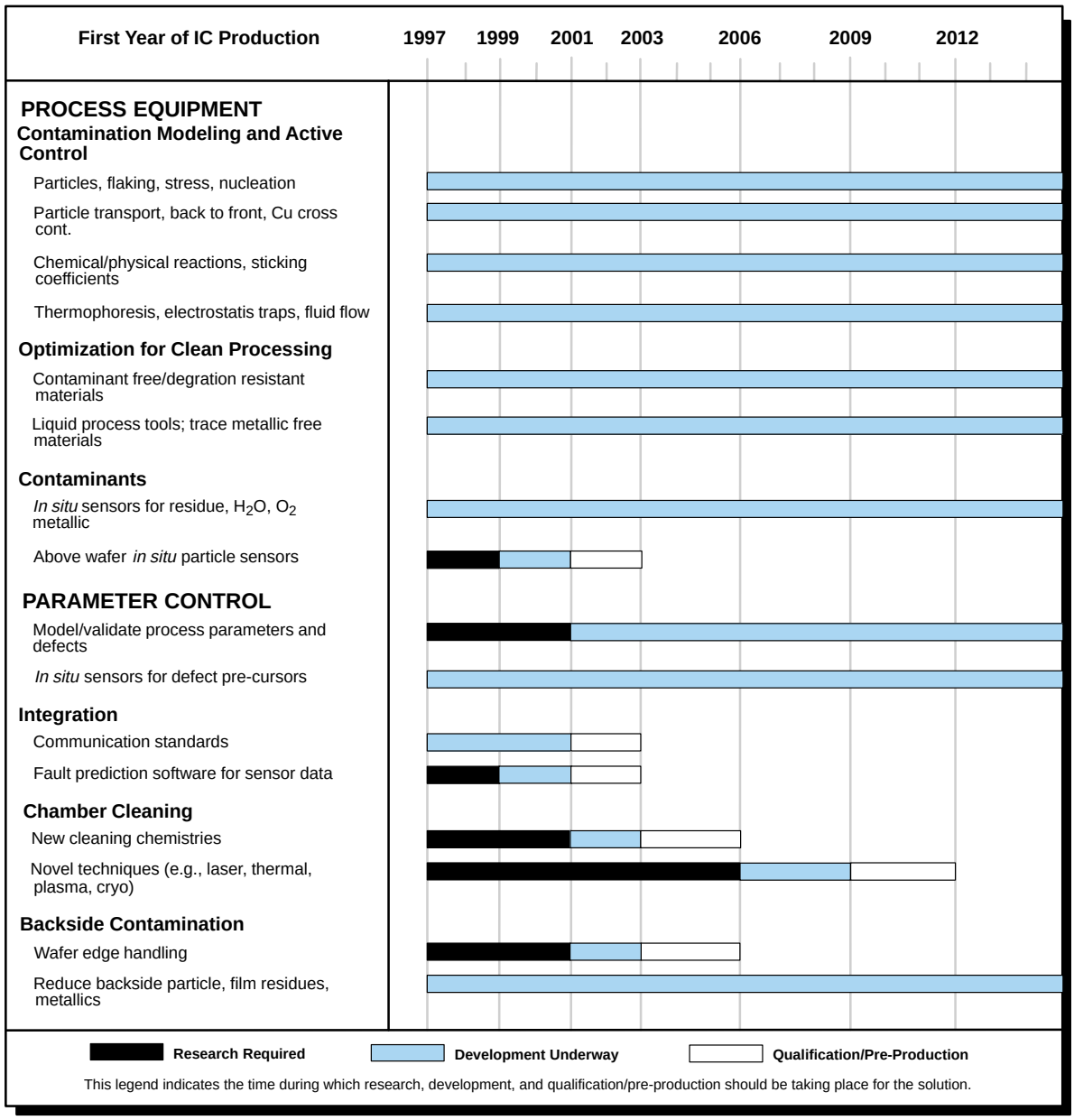


Figure 46 Defect Prevention and Elimination Potential Solutions (Continued)

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 35 years and actually enable cost-effective high volume manufacturing for 130–100 nm devices. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other nonvisual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/ depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature

management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

Wafer Environment Control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Availability of affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pregate and precontact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum loadlock tools, thereby decreasing contamination and loadlock pumpdown times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink endstations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and nonabsorbing materials development are key to effective wafer isolation deployment.

METROLOGY

Metrology is essential to the development and improvement of new processes and tools for future technology generations. It drives acceleration of yield ramping in pilot lines and factory start-ups and improvement of yield in mature factories. Metrology must migrate from offline to inline and *in situ* to achieve Roadmap goals. However, the implementation of real time, *in situ* sensor-based process control will probably occur over several technology generations. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning. In addition, over the next ten years, micro-electro mechanical systems (MEMS) are expected to evolve into new types of sensors for *in situ* metrology.

SCOPE

The metrology topics covered in the 1997 Roadmap are *Microscopy, Critical Dimension (CD) and Overlay, Film Thickness and Profile, Materials and Contamination Analysis, Dopant Profile, In situ Sensors for Process Control, Reference Materials,* and *Correlation of Physical and Electrical Measurements.* CD and overlay metrology is included in the *Lithography* section, film thickness metrology is discussed in both *Front End Processes* and *Interconnect* sections, while dopant profile metrology is found in the *Materials and Contamination Characterization* part of this section and in the *Front End Processes* and *Process Integration, Devices, & Structures* sections. Sensor-based process control is included in the *Factory Integration* section, as well as discussed in this Metrology section.

National Institute of Standards and Technology (NIST), Semiconductor Research Corporation (SRC), SEMATECH, American Society for Testing and Materials (ASTM), Semiconductor Equipment and Materials International (SEMI), metrology tool suppliers, and the national laboratory and university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. The precision to tolerance (P/T) metric for evaluation of automated measurement capability for use in statistical process control is accepted. This metric ratios the measurement variation (precision) of the metrology tool to the specified limits of the process. It is possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. Therefore, there is a need for a metric that describes the resolution capability of metrology tools for use in statistical process control. Since the type of resolution (e.g., thickness requires spatial resolution, levels of metallic on the surface require resolution of atomic percent differences, etc.) depends on the process, topic-specific metrics are required. Another metric for establishing the ability of a metrology tool to distinguish process variability from metrology tool variability also needs to receive more emphasis. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio.

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements for metrology. As discussed in the *Factory Integration* section, the need for a shorter ramp-up time for pilot lines means that characterization of tools and processes prior to pilot line must increase. However, as the process matures, the need for all types of metrology should decrease. As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data.

WAFER SIZE IMPACT

Metrology capability for larger diameter wafers precedes pilot line activities by three to five years. Process tool suppliers must build prototype tools and develop processes long before delivery of the first tools to the pilot line. Therefore, wafer suppliers and process tool manufacturers have specific large wafer metrology tool requirements several years prior to integrated circuit pilot line start-up. The present strategy for the IC industry indicates that the need for metrology tools for future generations will cover a mixture of wafer sizes (200, 300, and 450 mm). The first shipment of chips from a 300 mm fab is expected by 2001 and from a 450 mm wafer fab by 2010.

INFRASTRUCTURE NEEDS

A healthy industry infrastructure is required if suppliers are going to be able to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS are going to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities such as large diameter wafer/process tool development prohibitive. The initial sales of metrology tools is to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers does not occur until several years later. The present infrastructure cannot support this delay.

DIFFICULT CHALLENGES

Metrology needs by 2003 may be based on new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect materials will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 60 presents the ten major challenges for metrology.

Table 60 Metrology Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Robust sensors, process controllers, and data management that allow integration of add-on sensors	Standards for process controllers and data management must be agreed upon.
Impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Existing FTIR* method must be modified for heavily doped silicon wafers.
Measurement of the frequency-dependent dielectric constant of low κ interconnect materials at 5× to 10× base frequency.	Using existing equipment and procedures, test structures need to be developed and applied to low κ interconnect materials that account for clock harmonics, skin effects, and cross-talk
Control of new processes such as Damascene and copper metalization	High aspect ratio of future technology generations challenges all metrology methods. New process control needs are not yet established.
Reference materials and standard methods for gate dielectrics, thin films, and other process needs	Optical measurement of gate dielectric averages over too large an area and needs to characterize interfacial layers.

* *FTIR—Fourier transform infrared spectroscopy*

Table 60 Metrology Difficult Challenges

FIVE DIFFICULT CHALLENGES < 100 nm / BEFORE 2006	SUMMARY OF ISSUES
Nondestructive, manufacturing capable microscopy for critical dimension measurement, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape.
Standard electrical test method for reliability of ultra-thin silicon dioxide and new gate dielectric materials	The wearout mechanism for ultra-thin gate dielectrics is thought to be different from that observed for silicon dioxide at the thickness used in the 250 nm technology generation.
Metrology tools for 450 mm wafers	Infrastructure can not support development prior to volume need for new tools. Larger vacuum chambers for some analysis tools will require significant increases in total measurement time.
3-D dopant profiling	The dopant concentration levels result in large average spacings between dopant atoms. There is no known solution having required spatial resolution.
Manufacturing capable, physical inline metrology for transistor processes that provides SPC** required for electrical properties of transistor	Presently, the combined physical metrology for gate dielectric, CD, and dopant dose and profile does not give the required SPC of electrical properties.

** *SPC—statistical process control*

METROLOGY TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

Measurement requirements for metrology tools are listed in Table 61. The microscopy resolution refers to the ability of a CD measurement tool to distinguish between lines that differ in width. The spatial resolution requirements for 2- and 3-dimensional (2-D and 3-D) dopant profiling are based on the requirements of Modeling & Simulation. Meeting 2-D dopant profiling requirements will be difficult, and methods with slightly less spatial resolution may provide useful information. The precision requirement for dopant concentration metrology refers to integrated dose. Measurement accuracy for all metrology requires reference materials that have the required accuracy.

Table 61 Metrology Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Inline, nondestructive microscopy resolution (CD precision is different from resolution) (nm)	2	1.4	1.2	1	0.7	0.5	0.4
Particle analysis size (on patterned wafers) (nm)	75	60	50	45	35	25	15
Surface detection limits (Al, Ti, Zn)/ (Ni, Fe, Cu, Na, Ca) (atoms/cm^2)	5×10^9 5×10^8	2.5×10^9 4×10^8	2×10^9 3×10^8	1.5×10^9 2×10^8	1×10^9 1×10^8	5×10^8 $\leq 10^8$	$\leq 5 \times 10^8$ $\leq 10^8$
Composition and thickness gate dielectric (equivalent film thickness ± 3σ control) (nm)	4–5 ± 4%	3–4 ± 4%	2–3 ± 4%	2–3 ± 4-6%	1.5–2 ± 4-8 %	< 1.5 ± 4-8 %	< 1 ± 4-8 %
2- and 3-D dopant profile spatial resolution (nm)	5	3	3	2	1.5	1	0.8-0.6
Dopant concentration precision (across concentration range)*	5%	5%	4%	4%	3%	2%	2%
Barrier layer film thickness measurement capability and profile characterization on patterned wafers (thickness /line width) (nm)	50/250	25/180	25/180	20/130	15/100	10/70	5/50

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *Accuracy for dopant profiling depends upon use of accurate reference materials (see Reference Materials Discussion).*

MICROSCOPY

Microscopy is used in most of the core technology processes. Typically, microscopy is done using far-field light, electron beam, and scanned probe methods. Inline microscopy applications include CD and overlay measurement along with defect/particle detection, review, and auto-classification.

While offline microscopy can use destructive sample preparation methods to enhance imaging of small features, inline microscopy will have difficulty providing nondestructive, high throughput capability at the required resolution.

Each technology has its own limitations. State of the art, far-field optical microscopy is limited by the wavelength and diffraction of light. UV sources and near-field optical microscopy are being developed to overcome these limitations. Although inline CD measurement is performed with low voltage CD–SEM, both scanning electron microscopy (SEM) and atomic force microscopy (AFM) technology are considered too slow for the throughput needs of defect detection. High speed scanning has been demonstrated with arrayed scanning probe microscopy (SPM), but issues associated with stylus uniformity and the characterization and wear need to be addressed. This technique is most likely to be useful on surfaces with relatively gentle surface slopes. Arrayed SEM has been proposed as a method of improving SEM throughput. Light scattering for defect detection may require new shorter wavelength sources for high throughput applications. New inline SEM technology is required for overcoming image degradation due to the interaction of the electron beam with sample surface charging and contamination while maintaining adequate resolution.

Determination of 3-D sidewall shape for sub-100 nm contact/vias, transistor gates, interconnect lines, or Damascene trenches will require considerable advances in existing microscopy methods. Electron and optical holography and electron interferometry have been proposed as solutions for microscopy applications.

Scanning electron microscopy continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 180 nm technology generation, and roadblocks exist below the 100 nm generation.

There is a need to improve the modeling of the electron beam/sample interaction and the instrument electronics. Sample damage during both CD and defect review arises from two mechanisms—direct damage to the sample and dissipation of built-up charge in gate structures. A better understanding of the relationship between the physical object and the waveform analyzed inside the instrument is expected to improve CD measurement. Ultra-low voltage electron beams (< 100 eV) have been proposed as a method of overcoming sample charging and surface contamination issues.

Scanning probe microscopy is being used to calibrate SEM-based CD measurements. This overcomes the differences in response between different materials when CD is done at gate level versus metal levels. Materials properties may limit probe technology when it is applied to via and contact inspection below the 100 nm technology generation. New developments such as carbon nanotube probe tips need to be investigated.

Arrayed SPM and SEM Operation of two probe tips at very high scan speeds (1 cm/sec) was demonstrated in 1996. Operational conditions limit this embodiment of this development presently to characterization of surface planarity. This technology should be pursued both in expansion of the size of the array and in operational modes. Operation of a single micro-SEM has been demonstrated and arrayed formats proposed. Research is needed into the limits of electrostatic and magnetic lens designs when applied to the different operating conditions imposed by CD, defect review, and defect characterization.

Confocal and ultraviolet microscopy are beginning to be applied to detection and characterization. Light-scattering-based defect detection may be extended to meet the needs of the 100 nm technology

generation. Issues with the limitations of image data analysis for defect detection will continue to be critical as information content increases.

SENSOR-BASED METROLOGY FOR INTEGRATED MANUFACTURING

Given the continually increasing process requirements for future devices and structures, coupled with the equipment reliability, cost, and uptime requirements for 200–450 mm wafers, semiconductor manufacturing is slowly moving from fixed process recipe, open-loop control to closed-loop control via sensor-driven model-based integrated manufacturing (SDMBIM). One key pacing item is the transition away from offline metrology that has been the mainstay of semiconductor manufacturing. Currently, metrology is shifting towards *in situ* sensors, as these can provide in-time data for active process control and the elimination of wafer misprocessing. For 200 mm (and even more for the 300 and 450 mm wafers), misprocessing is becoming prohibitively expensive. SDMBIM will clearly be the cost-effective and necessary paradigm for both semiconductor manufacturing and back end assembly and test. Sensors also provide reductions in process chemical consumption, thus generating a positive environmental impact.

To enable this mode of operation, key sensors are required for critical equipment, process, and wafer state parameters. It is essential that these sensors have excellent stability, reliability, reproducibility, and ease of use to provide high quality data with the statistical significance needed to support integrated manufacturing. Although significant progress can be made with existing sensor technology, new sensors and computer integrated manufacturing (CIM) components still need to be developed. Potential solutions for these needs are summarized in Figure 47.

Achieving such solutions requires a team effort among all development partners. These are:

- The sensor suppliers (to develop smart sensors and the computational algorithms to turn the sensor data into useful information)
- The process tool suppliers (to support the physical integration and associated data management of these sensors)
- The user (to implement these tools in manufacturing)
- The local CIM system (to provide the infrastructure, and the appropriate feed-forward and feed-back capabilities from other processes in the flow)

Since many process state sensors useful for *in situ* metrology already exist, the emphasis needs to be on the integration of these sensors into commercial process tools. The integration of sensors into process tools and the development of the CIM system are shown in Figure 47 as continuing activities, since a gradual evolution of these items is expected.

Some of these key sensors are envisioned to be a new generation of sensors and micro-instruments built on MEMS technology and developments in optical metrology. In addition, greater synergy must be developed between the areas of sensing, metrology, and control. A new generation of equipment controllers is also needed to take advantage of smart sensors that are bus organized, digitally compensated, and self-testing. A generic open architecture is needed to allow common hardware to be used across a wide range of process tools, with each tool system populated by the sensors needed for that particular process. Standards for intra-tool, sensor-controller communication are essential and will facilitate closed-loop tool level control.

Besides the metrology technical requirements, full implementation of SDMBIM will require a continuing litany of well-documented success stories. Although this methodology has already demonstrated operational benefits (e.g., small-batch, fast-ramp furnaces, and rapid thermal processes [RTP]) by keeping these processes centered on target, there still is a reluctance to commit fully to this mode of operation. The barrier to widespread implementation of *in situ* metrology is the large overhead expense (cost, time, reliability) including tool modifications, sensor integration, the factory CIM system, and changes in operational methods. However, within the time frame covered in this Roadmap, the

manufacturing of 200–450 mm wafers will tilt the balance of *in situ* metrology cost versus wafer value clearly towards the latter. It is acknowledged that implementation of *in situ* metrology will be driven by reducing pilot wafer use while simultaneously increasing process capability. Another driving force is the set of critical requirements that can only be solved by *in situ* metrology.

For > 100 nm technology generations, the strategic need is to integrate the available process or wafer state sensors, the process tools, and the CIM systems into a manufacturing methodology that benefits fab operation through fault detection, classification, and prognosis or model-based process control. At this time, a few selected processes have been configured for wafer-to-wafer sensor-based metrology; the immediate challenge is to overcome barriers to the deployment of these methods across the entire process flow.

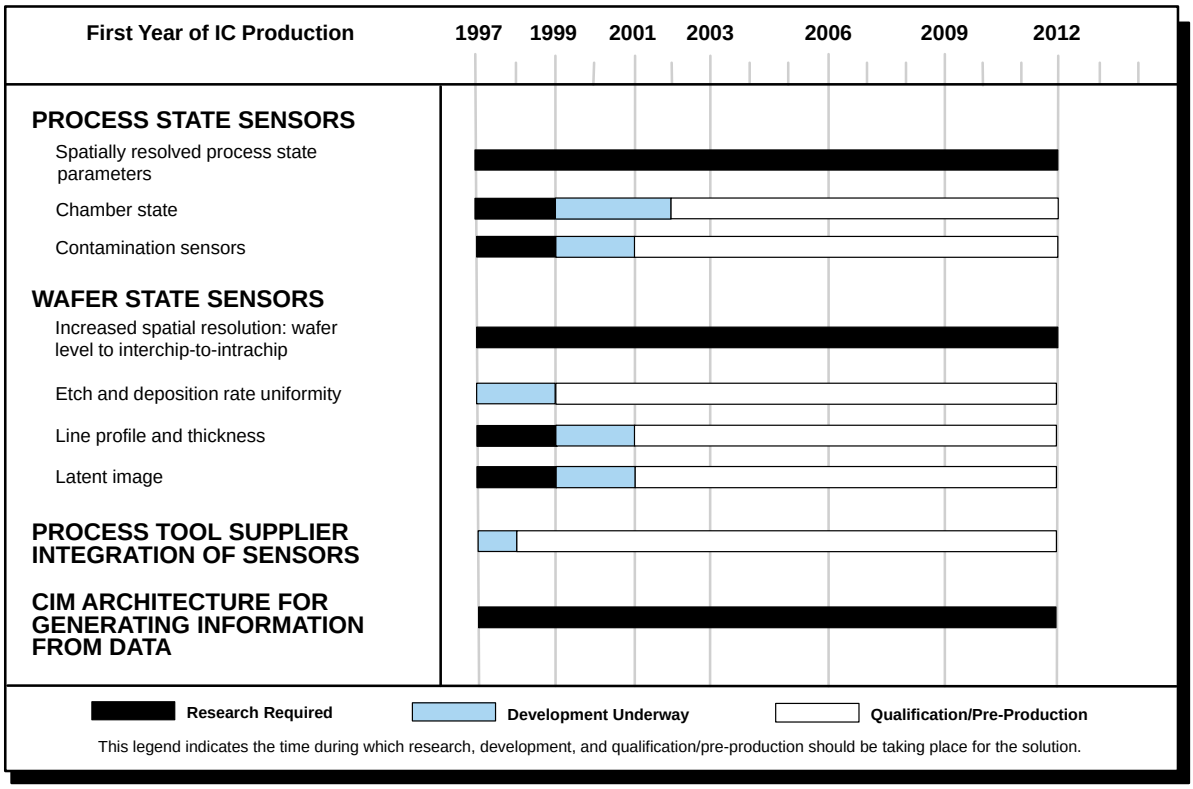


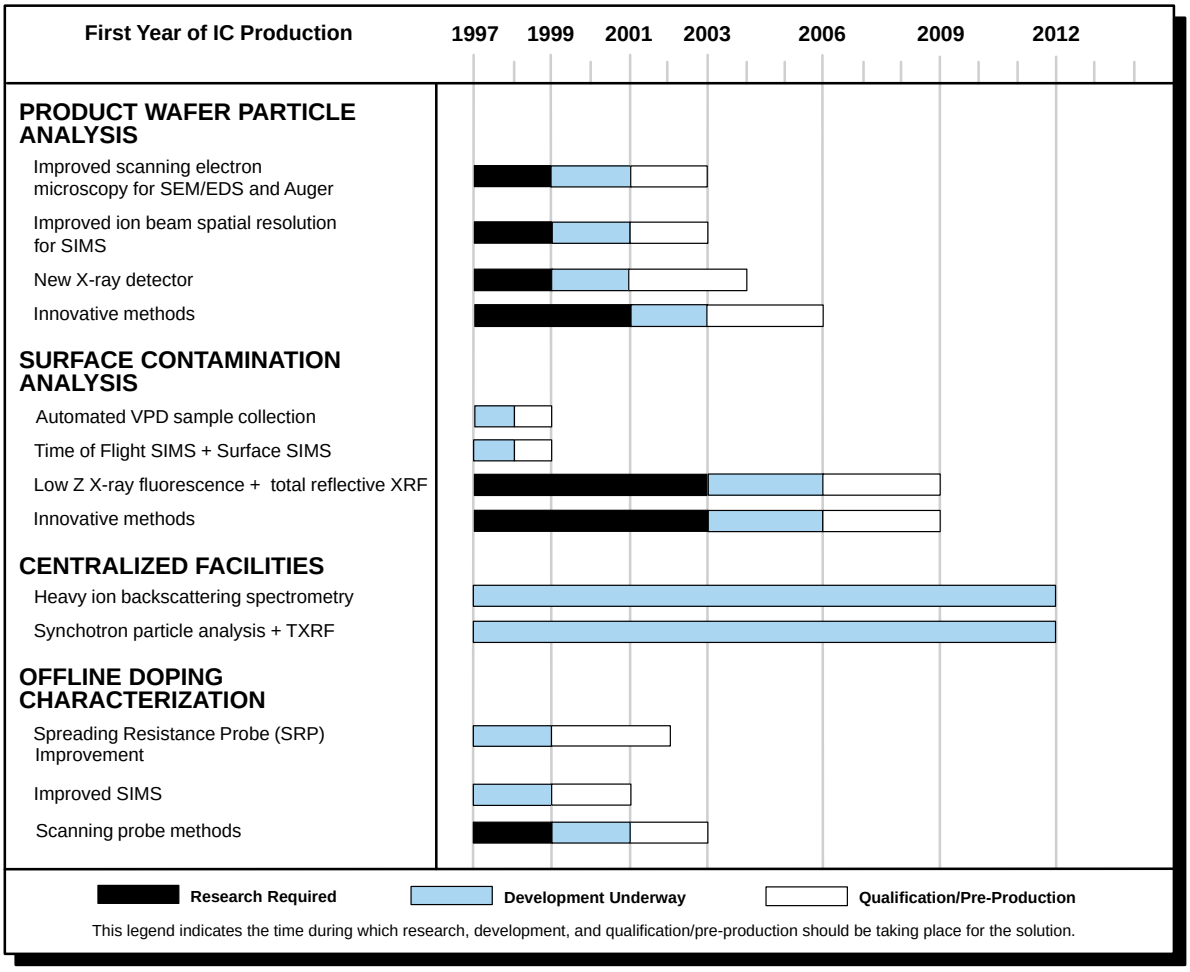
Figure 47 Sensor-based Metrology for Integrated Manufacturing Potential Solutions

Manufacturing sub-100 nm devices will require the availability of robust *in situ* equipment, process, and wafer-state sensors in process tools. These sensors must have adequate repeatability, reproducibility, and calibration capability to provide the necessary real time information for fault detection and process control. To achieve this, R&D organizations need to continue the development of increasingly faster data acquisition and computational algorithms for converting sensor data into useful information that enables real time fault detection and control. This includes a requirement for models to correlate the equipment or process state sensor signals to some performance metric (e.g., wafer state parameter, mean time between failure [MTBF], yield, and throughput). The process tool suppliers will need to own the controller, so that the tool can generate its own process based on relevant feed-forward and feedback information from the CIM system. Also, the process tools must accommodate real time feedback and control of their setpoint parameters to control a set of wafer properties to a target value.

MATERIALS AND CONTAMINATION CHARACTERIZATION

Crosscutting metrology needs for next generation devices also include analysis of particulate, metallic, and organic contamination, offline dopant characterization, and centralized analytical facilities for research and development. Potential solutions for these needs are shown in Figure 48**.** Heavy ion backscattering spectrometry (HIBS) used to calibrate reference materials for surface metallic contamination is an example of a method appropriate for a centralized facility.

Existing analysis methods for organic surface contamination, such as ion mobility mass spectrometry; thermal desorption gas chromatography/mass spectrometry; surface secondary ion mass spectrometry (SIMS) and time of flight SIMS (ToF–SIMS); and X-ray photoelectron spectroscopy are capable of qualitative (and in most cases quantitative) analysis of the specified control levels of 10^{14} to 10^{13} carbon atoms/cm^2 on silicon. The existing nondestructive methods for measuring metallic surface contamination, such as total reflection X-ray fluorescence (TXRF) analysis, have detection limits for Fe, Ni, Cu, and Na close to the required control levels specified for 180 nm design rule IC manufacturing. Statistical process control at the specified detection limits usually requires the measurement variability to be one tenth the control limit. Potential solutions for achieving the requisite particle and defect analysis on patterned wafer samples, surface contamination, and offline dopant profile and dose are summarized in Figure 48. Doping technology and technology computer-aided design (TCAD) process simulation require improved one, two, and three dimensional dopant profiling to address modeling for transient enhanced diffusion effects and process control for ultra-shallow junctions.



VPD—vapor phase decomposition

Figure 48 Materials and Contamination Characterization Potential Solutions

REFERENCE MATERIALS

Reference materials are physical objects with one or more well established properties used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar tools at different locations (internally or externally), or between model and experiment. Reference materials can be obtained from a variety of sources and come in a variety of forms and grades. Depending on the source, they may be called certified reference materials (CRM), consensus reference materials, NIST Traceable Reference Materials (NTRM®), or Standard Reference Materials (SRM®).

NIST has maintained its position as one of the leading internationally acceptable national authorities of measurement science in the semiconductor industry. NIST has also recognized the difficulty of keeping pace with the IC industry through the traditional method on need identification, instrumentation and technique development, and the development of SRMs. There are several approaches that allow the industry to supplement NIST's ability to supply reference materials. Commercial suppliers can submit calibration artifacts to a rigorous measurement program at NIST for the purpose of developing a NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark. A second approach, which has been growing in application is the accreditation of commercial laboratories by NIST through the National Voluntary Laboratory Accreditation Program. A third approach is the development of consensus reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM.

There are several technical requirements related to reference materials and certification, as follows:

- Reference materials must have properties that remain stable during use; variations in the material properties must be smaller than the calibration uncertainty.
- Reference materials may be difficult to manufacture with the desired attributes; frequently it is necessary to use specialized manufacturing techniques in short runs to obtain the samples to be measured and certified.
- Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology no current method of measurement is adequate for the purpose. When the basic measurement process has not been selected or proven, reference materials cannot be produced.
- Uncertainties in the certified value of the reference material must be less than 1/4 of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.
- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy better than 1/4 of the requirement; accuracy includes both bias and variability considerations.
- Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.

It is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials and process tool development. Each type of reference material has its own set of difficult challenges, involving different combinations of the challenges described above.

MODELING & SIMULATION

SCOPE

The applications of the focus Technology Working Groups (TWGs) are the drivers for the Modeling & Simulation requirements. The following topical areas are treated in this section: 1) *Equipment modeling*—hierarchy of models including the physical environment, conditions, and processes affecting the wafer; 2) *Feature-scale modeling*—front end process, lithography, and topography modeling, including structural, mechanical, and thermal aspects; 3) *Physical device modeling*—hierarchy of physically based models for active devices and interconnect; 4) *Circuit element modeling*—compact models for active, passive, and parasitic circuit components as well as parameter extraction; 5) *Package modeling*—electrical, mechanical, and thermal modeling; 6) *Simulation environments*—graphical user interfaces, tool integration, statistical modeling, coupling to experimental and fab data; 7) *Numerical methods*—grid generators, matrix solvers, parallel algorithms, and surface-advancement techniques.

Modeling is like a stool that requires three legs for a stable result. The three legs are as follows:

1. *Models*—a mental image of reality, formalized in a mathematical model
2. *Simulators*—the computer codes that implement the models
3. *Calibration and Validation*—the comparison of simulated results to relevant experimental data to determine numeric values for parameters and to demonstrate "suitability for purpose"

In early stages of development, modeling and simulation technology is often used to provide insight into technology directions and interactions between options. During later stages, it is used for quantitative analyses like optimization, sensitivity analysis, and process diagnosis. The technical requirements listed in this Roadmap are for the more demanding quantitative applications. Nevertheless, even if the technical requirements for a technology node are not met, modeling and simulation is still a very useful activity since it provides important technical insight.

DIFFICULT CHALLENGES

The difficult challenges listed in Table 62 indicate that the rapid productization of new models is crucial. It is essential to quickly respond to new developments and emerging challenges in focus areas.

Dopant profile evolution is a major concern. Thermal budgets have been reduced so much that profiles are dominated by damage and transient effects. This involves many tightly coupled physical processes, most of which are poorly understood. Dopant and defect metrology are critical to the development and calibration of models for profile evolution. Accurate tools do not exist for dimensional (1-D, 2-D, or 3-D) characterization of sub-100 nm technology.

The importance of interconnect is increasing in process and design. At high frequencies one needs to deal with RLC, transmission-line, and long-range coupling effects on semiconductor substrates. Progress is required towards efficient and accurate full-chip models of the interconnect system. Modeling and simulation technology needs to provide 3-D simulation tools that accurately describe the physical structure and properties of interconnect patterns. New materials and mechanisms (e.g., Cu diffusion through barrier layers into the dielectrics) and the reliability of interconnect systems (electromigration, stress, etc.) are of concern. Tools are needed to better model grain morphology and evolution during processing and during normal operation.

Topography modeling is limited by lack of knowledge of the physical and chemical surface processes (e.g., chemical vapor deposition [CVD], plasma etch, chemical mechanical planarization [CMP]). Selection of reactions and rate coefficients is critical to making predictions on deposited and etched profiles with accuracy in the sub-10 nm regime. Improved models for the physical properties of the resulting

layers need to be developed. Reactor and process design drive the linking of equipment modeling with topography modeling. Approximate methods that address pattern dependencies directly from layout are needed.

Developments in chip size, packaging techniques, power dissipation, and switching speed require new simulation tools that treat thermal, mechanical, and electrical effects self-consistently. Seamless modeling of interconnects from chip to package to board level is needed.

Table 62 Modeling & Simulation Difficult Challenges

DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2006	*SUMMARY OF ISSUES*
Productization of new models	Introduction of new models into industrial use takes ~ 3 years Calibration and validation of models
Defect-mediated dopant profile evolution	Damage dominates profile evolution Metrology for dopant profiles, point, and extended defects
High-frequency interconnect modeling	Accurate 3-D models Efficient simulation of full-chip interconnect delay On- and off-chip RLC Beyond RLC
Physical back-end modeling	Grain structure morphology and evolution Effectiveness of barrier layers Thermo-mechanical behavior, including effects from package CMP models
Packaging modeling	Integrated self-consistent treatment of thermal, mechanical, electrical (RLC and transmission line) effects
Predictive equipment/topography simulation	Reaction paths and rate constants Coupling of reactor and feature models requiring integration across disparate length/time scales Pattern effects
Predictive lithography simulation	Complete system model, improvements needed in models for resist, optical system, and extended resolution methodologies
DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Atomistic process modeling	Development of atomic mechanisms for all processing Atomic variation can dominate device characteristics
Practical nonequilibrium transport	Speed and accuracy in solving Boltzmann transport equation not available by current methods (e.g., DD*, HD**, or MC†) Capturing of non-equilibrium effects in compact models
Advanced quantum device modeling	2-D quantum modeling of MOSFETs

* *DD—drift diffusion model*
** *HD—hydro-dynamic model*
† *MC—Monte Carlo model*

Optical lithography at 150 nm and 130 nm requires modeling approaches that integrate the analysis of the opto-mechanical system with that of the resist materials. New phenomena will become important, such as polymer-surface interaction, chemical amplification, and the interaction of local resolution enhancements with image nonidealities.

Continuum physics models are no longer sufficient below 100 nm. Tools are needed for the physical and chemical processes at an atomic level. These tools will require much more computational resources as well as advanced skills in basic sciences. A hierarchy of tools is needed that is self-consistent and allows the tradeoff of speed versus accuracy.

Carrier transport will be heavily influenced by nonequilibrium effects. No simulation tools are available that meet accuracy, speed, robustness, and user-friendliness requirements at the same time. Towards the 50 nm node, a full 2-D or 3-D quantum description will be needed. Research on such techniques needs to start very early because a long lead time is anticipated.

TECHNOLOGY REQUIREMENTS

EQUIPMENT MODELING

The drivers for equipment modeling are equipment design, process control, sensor design, process design, and process integration. The requirements vary per application and per process being considered (thermal, deposition, etch). Thus, the metrics provided are expressed as a percent of specification limits or metrology capabilities. Models ranging from easy-to-use to complex, from fast-executing to computationally intensive, and from high accuracy in a constrained process space to moderately predictive over wide range should be available to satisfy all uses. Sensor design includes determination of what to measure, where to locate the sensor, as well as creation of "soft sensors," such as the use of a model to predict a quantity of interest from available measurements. As the application moves from equipment design toward process integration, the need for linkage between equipment models and wafer/feature scale models becomes stronger, and the requirements for accuracy become stricter. ESH applications do not generate any additional requirements.

Obtaining the required detailed chemistry and physics information is one of the biggest hurdles. The other chief roadblock is the linkage of equipment models to wafer models. Validation of models is required before their application will be considered. As a minimum, equipment models must be able to predict trends correctly (i.e., correct sign and order of magnitude).

TOPOGRAPHY MODELING

Fundamental reaction mechanisms and rate constants are key to properly capturing the physics and chemistry of surface evolution during thin film etching or deposition. The challenge of understanding ion surface interactions in detail must be met for predictive modeling of plasma-enhanced processes. Future topography simulation must include not only the geometrical shapes of the features, but the material properties and microstructure as well. A hierarchy of approaches from atomistic (molecular dynamics, Monte Carlo, quantum chemistry) to continuum must be employed.

More work is needed on modeling the reliability of the interconnect system, including the effects of electromigration , thermo-mechanical stress, and diffusion through barrier layers. Ultimately, this requires greater understanding of micro-structure (grain formation and evolution) and thin film material properties that differ from those of the bulk.

Providing linked equipment and feature-scale simulation remains a great challenge as the fluxes from the reactor determine the boundary conditions for the feature scale and vice versa. Understanding derived from both the equipment and feature scale areas is also needed for modeling pattern dependent variation. This is a problem of increased concern.

Table 63 Modeling & Simulation Technology Requirements

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Equipment Modeling							
Accuracy of reactor-scale conc. and fluxes versus inputs (% of meas. capab.)	trends	trends	50%	50%	20%	20%	20%
Accuracy of feature-scale conc. and fluxes versus inputs (% of meas. capab.)	trends	trends	50%	50%	20%	20%	20%
Etch/dep/growth uniformity (% spec.)	trends	100%	50%	50%	30%	20%	10%
Topography Modeling							
Δ (3-D topography profile)	6.2 nm	4.5 nm	3.7 nm	3.2 nm	2.5 nm	1.7 nm	1.2 nm
Δ (Interconnect reliability lifetime)	100%	50%	25%	10%	10%	10%	10%
Lithography Modeling							
Δ (3-D pattern profile)	6.2 nm	4.5 nm	3.7 nm	3.2 nm	2.5 nm	1.7 nm	1.2 nm
Front End Process Modeling							
Δ (Vertical and lateral junction depth)	25 nm	17 nm	14 nm	12 nm	10 nm	7 nm	5 nm
Δ (Gate oxide thickness)	0.45 nm	0.35 nm	0.30 nm	1 layer	1 layer	1 layer	1 layer
Δ (Total S/D series resistance)	2.50%	2.50%	2.50%	2.50%	2.50%	2.50%	2.50%
Δ (Long-channel V_t)	100 mV	72 mV	60 mV	60 mV	48 mV	36 mV	32 mV
Physical Device Modeling							
Δ (f_t) @ f_t (GHz)	2 @ 20	3 @ 30	3.5 @ 35	4 @ 40	5.5 @ 55	7.5 @ 75	10 @ 100
Δ (Gate leakage current)	100%	50%	35%	25%	20%	10%	10%
Δ (V_t roll off) (mV)	30	25	20	20	20	20	20
Δ (Time-to-failure)	100%	100%	100%	100%	100%	100%	100%
Δ (Interconnect RLC delay)	5%	5%	5%	5%	5%	5%	5%
Circuit Element Modeling							
Δ (Loaded gate delays)	13 ps	8.0 ps	6.7 ps	4.8 ps	2.8 ps	1.6 ps	1.0 ps
Δ (Speed of 100-element circuit, including speed degradation)	5%	5%	5%	5%	5%	5%	5%
g_m and r_o @ V_t+150 mV versus L, V_{bs}, T	5%	3%	2%	2%	2%	2%	2%
Package Modeling							
Δ (Package delay) (Off-chip clock freq.)	1%	1%	1%	1%	1%	1%	1%
Δ (Stress) (% of yield stress)	10%	10%	10%	10%	10%	10%	10%
Δ (Temp. versus position for chip and pkg.)	5°C	5°C	5°C	5°C	5°C	5°C	5°C

Solutions Exist *Solutions Being Pursued* *No Known Solution*

Table 63 Modeling & Simulation Technology Requirements (Continued)

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Numerical Methods							
Linear solvers—equations/minute	100k	150k	250k	250k	2.5M	5M	5M
Parallel speedup	—	4×	6×	9×	16×	30×	50×
Grid reliability (ppb)	300	180	120	90	26	14	7
MFLOPS* required	50	80	400	1000	4000	8000	8000
MC noise	NA	NA	NA	0.05	0.02	0.01	0.001
Simulation Environments							
Time needed for statistical sim.	10 weeks	6 weeks	4 weeks	2 weeks	2 weeks	1 week	1 week
Time needed for multi-tool initial problem setup	4 weeks	2 weeks	1 week	4 days	2 days	2 days	2 days
Correct data analyses per improvement cycle	0.1	1	1	1	2	4	10

Solutions Exist *Solutions Being Pursued* *No Known Solution*

* *MFLOPS—million floating point operations per second*
* *Number of linear equations generated by discretizing an increasing number of PDEs over a typical device grid of 5000 nodes in 2-D and later 50000 nodes in 3-D*

LITHOGRAPHY MODELING

It is no longer possible to develop lithographic systems that work generically for arbitrary patterns. A shift is observed towards pattern-specific methods such as phase-shift mask and optical proximity correction. Future generations demand further integration of all aspects of lithography to manage pattern-specific behavior.

This requires many advances—1) *Materials Modeling* improvements are needed in resist modeling, polymer-surface interaction, resist bake, resist spinning, silylation and edge roughness; 2) *Optical Modeling* improvements are needed in global application of local resolution enhancement, interaction of resolution enhancement and image nonidealities, substrate interactions, and alignment and overlay of features; and 3) *Non-Optical Modeling* improvements are required in photomask tolerances, proximity X-ray, projection E-beam, inspection, and measurements.

FRONT END PROCESS MODELING

Front end process modeling includes the simulation of the physical effects of manufacturing steps used to build transistors up to metalization, but excluding patterning activities. These areas are important for understanding and optimizing transistor fabrication. The needs for modeling are driven by the reduction of feature size in scaling transistors.

As technology scales, the requirements on implant energies are pushed to sub-keV energies, requiring understanding of the surface interactions and the nuclear stopping power. For wells, energies are being pushed to the MeV range requiring better understanding of electronic stopping mechanisms. Key to both efforts is damage production. The damage interacts with dopant diffusion and creates transient enhanced diffusion (TED), which can produce junction shifts on the order of several hundred nanometers. Significant effort needs to be expended to understand TED well enough so that the effects can be minimized. Despite a decade of work in this area, quantitative predictive models are still not widely available. Diffusion in gate materials needs to be characterized and understood so that gate stack technologies can be optimized.

Thin film growth needs to be better understood. With decreasing dimensions, stress effects on thin films are increasing. This can cause reliability and other problems near corners. This may be particularly true in 3-D structures. Characterization of films with small dimensions and thicknesses is

critically important but extremely difficult. In fact, all models need extensive characterization, which has been difficult and expensive. This drives metrology needs.

DEVICE MODELING

Device modeling includes a suite of formulations and tools from drift-diffusion simulation via hydrodynamic and numerical Boltzmann to Monte Carlo. The drift-diffusion approach, although physically flawed at 250 nm and below, has been remarkably successful. The key challenges are to 1) further develop this hierarchy to include quantum modeling; 2) refine the physical models in these formulations; and 3) provide an easy means of moving through this hierarchy of formulations in a consistent fashion.

Transport phenomena have so far focused on silicon. For 100 nm devices and below, the gate dielectrics will be so thin that gate current will become a very important design factor. Improvements in basic understanding are needed, including reliability aspects. Modeling efforts need to track emerging trends to use new materials and alternative device structures for the 100 nm generation.

CIRCUIT MODELING

Compact modeling and circuit simulation are key to chip design productivity. The challenges are the drastic increase of clock frequency and the exponential increase of the circuit complexity. Two opposing requirements need to be met, namely accuracy and CPU efficiency. The requirement for accuracy is derived from the clock frequency. With the rise/fall time of a gate loaded with an interconnect line at ~10% of the clock period, the accuracy for rise/fall time prediction should be ~10% (i.e., the simulation accuracy should be 1% of the clock period).

This can only be achieved by having accurate DC and high-frequency AC models for transistors, interconnect, passive, and parasitic elements. Model improvements for sub-100 nm need to address velocity overshoot, quantum effects, source barrier effects, and nonquasi-static behavior. Low-voltage technologies emphasize subthreshold and conductance behavior. Robust parameter extraction for these complex models will be a significant challenge.

The interconnect delay is more than 60% of the critical path delay in 350 nm technology and increasing with scaling. The accuracy of interconnect models depends on the interconnect geometry and the material properties, requiring accurate extraction or physical simulation. At 500 MHz clock frequencies, complex electrical effects will be significant such as inductive coupling, ground bounce, transmission-line, and skin effects.

Both active and interconnect models need to be characterized for process variations. For example, the variation in interlevel dielectric (ILD) thickness using CMP is more than 20%. The CPU efficiency of the models and simulations drives the number of circuit elements that can be simulated. Since in critical path analysis as much as 10% of all circuit elements may play a role, the CPU efficiency should be enough to handle 10% of the total component count in an overnight simulation.

PACKAGE MODELING

Packaging needs to meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. Advanced modeling tools are needed that seamlessly cover electrical, thermal, and mechanical aspects, both on- and off-chip. These phenomena can no longer be described independently.

Built-in and thermally induced mechanical stresses need to be modeled throughout the 3-D stack, coupling the chip and package level. The introduction of low-κ dielectrics with low thermal conductivity amplify the need for accurate thermal simulation, which needs to be solved consistently with electrical behavior given the higher power dissipation levels.

To move to 1.5 GHz chip-to-board speeds, the modeling of electrical signal propagation needs to be improved substantially from approximate RLC modeling to full transmission line modeling. Circuit simulation tools need to couple board to package to chip.

NUMERICAL METHODS AND ALGORITHMS

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena in the application tools. For example, more accurate solutions of the Boltzmann transport equation requires dealing with an increasing number of coupled partial differential equations over the device grid, thus driving linear solver technology.

The switch from 2-D to 3-D, the increase in problem complexity, and the increase in steps for process simulation all require that the failure rate in automated grid generation must drop by at least two orders of magnitude. A grid failure can be defined in a local sense as an incorrectly constructed mesh element or in a more global sense as an excessive truncation error induced in a certain region. Adaptable geometry design utilities are required for equipment/reactor design separate from wafer gridding utilities.

Particle-level Monte Carlo codes need an increase in raw CPU speed as well as variance reduction techniques to minimize noise within acceptable simulation times. The rapidly increasing demand for more MFLOPS may be successfully met by improving hardware, provided current trends continue. Workstation speed has improved by 1.8× on average each year since 1990. By the end of the Roadmap, when 640× more CPU cycles will be necessary, the projected trend is that performance needs to improve by a thousand.

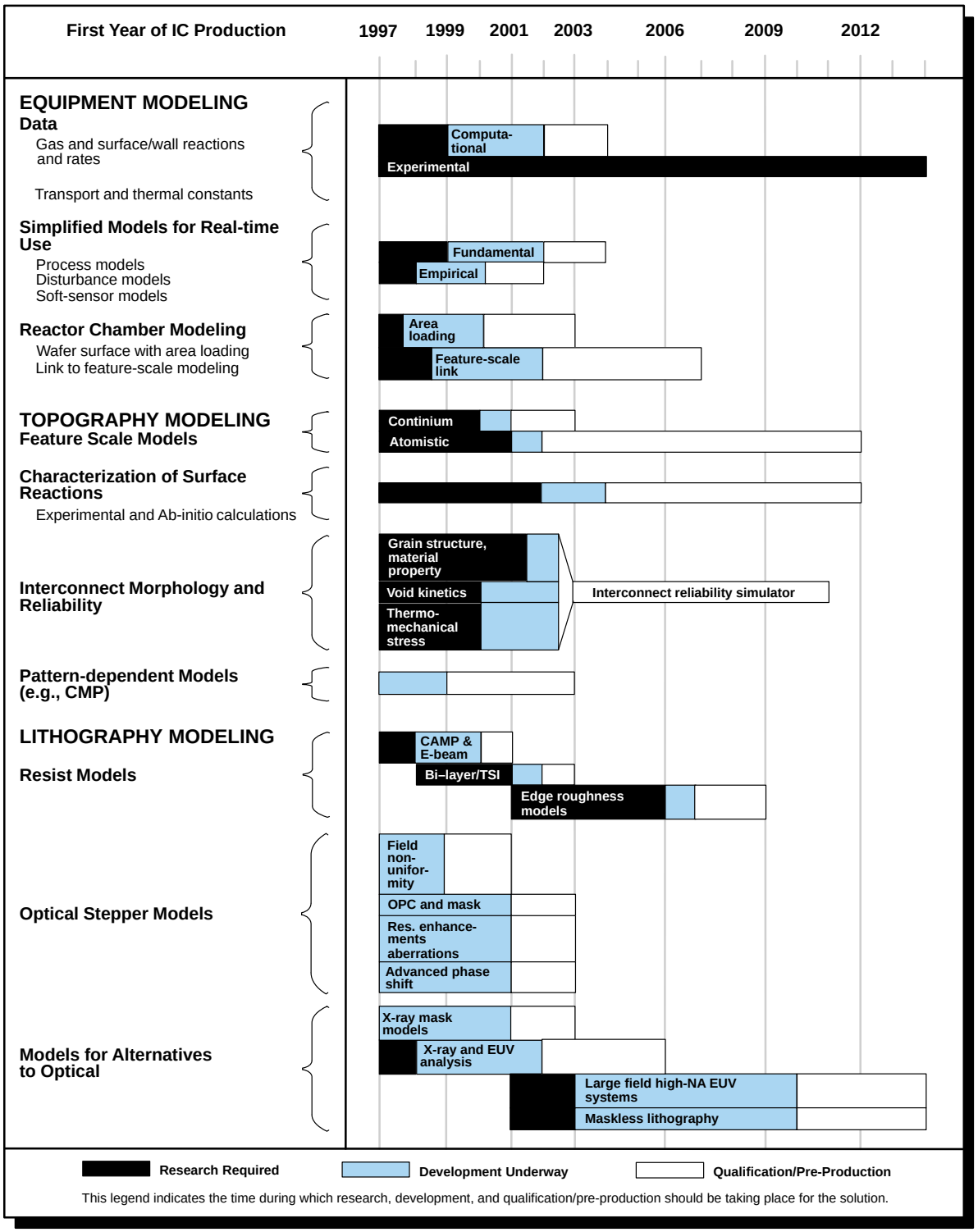
SIMULATION ENVIRONMENT

The practical use of modeling and simulation tools is facilitated by the simulation environment. This requires improvements in 1) *Tool Integration and Data Representation*—continuum physics and atomic-level codes and representations will coexist and require seamless conversion; 2) *Application Development*—synthesis of applications from interoperable modules as well as specific modules that hide underlying complexity; 3) *Group Applications*—many engineers will be working on various simulation aspects of one technology and need to be able to share results and get updates from one another; 4) *Statistical Services*—includes design of experiments, advanced statistical data analysis, sensitivity analysis, batch-mode operation; 5) *Extraction and Calibration*—includes management of coefficient data such as parameter extraction, model selection, and cross-tool optimization.

The ability to effectively utilize all the fab data to make correct and fast decisions is a basic driver for modeling and simulation environments. Thus, analysis tools and modeling tools must be combined into a simulation environment linked into the fab databases.

POTENTIAL SOLUTIONS

Modeling & Simulation potential solutions are charted in Figure 49.



CAMP—chemically amplified positive resist
EUV—extreme ultraviolet

Figure 49 Modeling & Simulation Potential Solutions

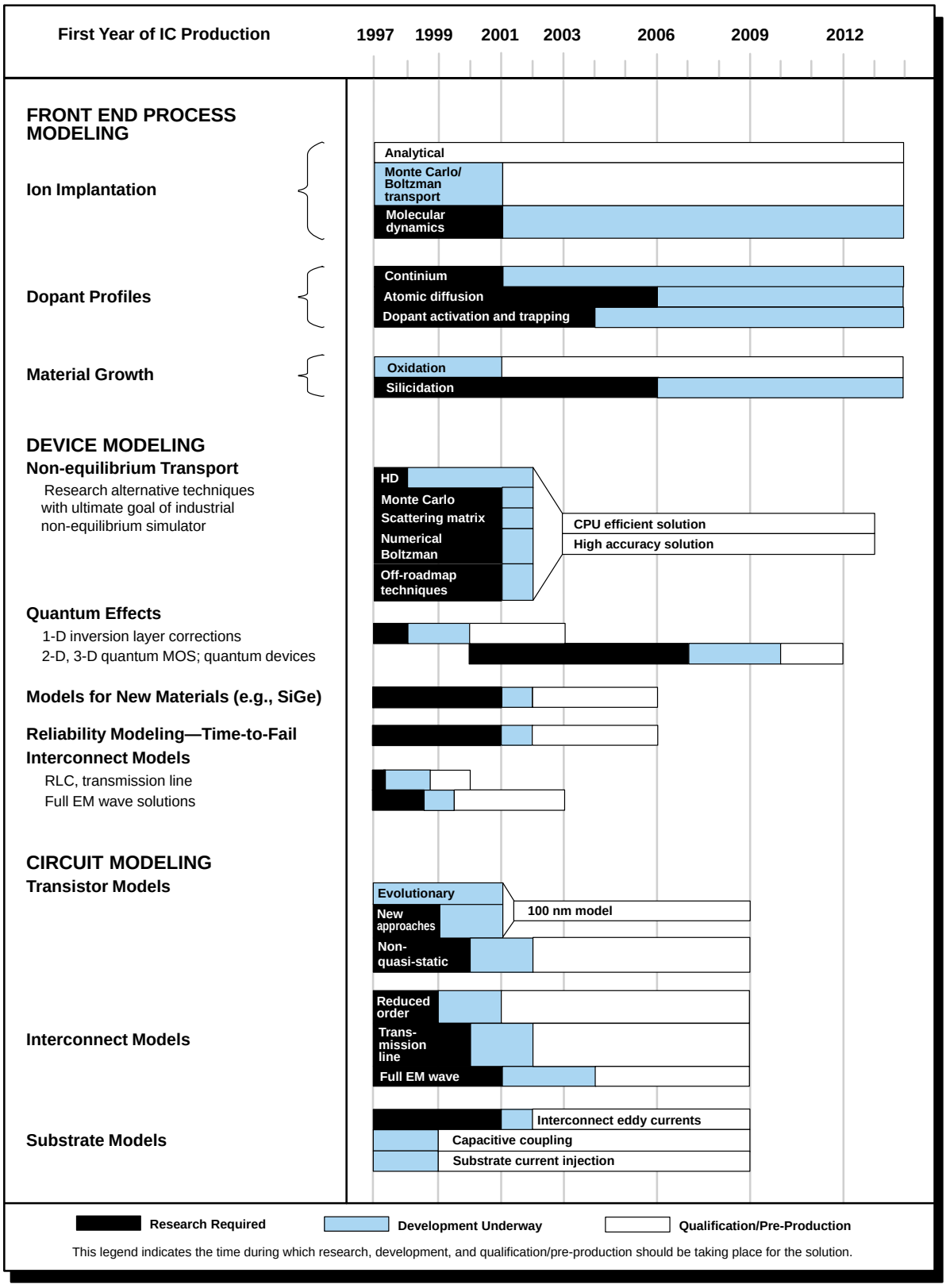


Figure 49 Modeling & Simulation Potential Solutions (Continued)

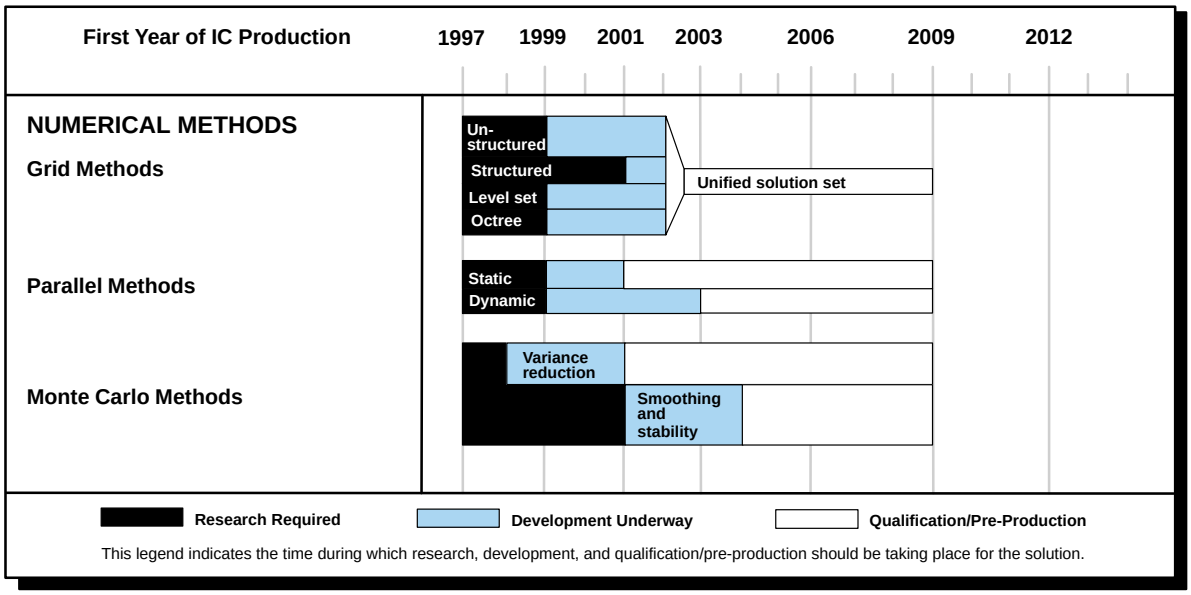


Figure 49 Modeling & Simulation Potential Solutions (Continued)

APPENDIX A

TECHNOLOGY WORKING GROUPS' MEMBERSHIP

DESIGN & TEST

Ray Abrishami, Mark Barber, Don Cottrell, Carlos Dangelo, Al Dunlop, Phil Fisher, Daniel Gajski, Ian Getreu, Robert Grafton, Justin Harlow, Randy Harr, Rich Howard (Co-Chair), Joanne Humiston, Andrew Kahng, Kurt Keutzer, Randy Kramer, Greg Ledenbach, Marc Mydill, Suresh Nadig, Wayne Needham, Bob Nesbitt, Richard Newton, Bill Ortner, Sam Pile, Carl Pixley, Janusz Rajski, Uli Schoettmer, Steven Schulz, Ron Scudder, Charles Sodini, Mike Temple, Dave Vallett, Peter Verhofstadt (Co-Chair), Don Wheater, Bruce Wooley

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

Robert Alexander, Dino Barpoulis, Dave Blackburn, Joe Brewer, Min-hwa Chi, Jim Chung, Ted Dellin, Brian Doyle, Bob Eklund, Scott Elrod, Steve Hillenius (Co-chair), Isaac Lagnado, Bill Lynch (Co-Chair), Martin Manley, Rick Mauntel, Joe McPherson, Jim Meindl, Wyn Palmer, John Pierce, Tak Ning, Sam Shichijo, P.K. Vasudev, Peter Zeitzoff

FRONT END PROCESSES

Vivek Bissessur, Allen Bowling (Co-Chair), Walter Class, Rinn Cleavelin, Michael Current, Alain Diebold, Scott Dunham, Dave Fatke, Gladys Felton-Upton (Co-Chair), Bob Havemann, Bob Helms, Jeanine Herrera, Howard Huff, David Jensen, George Kenig, Larry Larson, Don Linholm, Bill Lynch, Bob McDonald, Pete Panousis, Jagdish Prasad, Dave Seiler, Syd Wilson, Jim Wortman

LITHOGRAPHY

Bill Arnold (Co-Chair), Steven Berger, Skip Berry, Karen Brown (Co-Chair), John Canning, Franco Cerrina, Paul Chipman, Will Conley, Ted Fedynyshyn, Gene Fuller, Mark Gesley, Bob Gleason, George Gomba, Chuck Gwyn, Rich Harbison, Lloyd Harriott, John Herman, Dan Herr, Dan Hutcheson, Loren Linholm, Joe Mogab, Bill Oldham, Dave Patterson, Brett Rolfson, John Shamaly, Dave Shaver, Gil Shelden, Jerry Silverman, Peter Silverman, Grant Willson

INTERCONNECT

Bill Atkins, Sam Broydo, Chris Case, Joe Cecchi, Robin Cheung, George Cumming, Jonathan Dahm (Co-Chair), Bob Doering, Bruce Draper, Darrell Erb, Robert Fink, Dave Fraser, Bob Geffken, Dennis Hartman, Bob Havemann, Jeff Klein, Shyam Murarka, Jim Nulty, Gary Ray, Harry Schafft, Mike Thomas (Co-Chair), Simon Wong

FACTORY INTEGRATION

Jim Ammenheuser, Gabriel Barna, Don Baylis, Ron Billings, Hal Bogardus, Duane Boning, Stephanie Butler, Tom Byrd, Paul Chaloux, Carl Cunningham, Dick Deininger, James Duley, John Everton, Jackie Ferrell, Bill Fosnight, John Fowler, Daniel Gardner, Gary Gettel (Co-Chair), John Gragg, Gordon Greene, Ed Guttes, Ron Gyurcsik, Michael Hanssmann, Scott Hawker, Parris Hawkins, Court Hilton, Bill Jacobs, Rick Jeffrey, Ulrich Kaempf, Bob Kee, Devon Kinkean, Georgia-Ann Klutke, Tom Lambe, Bill Lamkin, Rob Leachman, Richard Lemons, Roy Maxion, Leon McGinnis, Don McIntosh, Gene Meieran, Joseph Montowski, Tony Mullins, John O'Hanlon, Dave Peercy, Paul Peercy, Bill Peterson, Duane Peterson, Kishore Potti, Bob Predmore, Jerry Pyles, Mark Rice, Ralph Richardson, Ray Ritter, Linton Salmon, Ray Schneider, Rick Scott, Joe Seward, Bob Shay, Marie Silverthorn, Perry Skelton, Court Skinner (Co-Chair), Gary Steinbach, Ed Ward, Tom Wear, Tracy Weed, Mitchell Weiss, James Whetstone, Joe White, Harvey Wohlwend, Sam Wood

ASSEMBLY & PACKAGING

Alan Allan, Bill Bottoms, Ron Bracken (Co-Chair), Chi Shi Chang, Jack Fisher, Ed Fulcher, Larry Gilg, George Harman, Jim Hayward, Dennis Herrell, Gil Herrera, Scott Kulicke, Che-Yu Li, Larry Marcanti, Alex Oscilowski (Co-Chair), Bob Pfahl, John Prince, Chuck Steidel, Samuel Wennberg

DEFECT REDUCTION

Robert Alexander, Ram Akella, Bobby Bell, Bob Blewer, Dan Clark, Susan Cohen, Randy Collica, Daren Dance, Keith Dillenbeck, Brian Duffy, Bill Fosnight, Bill Fil, Terry Francis, Pat Gabella, Chris Gondran, Milt Godwin, Mike Grobelny, Charlie Gross (Co-Chair), Lindsey Hall, Zach Hatcher, Ron Harris, Dan Hirleman, Matt Ivanis, David Jensen (Co-Chair), Devon Kinkead, Steve Lakeman, Fred Lakhani, Pat Lamey, Tom Larson, Wojciech Maly, James McAndrew, Dinesh Mehta, Venu Menon, Sanjiv Mittal, Charlie Peterson, Paul Proctor, Ralph J. Richardson, Val Rio, Jennifer Sees, Farhang Shadman, Jieh Hwa Shyu, Ken Tobin, Brian Trafas, Hank Walker

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APPENDIX B

OVERALL TECHNOLOGY CHARACTERISTICS TABLES

Table B–1 Overall Roadmap Technology Characteristics

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF–PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Memory							
Generation @ samples/introduction	256M	1G	*	4G	16G	64G	256G
Generation @ production ramp	64M	256M	1G	1G	4G	16G	64G
Bits/cm2 @ sample/introduction	96M	270M	380M*	770M	2.2B	6.1B	17B
"Affordable" cost/bit @ (packaged—microcents) @ samples/introduction	120	60	30*	15	5.3	1.9	0.66
Logic (High-Volume—Microprocessor)†							
Logic transistors/cm^2 (packed, including on-chip SRAM)	3.7M	6.2M	10M	18M	39M	84M	180M
"Affordable" cost/transistor @ (packaged-microcents)	3000	1735	1000	580	255	110	50
Logic (Low-Volume—ASIC)‡							
Usable transistors/cm^2 (auto layout)	8M	14M	16M	24M	40M	64M	100M
Nonrecurring engineering cost/usable transistor (microcents)	0.05 50	0.025 25	0.02 20	0.015 15	0.01 10	0.005 5	0.0025 2.5
Number of Chip I/Os							
Chip-to-package (pads) (high-performance)	1450	2000	2400	3000	4000	5400	7300
Chip-to-package (pads) (cost-performance)	800	975	1195	1460	1970	2655	3585
Number of Package Pins/Balls							
Microprocessor/controller (cost-performance)	600	810	900	1100	1500	2000	2700
ASIC (high-performance)	1100	1500	1800	2200	3000	4100	5500
Package cost (cents/pin) (cost-performance)	1.40–2.80	1.25–2.50	1.15–2.30	1.05–2.05	0.90–1.75	0.75–1.50	0.65–1.30
Chip Frequency (MHz)							
On-chip local clock (high-performance)	750	1250	1500	2100	3500	6000	10000
On-chip, across-chip clock (high-performance)	750	1200	1400	1600	2000	2500	3000
On-chip, across-chip clock (high-performance ASIC)	300	500	600	700	900	1200	1500
On-chip, across-chip clock (cost-performance)	400	600	700	800	1100	1400	1800

** Generation is for trend purposes only*
† Year 1 data will be less dense than subsequent shrinks
‡ Refers to high-performance, leading-edge, embedded-array ASICs

Table B1 Overall Roadmap Technology Characteristics (Continued)

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF–PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
Chip Frequency (MHz) (continued)							
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)	750	1200	1400	1600	2000	2500	3000
Chip-to-board (off-chip) speed (high-performance, peripheral buses)	250	480	785	885	1035	1285	1540
Chip Size (mm^2)							
DRAM	280	400	445*	560	790	1120	1580
Microprocessor	300	340	385	430	520	620	750
ASIC [max litho field area]	480	800	850	900	1000	1100	1300
Lithographic Field Size (mm^2)	22 × 22 484	25 × 32 800	25 × 34 850	25 × 36 900	25 × 40 1000	25 × 44 1100	25 × 52 1300
Maximum Number Wiring Levels	6	6–7	7	7	7–8	8–9	9
DRAM *1st Year Electrical D_0 @ 60% Yield/* *3rd Year @ 80% Yield (d/m^2)*	2080 /1390	1455 /985	1310* /875*	1040 /695	735 /490	520 /350	370 /250
MPU *1st Year Electrical D_0 @ 60% Yield/* *3rd Year @ 80% Yield (d/m^2)*	1940 /1310	1710 /1150	1510* /1025*	1355 /910	1120 /760	940 /640	775 /525
ASIC *1st Year Electrical D_0 @ 60% Yield (d/m^2)*	1210	725	685*	645	580	530	450
Minimum, mask count	22	22/24	23	24	24/26	26/28	28
Maximum substrate diameter (mm)							
Bulk or epitaxial or SOI***wafer	200	300	300	300	300	450	450
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)	1.8–2.5	1.5–1.8	1.2–1.5	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6
Maximum Power							
High-performance with heat sink (W)	70	90	110	130	160	170	175
Battery (W)—(Hand-held)	1.2	1.4	1.7	2.0	2.4	2.8	3.2
Design and Test							
Volume tester cost/pin ($K/pin) (high-performance)	10	10	10	10	10	10	10
Volume tester cost/pin ($K/pin) (cost-performance)	3	3	3	3	3	3	3

* *Generation is for trend purposes only*
** *D_0—defect density*
*** *Silicon On Insulator*
† *Year 1 data will be less dense than subsequent shrinks*
‡ *Refers to high-performance, leading-edge, embedded-array ASICs*

Table B–2 Multiple Year Intra-generation Data

YEAR OF FIRST PRODUCT SHIPMENT	*1997*	*1999*	*2001*	*2003*	*2006*	*2009*	*2012*
TECHNOLOGY GENERATIONS DENSE LINES (DRAM HALF–PITCH) (nm)	*250*	*180*	*150*	*130*	*100*	*70*	*50*
ISOLATED LINES (MPU GATES) (nm)	*200*	*140*	*120*	*100*	*70*	*50*	*35*
MATURING PRODUCT GENERATION LIFE CYCLE: CHARACTERISTICS PROJECTIONS							
Functions/Chip							
DRAM bits/chip—Years 1–6	267M	1.07G	1.7G*	4.29G	17.2G	68.7G	275G
Microprocessor total transistors/chip—Years 1–6	11M	21M	40M	76M	200M	520M	1.40B
Chip Size (mm^2)							
DRAM—Year 1	280	400	445*	560	790	1120	1580
DRAM—Year 3 (2^{nd} shrink)	170	240	270*	340	480	670	950
DRAM—Year 6 (2^{nd} cut-down—next gen.)	100	140	160*	200	280	390	550
Microprocessor—Year 1	300	340	385	430	520	620	750
Microprocessor—Year 3 (2^{nd} shrink)	180	205	230	260	310	370	450
Microprocessor—Year 6 (2^{nd} cut-down—next gen.)	110	125	140	150	180	220	260
Function Density (Functions/cm^2)							
DRAM Bits/cm^2—Year 1	96M	270M	380M*	770M	2.2B	6.1B	17B
DRAM—Year 3 (2^{nd} shrink)	160M	450M	640M*	1.3B	3.6B	10B	29B
DRAM—Year 6 (2^{nd} cut-down—next gen.)	270M	770M	1.1B*	2.2B	6.2B	18B	50M
Microprocessor total transistors/cm^2 (packed)—Year 1	3.7M	6.2M	10M	18M	39M	84M	180M
Microprocessor total transistors/cm^2 (packed)—Year 3 (2^{nd} shrink)	6.1M	10M	17M	29M	64M	140M	310M
Microprocessor total transistors/cm^2 (packed)—Year 6 (2^{nd} cut-down—next gen.)	10M	17M	29M	50M	110M	240M	530M
"Affordable" Packaged Unit Cost/Function (Microcents/Function)							
DRAM packaged unit cost/bit @ (microcents)—Year 1	120	60	30*	15	5.3	1.9	0.66
DRAM packaged unit cost/bit @ (microcents)—Year 3 (2^{nd} shrink)	36	18	9*	4.5	1.6	0.57	0.20
DRAM packaged unit cost/bit @ (microcents)—Year 6 (2^{nd} cut-down—next gen.)	6.0	3	1.5*	0.76	0.28	0.09	0.03
Microprocessor packaged unit cost/transistor @ (microcents)—Year 1	3000	1735	1000	580	255	110	49
Microprocessor packaged unit cost/transistor @ (microcents)—Year 3 (2^{nd} shrink)	910	525	305	175	75	34	15
Microprocessor packaged unit cost/transistor @ (microcents)—Year 6 (2^{nd} cut-down—next gen.)	290	167	97	56	24	11	4.7

** 1.7G Generation is for trend purposes only, and may not actually occur*

GLOSSARY OF OVERALL CHARACTERISTICS

Nominal Generational Scale

YEAR OF FIRST PRODUCT SHIPMENT (Inter-generation, Table B1 and B2)—Year in which the leading chip manufacturer supplies quantities of samples (10K–100K) of dynamic random access memories (DRAMs) that are manufactured with production tooling (Other technology family members, such as microprocessors (MPUs) of the same generation (same feature size], are now being introduced concurrently, and in some cases, ahead of the DRAM product.)

TECHNOLOGY GENERATIONS (Minimum Feature Size [nm])—Ground rules of process is governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level feature size. For logic, such as microprocessors (MPUs), gate length is most representative of the technology level.

MATURING PRODUCT GENERATION LIFE CYCLE: CHARACTERISTICS PROJECTIONS (Intra-Generation, Table B2)—Year 1 is the inter-generation first product shipment year. Manufacturing process and equipment technology improves continually within a given technology generation. Chip size "shrinks" occur annually to take advantage of the latest manufacturing process and equipment, which improve continually within a given technology generation.
Year 3 marks the completion of the second full production year of the product generation using the second shrink of the chip.
Year 6 (completion of 5^{th} year of production) of a given product generation is actually manufactured using super-shrink (cut-down) product on the next technology-generation manufacturing line.

Characteristics Of Major Markets

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs, application-specific integrated circuits [ASICs]) that can be cost-effectively manufactured on a single monolithic chip at the available technology level (Logic transistors include both SRAM and logic transistors.)

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured at a given product and manufacturing technology node (Estimates are projected based upon historical data trends. Multi-chip-packaged memory and logic are not covered explicitly.)

"Affordable" Packaged Unit Cost/Function—Final cost in microcents of a tested and packaged chip divided by ***Functions/Chip***
Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Smaller chip sizes from technology and design improvements; increasing wafer diameters; decreasing equipment cost-of-ownership (CoO); increasing equipment overall equipment effectiveness; and reduced package and test costs, etc. are all needed to meet the affordability requirements.)

Functions/cm^2—The ***Functions/Chip*** on a single monolithic chip divided by the ***Chip Size***.

Memory

Generation @ Samples/Introduction—The anticipated bits/chip of the DRAM product generation introduced at a given manufacturing technology node

Generation @ Production Ramp—The anticipated bits/chip of the DRAM generation that is ramping into volume production at a given manufacturing technology node (This overlaps with the introduction of the next product generation.)

Bits/Chip—Nominal number of functional bits (after repair) on a single monolithic chip

Logic (High Volume—Microprocessor)

Microprocessor Total Transistors/Chip—Nominal number of all SRAM and logic transistors that are anticipated (based upon historical trends) to be on a single monolithic chip at a given technology node

Logic (Low Volume—ASIC)

Usable Transistors/cm^2 (Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells.

NRE Cost/Transistor (Microcent)—Nonrecurring engineering cost in microcents (chip design, test design, masks, etc.) divided by the number of transistors/chip and amortized over the production volume.

Chip and Package—Physical and Electrical Attributes

Number Of Chip I/Os

Chip-to-package (pads)(high-performance)—Number of I/O pads of chip permanently connected to package plane for functional or test purposes and includes any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.)

Number Of Package Pins/Balls

Microprocessor/controller cost-performance—Number of pins or solder balls presented by the package for connection to the board (This may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package.)

ASIC (high-performance)—Same definition as microprocessor/controller

Package cost (cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin

Chip Frequency (MHz)

On-chip, local clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip

On-chip, across-chip clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors for interconnect signals that run across the full width of the chip (Typically, this is lower than the localized clock performance due to capacitance loading of the long cross-chip interconnect.)

On-chip, across-chip ASIC clock, high-performance—Same as local clock high-performance

On-chip, across-chip, cost-performance—On-chip clock frequency of cost-performance high-volume microprocessors for interconnect signals that run across the full width of the chip

Chip-to-board (off-chip) speed (high-performance, reduced-width, mutiplexed bus)—Maximum signal I/O frequency to specialized board reduced-width, multiplexed buses of high and low volume logic devices

Chip-to-board (off-chip) speed (high-performance, peripheral buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node

Maximum Number Of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution

Fabrication Attributes And Methods

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic)

Maximum Substrate Diameter (mm)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers

Electrical Design And Test Metrics

Power Supply Voltage (V)

Minimum Logic V_{dd}— Nominal operating voltage of chips from power source for operation at design requirements

Maximum Power

High-performance with heat sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink

Battery (W)—Maximum total power/chip dissipated in battery operated chips

Design And Test

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

APPENDIX C

ACRONYMS

A

AC, alternating current
AFM, atomic force microscopy
ALE, application logic element
AMHS, automated material handling systems
AQL, acceptable quality level
APC, advanced process control
APM, atmospheric passivation module OR acoustic plate mode
ARAMS, Automated Reliability, Availability, and Maintainability Standard
ARC, antireflective coating
ARDE, aspect-ratio-dependent etching
ASIC, application-specific integrated circuit
ASP, average selling price
ASTM, American Society for Testing and Materials
ATE, automatic test equipment
ATPG, automatic test pattern generation
AWG, arbitrary waveform generation

B

BEOL, back end of line
BESOI, bonded and etchback SOI
BF, bright field
BGA, ball grid array
BiCMOS, bipolar complementary metal-oxide semiconductor
BIST, built-in self test
BMD, bulk micro defects
BOX, buried oxide
BPSG, boro phosphosilicate glass
BW, bandwidth

C

CAD, computer-aided design
CAGR, compound annual growth rate
CAM, computer-aided manufacturing
CAMP, chemically amplified positive resist
CD, critical dimension

CDE, chemical downstream etch
CFM, contamination-free manufacturing
CIM, computer-integrated manufacturing
CMOS, complementary metal-oxide semiconductor
CMP, chemical mechanical planarization
CNC, condensation nucleus counter
CoO, cost of ownership
COP, crystal originated pits
C_p , process capability
C_{pk} , process capability index
CPU, central processing unit
CRM, certified reference materials
CSP, chip scale packages
CTE, coefficient of thermal expansion
CVD, chemical vapor deposition
CZ, Czochralski

D

DBMS, data base management system
DCA, direct chip attachment
DC, direct current
DD, drift diffusion model
DF, dark field
DFESH, design for ESH
DFLP, design for low power
DFM, defect free manufacturing
DFR, design for reliability
DFT, design for testability
DFX, design for manufacturability
DI, deionized
DIBL, Drain Induced Barrier Lowering
DLBI, device level burn-in
DLT, device level test
DoC, Department of Commerce
DoD, Department of Defense
DOE, design of experiments
DoE, Department of Energy
DOF, depth of field
DRAM, dynamic random access memory
DSM, deep sub-micron
DSP, digital signal processing

DUT, device under test
DUV, deep ultraviolet

E

EBDW, electron-beam direct-write
ECAD, engineering computer-aided design
ECL, emitter coupled logic
ECR, electron cyclotron resonance
EDA, electronic design automation
EDI, electronic data interchange
EDIF, electronic design interchange format
EGE, ethylene glycol ethers
EM, electromigration
EMC, electromagnetic compatibility
EMG, electromigration
EMI, electromagnetic interference
EPA, Environmental Protection Agency
ESD, electrostatic discharge
ESH, Environment, Safety, and Health
EUV, extreme ultraviolet
EWMA, exponentially weighted moving average

F

FA, failure analysis
FEP, front end processes
FEOL, front end of line
FFT, Fast Fourier Transform
FIB, focused ion beam
FIT, failures in time
FPGA, field programmable gate array
FS, sample rate
FSM, finite state machine
FTAB, focused technical advisory board
FTIR, Fourier transform infrared spectroscopy

G

GEM, Generic Equipment Model
GILD, gas immersion laser doping
GOI, gate oxide integrity
GUI, graphical user interface

H

HAP, hazardous air pollutants
HD, hydro dynamic model
HDL, hardware description language
HDP, high density plasma
HIBS, heavy ion backscattering
HVAC, heating, ventilation, and air conditioning

I

IC, integrated circuit
ICP, inductively-coupled plasma
IDDQ, direct drain quiescent current
ILD, interlevel dielectric
I/O, input/output
IP, ion projection OR intellectual property
IIPC, Institute for Interconnecting and Packaging Electronic Circuits
IR, infrared
ISO, International Standards Organization
ISX, inherently self-X
IWG, implementation working group

J

JEDEC, Joint Electron Device Engineering Council

K

KGD, known good die

L

LATID, large angle tilt implant device
LDD, lightly doped drain
LPCVD, low pressure CVD
LOCOS, local oxidation of silicon
LSI, large-scale integration

M

MARCO, Microelectronics Advanced Research Corporation
MBP, materials and bulk processes
MB/s, megabit/second
MC, Monte Carlo model
MCM, multichip module
MCP, multichip package
MCS, material control system

MCZ, magnetic Czochralski
MEMS, micro-electromechanical system
MES, manufacturing execution system
MESC, Modular Equipment Standards Committee (SEMI)
MFLOPS, million floating point operations per second
MIES, manufacturing information and execution system
MIMO, multi-input/multi-output
MLM, multi level metal
MOS, metal-oxide semiconductor
MOSCAP, metal-oxide semiconductor capacitor
MOSFET, metal-oxide semiconductor field effect transistor
MPU, microprocessor
MSDS, material safety data sheet
MTBF, mean time between failure
MTBI, mean time between incident
MWBD, mean wafers between defects

N

NEMI, National Electronic Manufacturers Initiative
NFOM, near field optical microscopy
NIST, National Institute of Standards and Technology
NMOS, negative channel metal-oxide semiconductor
NRE, nonrecurring engineering
NRZ, nonreturn-to-zero
NSF, National Science Foundation
NTRM®, NIST Traceable Reference Materials
NTRS, National Technology Roadmap for Semiconductors

O

OBEM, object-based equipment model
ODS, ozone-depleting substances
OEE, overall equipment effectiveness
OES, optical emission spectroscopy
OFE, overall factory effectiveness
OPC, optical proximity correction
ORTC, overall roadmap technology characteristics

P

PBGA, plastic ball grid array
PC, phase contrast
PFC, perfluorocompound
PGILD, projection gas immersion laser doping
PID, proportional integral differential
PIDS, Process Integration, Devices & Structures
PIII, plasma immersion ion implantation
PM, preventive maintenance
PMOS, positive channel metal-oxide semiconductor
POU, point-of-use
PPC, process proximity correction
PR&D, process research and development
PSD, power spectral density
PSG, phosphosilicate glass
PSL, polystyrene latex
PSM, phase shift mask
P/T, precision to tolerance
PTAB, project technical advisory board
PTH, plated through hole
PVD, physical vapor deposition
PVDF, polyvinylidene fluoride
PWP, particles per wafer pass

Q

QDR, quick dump rinse
QFP, quad flat package

R

RCG, Roadmap Coordinating Group
R&D, research and development
RET, resolution enhancement techniques
RF, radio frequency
RIE, reactive ion etching
RMS, root main square OR Recipe Management Standard
RTL, Resistor Transistor Logic OR resistor transistor level
RTP, rapid thermal processes
RZ, return-to-zero

S

SCM, scanning capacitance microscopy
SCP, single chip package
S/D, source/drain
SDMBIM, sensor-driven, model-based integrated manufacturing
SECS, semiconductor equipment communication standard
SEM, scanning electron microscopy
SEMI, Semiconductor Equipment and Materials International
SFDR, spurious free dynamic range
SFQR, see Table 20
SIA, Semiconductor Industry Association
SIMOX, separation by implantation of oxygen
SIMS, secondary ion mass spectrometry
SL, single layer
SM, stress migration
SMT, surface mount technology
SNUR, Significant New Use Rule
SOG, spin-on glass
SOC, system on a chip
SOI, silicon on insulator
SPC, statistical process control
SPICE, simulated program with integrated circuit emphasis
SPM, scanning probe microscopy
SRAM, static random access memory
SRC, Semiconductor Research Corporation
SRM®, Standard Reference Materials
SRP, spreading resistance profiling
SSA, spatial signal analysis
STI, shallow trench isolation
SWIM, Semiconductor Workbench for Integrated Modeling

T

TAB, tape automated bonding
TCAD, technology computer-aided design
TD, threading dislocation OR thermal desorption
TED, transient enhanced diffusion
TEM, transmission electron microscopy
TFC, total fault coverage
TFT, thin film transistors
THC, total hydrocarbon
TLI, thin layer imaging

TOC, total oxidizable carbon
ToF, time of flight
TPG, test pattern generation
TPM, total productive maintenance OR total productive manufacturing
TSCA, Toxic Substance Control Act
TWG, Technology Working Group
TXRF, total X-ray reflection fluorescence

U

UBM, under bump metallurgy
ULSI, ultra large scale integration
UPW, ultrapure water
UV, ultraviolet

V

VHDL, Verilog hardware descriptive language
VLSI, very large-scale integration
VME, virtual manufacturing enterprise
VOC, volatile organic compound
VPD, vapor phase decomposition

W

WEC, wafer environment control
WIP, work in progress
WLBI, wafer-level burn-in
WLR, wafer-level reliability
WSM, wafer starts per month
WLT, wafer-level test

Y

YR, yield ramp

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