Multi-Chip Module Status

MVD Critical Path
Electronic die fabrication and MCM define electronics schedule

All electronic die designed
- AMUADC in fabrication
- TGV32 -
  - Last minute switch to HP
  - Design review Dec 15 - results look good
- Xilinx 4010 in fabrication

All must be Known Good Die - ISE

MCM high risk
- Design impacts ALL of mechanics and cooling designs
- Only one vendor! - Lockheed Martin

LDRD project on simpler MCM:

Used 8 channel die
32 total channels

8 months behind schedule
100% cost overrun
Poor communication and management
Little Q&A procedures
Low yield
Currently being tested

Meeting at Lockheed Martin - November 17th

* Managment reports to us once a week
* Q&A procedures defined and monitored
* Have recently unionized - rigid training
* Changing from R&D to production facility
* Have increased facility in terms of setup
* Purchased equipment spares
* Have prepared openning in schedule with little competition
* Detailed SOW
* LANL Designer at LM for design exchange and verification
* Cost + fixed fee contract is risk

Tentatively and generally agreed to cost and schedule

Final MCM

Design at LANL/NIS
Lead Engineer - Gary Smith
Lead Designer - Gary Richardson

256 channels/MCM
4 preamp, 4 AMUADC, 2-4010, opamp, T sensor per MCM
Trace pitch = 54 μm
line width = 43 μm
I/O pad pitch = 150μm

4 layers + base metal

M0 = 0.1μm titanium/0.3μm Cu/4μm Cu
M1 = Signals, all connections off IC chips
M2 = Bus lines
M3 = Power lines
M4 = surface mount components