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DATE: September 10, 1997 Revised PPM-97-029
TO: P. Huber/400
FROM: K. Sahu/300.1 KS
SUBJECT: Radiation Report on: AD562
Project: GOES-NO/PQ
Job #: EE78166
Project part #: AD562

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A radiation evaluation was performed on AD562 (12 bit A/D Converter) to determine the total dose tolerance of these parts. A brief summary of the test results is provided below. For detailed information, refer to Tables I through IV and Figure 1.

The total dose testing was performed using a Co^{60} gamma ray source. During the radiation testing, eight parts were irradiated under bias (see Figure 1 for bias configuration) and two parts were used as control samples. The total dose radiation levels were 10.0, 20.0, 35.0, 50.0, 75.0, 100.0, 125.0, 150.0 and 200.0 kRads.* The dose rate was between 0.250 and 1.250 kRads/hour (0.069 to 0.36 Rads/sec.). (See Table II for radiation schedule.) After the 125.0 kRad exposure, the parts were annealed for 360 hours at 25°C. After the 150.0 kRad exposure, the parts were stored without bias for several weeks before the 200 kRad exposure. After each radiation exposure and annealing treatment, parts were electrically tested according to the test conditions and the specification limits** listed in Table III. Additionally, the biasing power supply current was monitored during each irradiation step.

Initial electrical measurements were made on 10 samples. Eight samples (SN's 1, 2 (PMI), 168, 169, 170, 171, 172, and 173 (Analog Devices)) were used as radiation samples while SN's 166 and 167 (AD) were used as control samples. All parts passed all tests during initial electrical measurements.

Analog Devices Parts:

All parts passed all tests upon irradiation to 35.0 kRads. No significant degradation was observed in any test parameter.

After the 50.0 kRad irradiation, most parts marginally exceeded the specification limit of ±0.500 lsb for DNL with readings in the range of 0.513 to 0.605 lsb. **All parts passed all other tests.**

After the 75.0 kRad irradiation, parts showed further degradation in DNL. Only SN 172 passed the DNL test, other readings were in the range of 0.515 to 1.017 lsb. **All parts passed all other tests.**

After the 100.0 kRad irradiation, all parts failed the DNL test with readings in the range of 0.593 to 1.682 lsb. **All parts passed all other tests.**

After the 125.0 kRad irradiation, all parts failed the DNL test with readings in the range of 0.572 to 1.461 lsb. **All parts passed all other tests.**

After annealing the parts for 360 hours at 25°C, the parts showed significant recovery in DNL with only two parts exceeding the specification limit with readings of 0.835 and 0.584 lsb.

* The term Rads, as used in this document, means Rads (silicon). All radiation levels cited are cumulative.
** These are manufacturer's pre-irradiation data specification limits. The manufacturer provided no post-irradiation limits at the time these tests were performed.

After the 150 kRad irradiation, the readings were similar to post 75 kRad levels with SN172 passing DNL and all others in the range of 0.527 to 1.223 lsb. **All parts passed all other tests.**

After sitting without bias for 39 days, the parts showed no recovery with readings almost identical to those for 150 kRads.

After the 200 kRad irradiation, all parts except SN 173 (see below) exceeded the specification limit for DNL with readings in the range of 0.629 to 1.622 lsb. SN 173 suffered a catastrophic failure in TTL_zero with a reading of 32.41 lsb, CMOS_zero with a reading of 32.38 lsb, exceeded the specification limit for LE with a reading of 1.425 lsb, and exceeded the specification limit for DNL with a reading of 19.166 lsb. **All parts passed all other tests.**

PMI Parts:

All parts passed all tests upon irradiation to 20.0 kRads. No significant degradation was observed in any test parameter.

After the 35.0 kRad irradiation, both parts marginally exceeded the specification limit of ±0.500 lsb for DNL with readings of 0.734 and 0.618 lsb. **Both parts passed all other tests.**

After the 50.0 kRad irradiation, both parts continued to degrade in DNL with readings of 1.168 and 0.974 lsb. **Both parts passed all other tests.**

After the 75.0 kRad irradiation, both parts showed significant degradation in DNL readings were 1.284 and 1.476 lsb. **Both parts passed all other tests.**

After the 100.0 kRad irradiation, both parts further degraded in DNL with readings of 1.999 and 2.376 lsb. SN 2 also exceeded the specification limit of ±0.500 lsb for LE with a reading of 0.724 lsb. **Both parts passed all other tests.**

After the 125.0 kRad irradiation, both parts further degraded in both the LE and DNL tests. Readings were 0.649 and 1.625 lsb for LE and 2.103 and 4.193 lsb for DNL. **Both parts passed all other tests.**

After annealing the parts for 360 hours at 25°C, the parts showed significant recovery, but continued to fail LE and DNL. Readings were 0.573 and 0.828 lsb for LE and 1.883 and 2.447 lsb for DNL. **Both parts passed all other tests.**

After the 150 kRad irradiation, both parts again continued to fail LE and DNL with readings of 0.647 and 0.863 lsb for LE and 2.114 and 3.234 lsb for DNL. **Both parts passed all other tests.**

After sitting without bias for 39 days, the parts showed no recovery with readings almost identical to those for 150 kRads.

After the 200 kRad irradiation, both parts again continued to fail LE and DNL with readings of 0.665 and 1.328 lsb for LE and 2.410 and 4.305 lsb for DNL. **Both parts passed all other tests.**

Table IV provides a summary of the test results with the mean and standard deviation values for each parameter after each irradiation exposure and annealing step.

Any further details about this evaluation can be obtained upon request. If you have any questions, please call me at (301) 731-8954.

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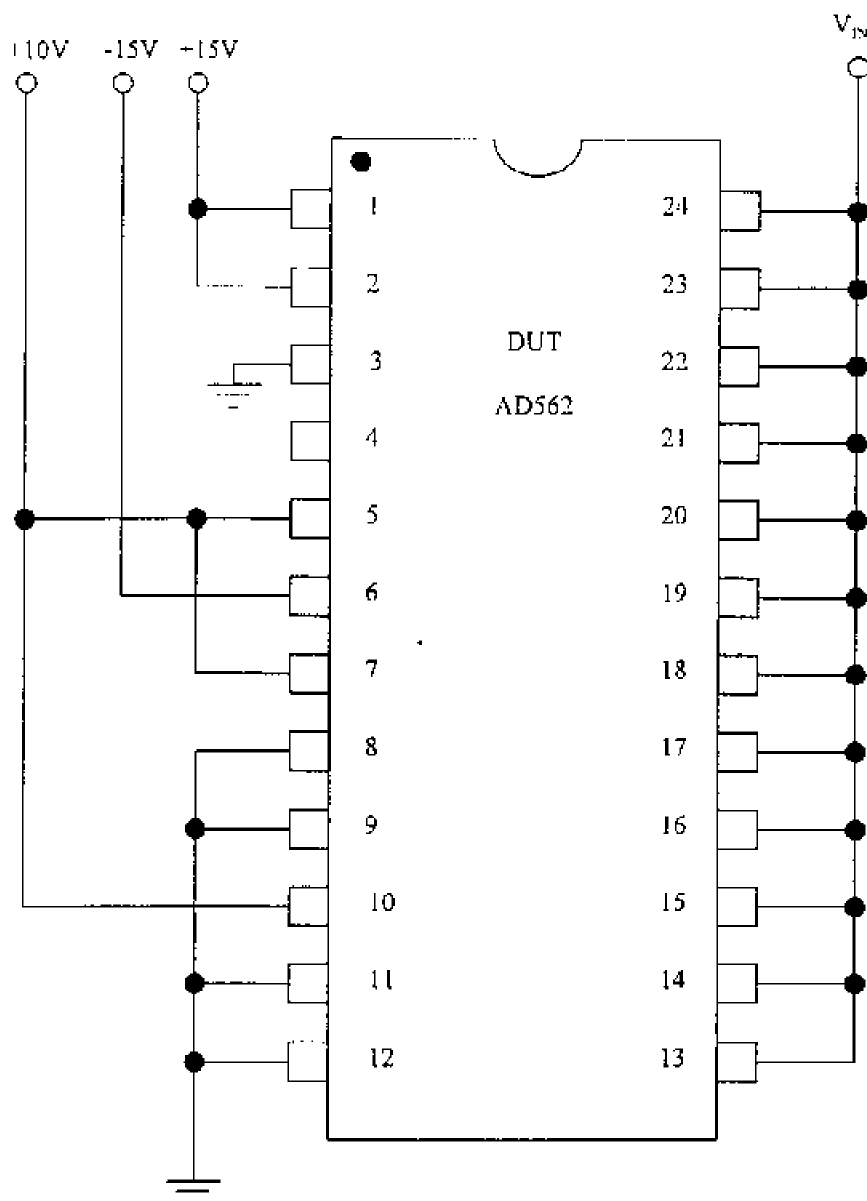
Figure 1. Radiation Bias Circuit for AD562



Notes:

1. V_{IN} = 0V to 15V peak to peak square wave with f_o = 1kHz.
2. Measure and record I_{CC} before and after each radiation exposure.

Pin Configuration:

1: V_{CC} +5V/+15V IN 2: CMOS/TTL Logic Threshold 3: Ref V, LO IN 4: AMP Summing Junction 5: Ref V, HI IN 6: V_{EE} -15V IN
7: Bipolar Offset R IN 8: Bipolar Offset R OUT 9: DAC OUT 10: 10V Span R 11: 20V Span R 12: GRD
13 – 24: Bit 12 (LSB) IN to Bit 1 (MSB) IN

TABLE I. Part Information

Generic Part Number:	AD562
GOES-NO/PQ Part Number:	AD562
Charge Number:	EE78166
Manufacturer:	PMI, Analog Devices
Lot Date Code (LDC):	PMI: 8742, AD: 9647A
Quantity Tested:	10
Serial Numbers of Control Samples:	166, 167 (AD)
Serial Numbers of Radiation Samples:	1, 2 (PMI), 168, 169, 170, 171, 172, 173 (AD)
Part Function:	12-bit A/D Converter
Part Technology:	Bipolar
Package Style:	24 Pin DIP
Test Equipment:	A540
Test Engineer:	S. Norris

- The manufacturer for this part guaranteed no radiation tolerance/hardness.

TABLE II. Radiation Schedule for AD562

EVENT	DATE
1) INITIAL ELECTRICAL MEASUREMENTS	06/13/97
2) 10.0 KRAD IRRADIATION (0.250 KRADS/HOUR)	06/16/97
POST-10.0 KRAD ELECTRICAL MEASUREMENT	06/17/97
3) 20.0 KRAD IRRADIATION (0.250 KRADS/HOUR)	06/17/97
POST-20.0 KRAD ELECTRICAL MEASUREMENT	06/18/97
4) 35.0 KRAD IRRADIATION (0.250 KRADS/HOUR)	06/18/97
POST-35.0 KRAD ELECTRICAL MEASUREMENT	06/19/97
5) 50.0 KRAD IRRADIATION (0.250 KRADS/HOUR)	06/19/97
POST-50.0 KRAD ELECTRICAL MEASUREMENT	06/20/97
6) 75.0 KRAD IRRADIATION (0.750 KRADS/HOUR)	06/23/97
POST-75.0 KRAD ELECTRICAL MEASUREMENT	06/25/97
7) 100.0 KRAD IRRADIATION (1.250 KRADS/HOUR)	06/25/97
POST-100.0 KRAD ELECTRICAL MEASUREMENT	06/27/97
8) 125.0 KRAD IRRADIATION (1.250 KRADS/HOUR)	07/01/97
POST-125.0 KRAD ELECTRICAL MEASUREMENT	07/03/97
9) 360 HOUR ANNEALING @25°C	07/03/97
POST-360 HOUR ANNEAL ELECTRICAL MEASUREMENT	07/22/97
10) 150.0 KRAD IRRADIATION (1.250 KRADS/HOUR)	07/23/97
POST-150.0 KRAD ELECTRICAL MEASUREMENT	07/25/97
11) 39 DAYS UNBIASED @25°C	07/25/97
POST-39 DAYS UNBIASED ELECTRICAL MEASUREMENT	09/03/97
12) 200.0 KRAD IRRADIATION (1.250 KRADS/HOUR)	09/03/97
POST-200.0 KRAD ELECTRICAL MEASUREMENT	09/05/97

Effective Dose Rate = 150,000 RADS/40 DAYS = 156.3 RADS/HOUR=0.043 RADS/SEC.
The 200 kRad run is not included in this calculation due to the extreme time difference between steps.

PARTS WERE IRRADIATED AND ANNEALED UNDER BIAS, SEE FIGURE 1.

Table III. Electrical Characteristics of AD562 /1

For all tests: V_{CC}=5V, V_{SS}=-15V, AGND and DGND=0V, V_{REF}=10V unless otherwise specified.

Test #/2	Parameter	Symbol	Units	Test Conditions	Spec. Lim. min	Spec. Lim. max
1	+Supply Current	$I_{CC}1$	mA	TTL, V_S = 15V, V_{IN} = logic 1 = 2.0V, V_{CC}= 15V	3.0	18.0
2	+Supply Current	$I_{CC}2$	mA	CMOS, V_S = 15V, V_{IN} = logic 1 = 0.0V, V_{CC}=15V	3.0	18.0
3	-Supply Current	$I_{EE}1$	mA	TTL, V_S = 15V, V_{IN} = logic 0 = 2.0V, V_{SS}=-15V	-25.0	-5.0
4	-Supply Current	$I_{EE}2$	mA	CMOS, V_S = 15V, V_{IN} = logic 0 = 0.0V, V_{SS}=-15V	-25.0	-5.0
6-17	Input Current High	Iih	µA	V_S = 15V, Pin 2 tied to Pin 1, V_{IN} = logic 1 = 10.5V	-1.0	100.0
18-29	Input Current Low	Iil	µA	V_S = 15V, Pin 2 tied to Pin 1, V_{IN} = logic 1 = 0V	-200.0	1.0
30	Zero Scale Current	TTL_zero	lsb	V_{IN} = logic 0 = 0V, V_O = 0V	-2.0	2.0
31	Zero Scale Current	CMOS_zero	lsb	V_S = 15V, Pin 2 tied to Pin 1, V_{IN} = logic 0 = 0V, V_O = 0V	-2.0	2.0
32	Unipolar Output Current	U_Iout	mA	Unipolar mode	-2.4	-1.6
34	Power Supply Sensitivity	Pss1	lsb	Unipolar mode, TTL, V_S = 5 ±0.5V, V_{IN} = logic 1 and 0	-0.328	0.328
35	Power Supply Sensitivity	Pss2	lsb	Unipolar mode, CMOS, V_S = 15 ±1.5V, V_{IN} = logic 1 and 0	-0.328	0.328
36	Power Supply Sensitivity	Pss	lsb	Unipolar mode, CMOS, V_S = 5 ±0.5V, V_{IN} = logic 1 and 0	-1.310	1.310
37	Linearity Error	LE	lsb	Unipolar mode	-0.500	0.500
38	Diff. Nonlinearity	DNL	lsb	Unipolar mode	-0.500	0.500

Notes:

1/ These are the manufacturer's non-irradiated data sheet specification limits. The manufacturer provided no post-irradiation limits at the time the tests were performed

2/ There are no tests 5 or 33.

TABLE IVa: Summary of Electrical Measurements After Total Dose Exposures and Annealing for AD562 Analog Devices Parts /1

Test			Spec. Lim. /2		Initial		Total Dose Exposure (kRads)														Annealing		TDE (kRads)		Unbiased		TDE (kRads)	
							10.0		20.0		35.0		50.0		75.0		100		125		360 hours @25°C		150		39 days @25°C		200 /3	
#	Parameters	Units	min	max	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd
1	ICC1	mA	3.0	18.0	10.2	0.5	9.7	0.4	9.6	0.1	9.6	0.1	9.3	0.4	9.3	0.4	9.2	0.4	9.2	0.4	9.4	0.1	9.1	0.4	9.3	0.4	9.2	0.4
2	ICC2	mA	3.0	18.0	10.2	0.5	9.7	0.4	9.6	0.1	9.6	0.1	9.4	0.4	9.4	0.4	9.3	0.4	9.3	0.4	9.5	0.1	9.2	0.4	9.4	0.4	9.3	0.4
3	IEE1	mA	-25.0	-5.0	-14.8	0.4	-14.4	0.1	-13.9	0.4	-13.9	0.4	-13.8	0.4	-13.8	0.4	-13.8	0.4	-13.8	0.4	-13.9	0.4	-13.7	0.4	-13.8	0.4	-13.7	0.4
4	IEE2	mA	-25.0	-5.0	-14.8	0.4	-14.4	0.1	-13.9	0.4	-13.9	0.4	-13.8	0.4	-13.8	0.4	-13.8	0.4	-13.8	0.4	-13.9	0.4	-13.7	0.4	-13.8	0.4	-13.7	0.4
7-16	Iih	µA	-1.0	100.0	0.0	0.2	-0.3	0.05	-0.2	0.1	0.0	0.1	-0.1	0.2	0.0	0.1	-0.2	0.1	-0.2	0.1	-0.3	0.1	-0.2	0.1	-0.2	0.1	-0.1	0.1
18-29	Iil	µA	-200.0	1.0	-5.7	0.2	-19.3	1.3	-25.0	1.5	-24.1	1.0	-23.7	1.2	-26.7	2.0	-20.9	1.3	-21.4	2.4	-14.2	1.6	-17.4	1.9	-22.1	2.8	-16.8	1.9
30	TTL_zero	lsb	-2.0	2.0	0.09	0.01	0.10	0.02	0.12	0.06	0.10	0.01	0.09	0.03	0.10	0.02	0.16	0.06	0.17	0.05	0.11	0.02	0.14	0.07	0.14	0.06	0.25	0.17
31	CMOS_zero	lsb	-2.0	2.0	0.08	0.01	0.09	0.02	0.11	0.06	0.09	0.01	0.08	0.03	0.09	0.02	0.14	0.05	0.15	0.04	0.10	0.02	0.17	0.07	0.12	0.06	0.22	0.15
32	U_Iout	mA	-2.4	-1.6	-2.004	0.0005	-2.005	0.0005	-2.004	0.0005	-2.007	0	-2.006	0.0004	-2.005	0.0005	-2.007	0.0005	-2.004	0.0005	-2.004	0.0004	-2.004	0.0004	-2.004	0.0004	-2.003	0.0004
34	Pss1	lsb	-0.328	0.328	0.035	0.012	-0.001	0.004	0.013	0.051	0.018	0.039	0.009	0.040	-0.003	0.040	0.028	0.018	-0.031	0.025	0.028	0.022	-0.051	0.038	-0.001	0.026	-0.021	0.034
35	Pss2	lsb	-0.328	0.328	0.004	0.001	-0.005	0.001	-0.005	0.002	-0.005	0.001	-0.005	0.002	-0.005	0.002	-0.005	0.002	-0.006	0.002	-0.006	0.002	-0.005	0.003	-0.006	0.002	-0.009	0.006
36	Pss	lsb	-1.310	1.310	0.040	0.018	-0.026	0.020	-0.015	0.022	0.083	0.009	0.074	0.020	0.013	0.020	0.095	0.013	0.021	0.013	0.028	0.015	0.024	0.013	-0.011	0.016	-0.012	0.018
37	LE	lsb	-0.500	0.500	0.047	0.012	0.059	0.008	0.072	0.009	0.082	0.023	0.092	0.029	0.113	0.047	0.110	0.032	0.139	0.062	0.102	0.019	0.126	0.049	0.146	0.047	0.147	0.066
38	DNL	lsb	-0.500	0.500	0.098	0.006	0.120	0.014	0.198	0.038	0.349	0.041	0.525	0.073	0.707	0.220	0.866	0.168	0.958	0.358	0.497	0.170	0.746	0.291	0.823	0.304	1.002	0.339

Notes:

1/ The mean and standard deviation values were calculated over the six parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table

2/ These are manufacturer's pre-irradiation data sheet specification limits. No post-irradiation limits were provided by the manufacturer at the time the tests were performed.

3/ SN 173 suffered a catastrophic failure of TTL_zero and CMOS_zero and they are not included in the calculation of mean and standard deviaiton for clarity.

Radiation sensitive parameters: TTL_zero, CMOS_zero, LE, DNL

TABLE IVb: Summary of Electrical Measurements After Total Dose Exposures and Annealing for AD562 PMI Parts /1

Test			Spec. Lim. /2		Initial		Total Dose Exposure (kRads)														Annealing		TDE (kRads)		Unbiased		TDE (kRads)	
							10.0		20.0		35.0		50.0		75.0		100		125		360 hours @25°C		150		39 days @25°C		200	
#	Parameters	Units	min	max	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd	mean	sd
1	ICC1	mA	3.0	18.0	3.9	0.05	3.9	0.04	3.8	0.05	3.8	0.04	3.8	0.05	3.7	0.03	3.7	0.03	3.7	0.03	3.8	0.04	3.7	0.03	3.7	0.03	3.7	0.03
2	ICC2	mA	3.0	18.0	3.9	0.05	3.9	0.05	3.8	0.05	3.8	0.04	3.8	0.05	3.7	0.03	3.7	0.03	3.7	0.03	3.8	0.04	3.7	0.02	3.7	0.03	3.7	0.03
3	IEE1	mA	-25.0	-5.0	-6.61	0.09	-6.34	0.09	-6.29	0.10	-6.22	0.10	-6.17	0.10	-6.14	0.11	-6.12	0.11	-6.12	0.12	-6.19	0.10	-6.15	0.12	-6.13	0.13	-6.13	0.13
4	IEE2	mA	-25.0	-5.0	-6.41	0.09	-6.37	0.09	-6.34	0.10	-6.28	0.11	-6.24	0.11	-6.21	0.11	-6.19	0.12	-6.20	0.12	-6.25	0.10	-6.22	0.13	-6.21	0.13	-6.13	0.13
7-16	Iih	µA	-1.0	100.0	3/		3/		3/		3/		3/		0.1	0	-0.1	0.05	-0.3	0.05	-0.3	0	-0.2	0.05	0.1	0.05	0.1	0.05
18-29	Iil	µA	-200.0	1.0	-2.3	0.2	-3.6	0	-5.4	0.2	-6.4	0	-6.7	0.2	-8.9	0.2	-8.4	0.3	-8.7	0.2	-7.5	0.8	-6.3	0.2	-8.6	0	-7.7	0.1
30	TTL_zero	lsb	-2.0	2.0	-0.05	0	-0.06	0.005	-0.05	0	-0.05	0.005	-0.04	0.005	-0.05	0.005	-0.05	0.005	-0.04	0	-0.05	0.005	-0.05	0.005	-0.05	0.005	-0.05	0.005
31	CMOS_zero	lsb	-2.0	2.0	-0.06	0.005	-0.06	0.005	-0.05	0	-0.05	0.005	-0.04	0.005	-0.05	0.005	-0.05	0.005	-0.04	0	-0.05	0.005	-0.05	0.005	-0.05	0.005	-0.05	0.005
32	U_Iout	mA	-2.4	-1.6	-2.005	0.001	-2.004	0.002	-2.004	0.002	-2.002	0.001	-2.001	0.0005	-2.000	0.0005	-1.997	0.003	-1.994	0.0005	-1.997	0.003	-1.997	0.003	-1.997	0.003	-1.997	0.003
34	Pss1	lsb	-0.328	0.328	0.023	0.017	-0.006	0.046	0.027	0.059	0.013	0.024	0.029	0.020	0.014	0.003	0.018	0.008	0.032	0.011	0.005	0	0.006	0.007	0.025	0.005	0.017	0.010
35	Pss2	lsb	-0.328	0.328	0.066	0.017	0.059	0.022	-0.026	0.012	-0.007	0.004	-0.002	0.022	-0.019	0.008	-0.012	0.004	-0.024	0.011	0.025	0.011	-0.025	0.001	-0.016	0.001	-0.025	0.006
36	Pss	lsb	-1.310	1.310	0.050	0.007	0.094	0.022	0.042	0.031	0.166	0	0.190	0.052	0.253	0.020	0.117	0.205	0.443	0.066	0.311	0.003	0.269	0.043	0.293	0.027	0.289	0.049
37	LE	lsb	-0.500	0.500	0.062	0.010	0.100	0.006	0.135	0.017	0.267	0.022	0.370	0.008	0.416	0.035	0.588	0.137	1.137	0.488	0.701	0.126	0.752	0.111	0.745	0.108	0.997	0.332
38	DNL	lsb	-0.500	0.500	0.196	0.010	0.282	0.007	0.362	0.052	0.681	0.063	1.071	0.097	1.376	0.092	2.188	0.189	3.508	1.405	2.165	0.282	2.674	0.560	2.668	0.498	3.358	0.948

Notes:

1/ The mean and standard deviation values were calculated over the two parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table.

2/ These are manufacturer's pre-irradiation data sheet specification limits. No post-irradiation limits were provided by the manufacturer at the time the tests were performed.

3/ Due to a programming error in the A540, no measurements of this parameter were taken at this level

Radiation sensitive parameters: LE, DNL

TABLE IVc: Summary of Electrical Measurements After Total Dose Exposures and Annealing for AD562 Biasing Power Supply Current

			Total Dose Exposure (kRads)							Annealing	TDE	Unbiased	TDE
Unit	Setting	Initial	10.0	20.0	35.0	50.0	75.0	100	125	360 hours @25°C	150	39 days @25°C	200
Power Supply 1	+15V	+80mA	+80mA	+80mA	+80mA	+60mA	+60mA	+60mA	+60mA	+60mA	+60mA	+60mA	+60mA
Power Supply 2	-15V	-100mA	-100mA	-100mA	-100mA	-95mA	-95mA	-95mA	-95mA	-95mA	-90mA	-90mA	-90mA
Power Supply 3	+10V	+40mA	+40mA	+40mA	+40mA	+40mA	+40mA	+40mA	+40mA	+40mA	+50mA	+50mA	+50mA