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Subcontractor Report

Commercialization of CIS-Based Thin-Film PV

Final Technical Report
August 1998 – November 2001

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National Renewable Energy Laboratory

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Preface

Siemens Solar Industries (SSI) has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980 [1]. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2 (verified by NREL).

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility using small area test devices and mini-modules. Statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% (verified by NREL) that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules [2].

From September 1995 through December 1998, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module (verified by NREL). During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of $Cu(In,Ga)(S,Se)_2$ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber ($Cu(In,Ga)Se_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm^2) module. During subcontract Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) was delivered to the NREL Outdoor Test Facility. The NREL

measured average efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module [3].

The primary objectives of this subcontract are to scale up substrate size and to scale up production capacity of the baseline SSI CIS-based module process while introducing CIS-based products. The primary goals of this subcontract are to scale the substrate size from approximately 900 cm^2 (1 ft^2) to approximately 4000 cm^2 by the middle of the Phase II, and to achieve pilot production rates of 500 kW per year by the end of Phase III. Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation. SSI will continue mid-term and longer-term thin-film R&D with the goals of:

- Assuring future product competitiveness
- Improving module performance
- Reducing cost per watt
- Assuring product reliability

This document reports on progress toward these objectives and goals through this three-year subcontract (August 1998 through November 2001).

Acknowledgments

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Summary

Compared to traditional wafer-based crystalline silicon technologies, monolithic integration of thin film solar cells can lead to products of comparable performance but with significant manufacturing advantages [1]: lower consumption of direct and indirect materials, fewer processing steps and easier automation. Monolithic integration is required to achieve these advantages since this eliminates multiple process steps and handling operations during formation of the absorber and during module assembly. The basic module elements for all thin-film technologies (alloys of amorphous silicon, cadmium telluride and CIS) are the same; the module elements are a circuit-glass/cover-glass laminate, a frame, and a junction box. The basic circuit elements are also very similar; they each have a base electrode, an absorber, a junction, a top electrode and three patterning steps for monolithic integration. While the details of these module elements or equivalent module elements differ, the basic cost structures are very similar on an area-related basis. Since the cost per unit area is the same, the cost per watt is inversely proportional to the module efficiency. CIS cells and monolithically integrated modules have demonstrated the highest efficiencies of any candidate thin-film technologies; therefore, CIS is expected to have the lowest manufacturing cost/watt.

The primary objectives of the SSI "Commercialization of CIS-Based Thin-Film PV" subcontract were to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. An additional mid- to longer-term objective was to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. The foundation of SSI's approach to process scale-up, process optimization, and demonstration of product durability was the application of design of experiment and statistical process control methodologies. These combined objectives were pursued to fabricate efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. SSI milestones for this subcontract were to:

- Scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) by the middle of the second phase of this subcontract. The criteria for achievement of this milestone was a 4000 cm^2 circuit plate process that had been adopted for SSI commercial activities and was reproducible as determined by statistical process control criteria.
- Achieve a pilot production rate 500 kW per year by the end of subcontract

During this subcontract, SSI applied systematic research, development, production and business methodologies to a carefully planned substrate size and capacity scale-up of CIS-based thin-film technology. These methodologies included Statistical Process Control (SPC), Analysis of Variation (ANOVA), and Design of Experiments (DOE) --- approaches widely recognized as appropriate for manufacturing businesses. SSI also conducted research and development on longer-term issues in support of SSI's ongoing commitment to improve this technology. SSI independently and in conjunction with TFPPP team activities pursued improved understanding of processes, devices, and materials. SSI's role in advancing mid- to longer-term CIS technology emphasizes issues related to commercialization of CIS technology and assured future product competitiveness.

Siemens Solar was the first company in the world to start production of PV modules based on CIS thin-film technology; 5-Watt and 10-Watt modules in 1998. This was a major milestone in the development of PV and, during this subcontract, R&D Magazine recognized the significance of this event by awarding the prestigious R&D 100 Award to the Siemens Solar family of CIS solar modules. NREL, the California Energy Commission and SSI shared this award.

Deliverables for the first subcontract phase were defined as 900-cm^2 (~1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%. The 10-Watt "ST10" module most closely matched this definition. However, activities during the first subcontract period led to the availability of larger commercial products with higher efficiencies than anticipated at the time the deliverables were defined. SSI expanded the CIS product line in 1999 to include 20-Watt "ST20" modules and 40-Watt "ST40" modules. Samples of these commercial products were delivered to NREL during the first subcontract phase. Also during the first subcontract phase, a record-breaking efficiency of more than 12% was verified by NREL for an ST-40 module. This result in 1999 far surpassed the DOE year 2000 goal for a commercial CIS module above 10%.

During the second subcontract phase, SSI delivered 20 ST-40 large area modules, all with efficiencies over 11%, to meet the subcontract deliverables defined as large area modules with efficiencies of over 10%. Also during this subcontract period, the average efficiency based on a Gaussian fit to the main portion of the circuit plate efficiency distribution was increased from 10.8% prior to this subcontract to 11.6% for this subcontract period. This improvement was particularly notable since it was achieved along with an over 300% increase in production volume.

No one major process improvement was responsible for this demonstrated increase in average efficiency accomplished while simultaneously increasing production volume. Instead, these advancements were due to continuous improvement of all process along with particular attention to process research for two critical processes – CIS formation in new large area reactors and the quality of molybdenum deposited in new high capacity sputtering equipment. Judicious application of manufacturing engineering disciplines (statistical process control, analysis of variation and design of experiments) led to a clear definition of near term yield issues. Process development improved adhesion, decreased breakage, addressed control of raw materials, and decreased failures associated with patterning.

Further R&D of all CIS processes for part size and capacity scale-up was pursued during the third and final subcontract phase. Major accomplishments during the third subcontract phase included addressing process issues for implementation of high quality high throughput Mo deposition and patterning, high throughput precursor deposition, and higher throughput reaction of the precursor. Circuit plate production capacity was increased by more than an order of magnitude from the beginning of this subcontract while circuit and module efficiencies were steadily improved. The second subcontract milestone – to achieve a pilot production rate 500 kW per year by the end of subcontract - was first achieved in March of 2001 and the SSI production rate has consistently exceeded this rate since June of 2001.

Demonstrated mechanical and electrical yield enhancements for baseline processing are as important as progress in circuit plate or laminate efficiency. Overall line yield losses have

typically been dominated by mechanical yield. Even so, circuit electrical yield was improved from about 90% to typically above 95% while increasing capacity! During a timeframe representative of the first phase of this subcontract (May through September 1999), overall line yield analyzed on a monthly basis ranged from 32% to 61%. During a timeframe representative of the last phase of this subcontract (January through November 2001), overall line yield ranged from 56% to 89%. This dramatic improvement through the subcontract in both the value and range of monthly yield was the result of addressing disparate special causes. The SSI CIS production process has exhibited good process control for extended periods. Improving yield has been demonstrated even while implementing new equipment, implementing process changes for increased throughput and exploring process changes for improved performance.

These significant subcontract achievements through all subcontract phases were realized by applying systematic research and development methodologies to characterize and improve SSI's CIS process. Subcontract work demonstrated both a viable process for further scale-up and the potential for further performance and yield improvements. Special causes that are inherently encountered as a process evolves were and will continue to be addressed. Progress through multiple cycles of learning has and will continue to be the way to characterize and improve processes for better production compatibility, for improved performance, to scale-up substrate size and for increased throughput.

SSI capabilities were leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. SSI's participation in Team activities focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of eliminating or minimizing their impact. SSI received support from NREL for a broad range of research topics including process development and specialty device and materials measurements. Team activities emphasized research topics common to multiple CIS R&D groups whereas additional collaborations addressed issues that were generally more specific to SSI activities. Both types of collaborations with NREL have greatly contributed to SSI's progress.

NREL also supports SSI through long term testing of arrays and individual modules at the NREL Outdoor Test Facility (OTF). Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over thirteen years. During this subcontract FM and UL approval was obtained for the ST series of products. The performance of the ST family of CIS thin-film products is backed by a 10-year warrantee.

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. SSI achieved all subcontract milestones. The prerequisites for scale up of present processes have been demonstrated. Further device and production R&D can lead to higher efficiencies, lower cost, and even longer product lifetime. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over even longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of further efficiency improvements for future products. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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Introduction

Overview

Multinary $Cu(In,Ga)(Se,S)_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells have exceeded 18% efficiency for devices fabricated at NREL [4]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [5]. During this subcontract (1999) a record breaking efficiency of more than 12% for a commercial large area module was verified by NREL [6] exceeding DOE year 2000 goal for a commercial CIS module above 10%.

Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field-testing for over thirteen years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [5].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [5, 7]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

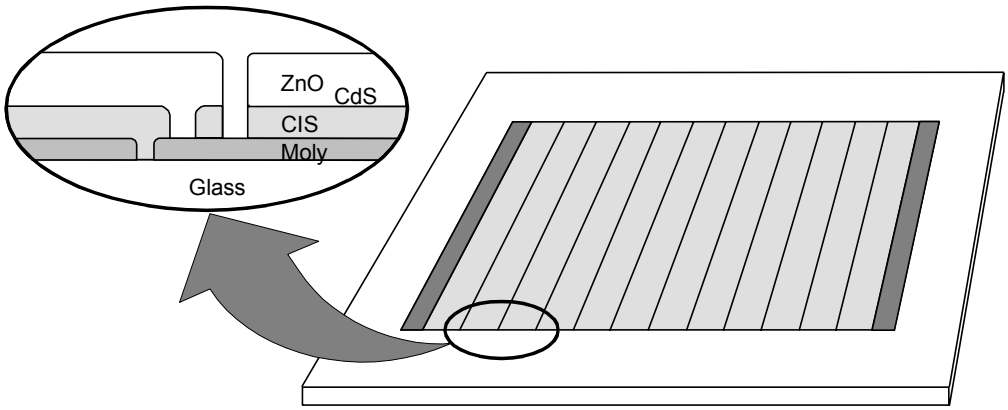

Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [5]. The technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [5]. All thin film technologies have similar manufacturing costs per unit area since they all use similar or equivalent deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme which is for the most part independent of the thin film technology. Costs for alternative encapsulation schemes are typically similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Siemens Solar is approximately 11%. This performance is comparable to many modules based on crystalline silicon, and is substantially better than the performance reported for competing thin-film technologies. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most terrestrial photovoltaic products today are designed to charge a 12-volt battery, however the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically (Figure 1); the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary sodalime window glass, which is cleaned and an SiO_2 barrier layer is deposited to control sodium diffusion and improve adhesion between the CIS and the molybdenum (Mo) base electrode. The Mo base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper, gallium and indium precursors to CIS formation are then deposited by sputtering. Deposition of the precursors occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target (17 at% Ga) and then from a pure indium target. CIS formation is accomplished by heating the precursors in H_2Se and H_2S to form the CIS absorber. Beginning at room temperature, furnace temperature is ramped to around 400ºC for selenization via H_2Se, and ramped again to around 500ºC for subsequent sulfidation via H_2S, followed by cool-down to room temperature. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to

as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer" layer. A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a "window layer" or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

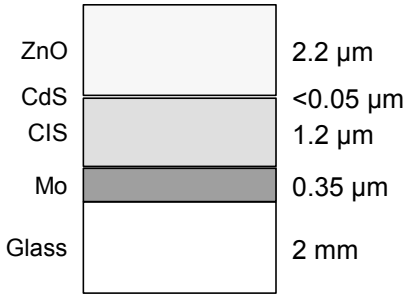

Figure 2. Structure of SSI's CIS cell structure (not to scale).

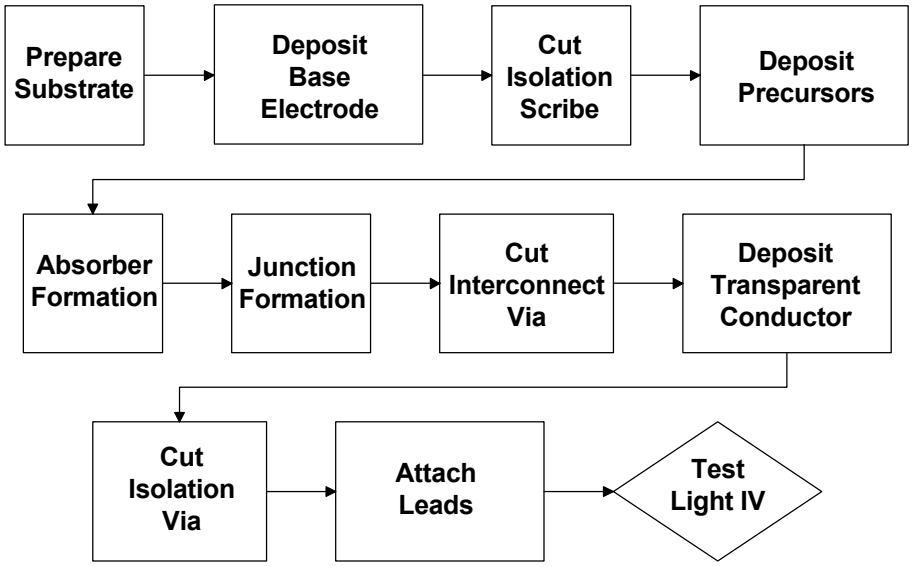

Figure 3. SSI CIS Circuit Processing Sequence.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher Ga concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 4. Efficiency, voltage, and adhesion improvements have been reported for the SSI graded absorber structure [2, 8, 9].

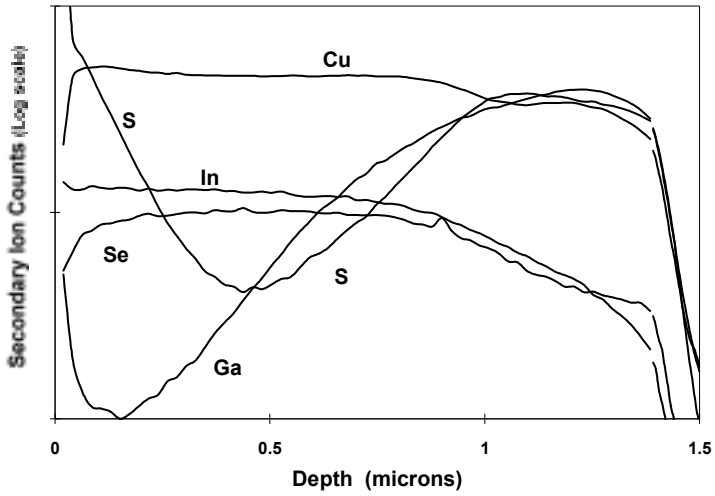

Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 5 illustrates the module configuration used for prototypes and ST products during this subcontract period [3]. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

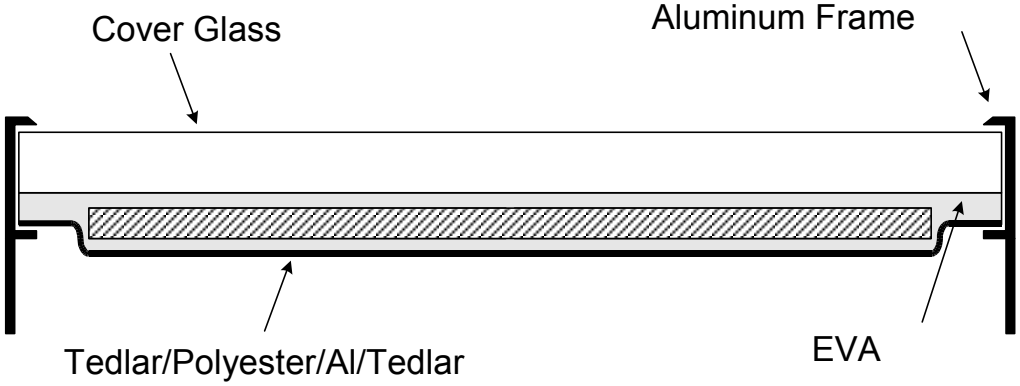

Figure 5. Single circuit plate module configuration with a TPAT backsheet.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using device structures that exercise all aspects of large area module production [10]
- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [11, 12].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed. Communication of this progress is typically best expressed in the language of the SPC discipline [13]. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability measured using the SPC discipline and compared to a predictable baseline process. Confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA to demonstrate statistically significant results.

Subcontract Activities and Milestones

The primary work of this subcontract is to advance module fabrication processes by progressively scaling substrate size and capacity for the SSI baseline CIS circuit-plate process. Simultaneously, SSI is pursuing understanding of the impact of circuit plate and module fabrication processes on device performance and module reliability. Understanding and optimization of the these processes is based on the application of DOE and SPC methodologies to identify dominant process issues and address process specific topics. Five subcontract activities have been defined to support this work:

Substrate Size Scale-up – The primary emphasis for this activity is to progressively scale substrate size from approximately 900 cm^2 (1 ft^2) approximately 4000 cm^2 (4 ft^2).

Capacity Scale-up - The technical base supporting manufacturability will be advanced as the production capacity is increased to about 500 kW/yr.

Product Durability - SSI will continue package development and qualification in parallel with substrate size and capacity scale up.

Environment, Safety and Health (ES&H) - SSI will continue internal programs and collaborative efforts such as with the TFPPP ES&H team to safely produce CIS-based

devices and modules and to explore technical approaches for removing and recycling module components.

Process Improvements – This task emphasizes advancement of the technical base supporting manufacturing as SSI scales up substrate size and capacity. SSI capabilities are leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics.

Milestones

SSI milestones for this subcontract are to:

- Scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) by the middle of the second phase of this subcontract. The criteria for achievement of this milestone is a 4000 cm^2 circuit plate process that has been adopted for SSI commercial activities and is reproducible as determined by statistical process control criteria.
- Achieve a pilot production rate of 500 kW per year by the end of this subcontract

Deliverables

The following deliverables have been defined for each phase of this subcontract.

Phase I

D1. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D2. End of the 12th month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Phase II

D3. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.

D4. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Phase III

D5. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12%.

D6. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12% for the NREL Module Testing Team.

Technical Review

Large Area Circuit Fabrication

Circuit Plate & Module Statistics

Circuit plate statistics representative of the beginning of this subcontract were compiled using data from a few months before and the early portion of this subcontract (Figure 6, Figure 7). During that time frame (January through November 1998), about 1300 ~30x120 cm circuit plates were produced including 18% that were dedicated to experiments [3, 14].

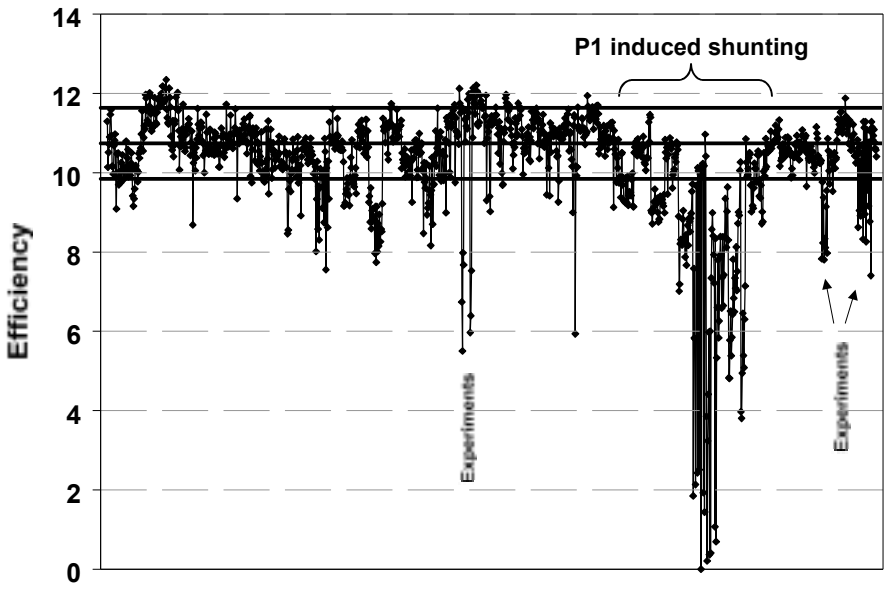

Figure 6. CIS Circuits Produced January through November 1998 (abscissa – module identifier).

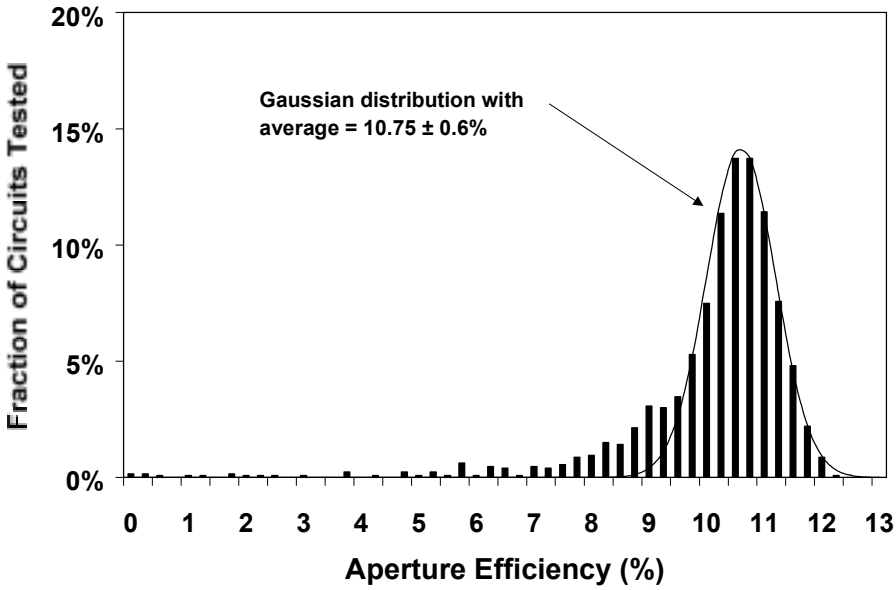

Figure 7. CIS Circuit Efficiency Distribution - January through November 1998.

This process data demonstrates generally good control for extended periods with an average efficiency of 10.8% based on a Gaussian fit to the main portion of the distribution. Periodic shifts in the short-term average efficiency between about 10.25 and 11.25 resulted from shifts in V_{oc} and FF that were related to batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser scribed pattern lines in the Mo base electrode resulted from batch-to-batch variability in base electrode preparation.

Similar data representative of the first phase of this subcontract is presented in Figure 8 and Figure 9. This timeframe corresponds with the SSI fiscal year (October 1998 through September 1999) and there is some overlap with the data presented in the previous charts. An average efficiency of 11.2% is demonstrated for 3,030 circuit plates.

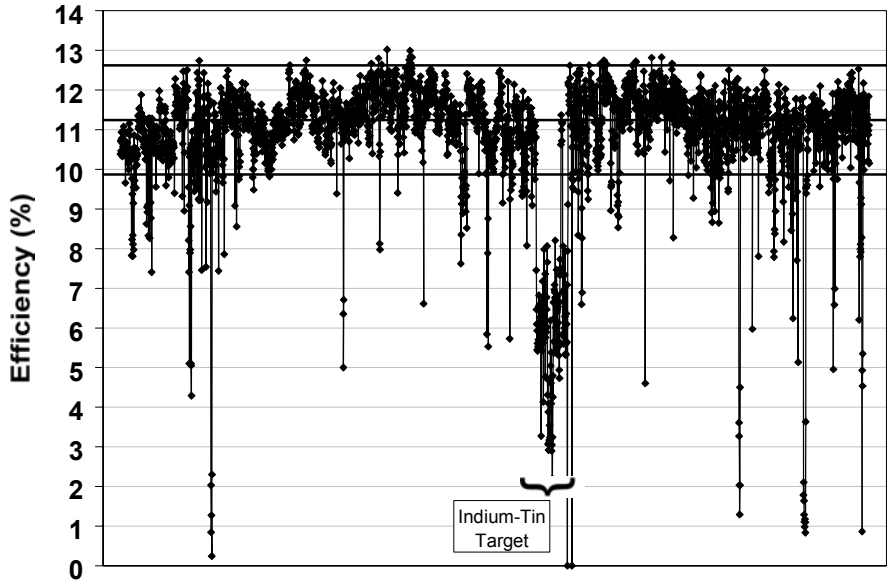

Figure 8. CIS Circuits Produced October 1998 through September 1999 (abscissa – module identifier).

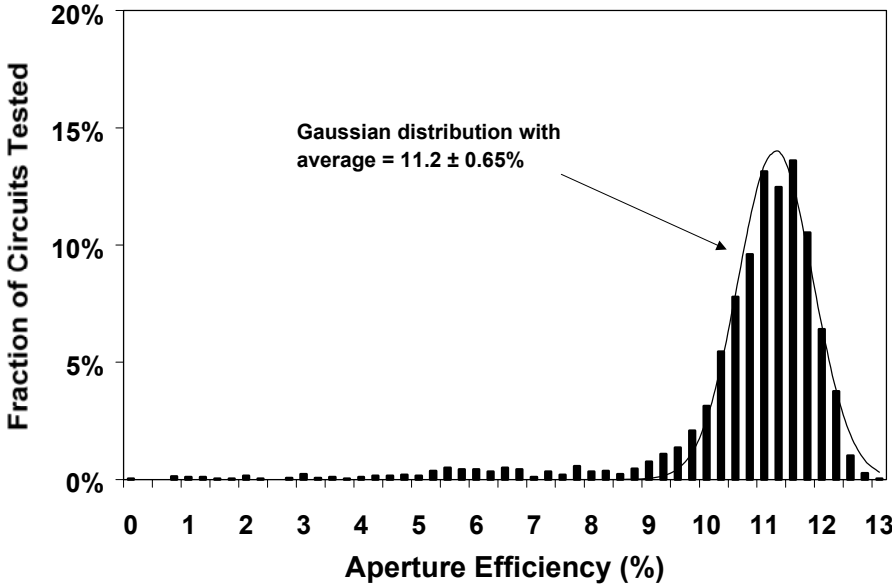

Figure 9. CIS Circuit Efficiency Distribution - October 1998 through September 1999.

This process data also exhibits generally good control for extended periods. The average efficiency based on a Gaussian fit to the main portion of the distribution increased from 10.8% to 11.2% in part due to better overall process consistency and in part due to changes in the reaction process. Small periodic shifts in the short-term average efficiency continued due to shifts in V_{oc} and FF resulting from batch-to-batch variability in precursor or base electrode preparation. Process development eliminated or greatly reduced periodic shunting along the laser scribed pattern lines. With the exception of identified special causes for irregular performance such as bad raw materials, 87% of the circuit plates were above 10% efficiency. Also during this timeframe, NREL confirmed a world-record 12.1 percent conversion efficiency for a large area (3651 cm^2) CIS module.

Progress during the second subcontract period (September 1999 through August 2000) included production volume increases of over 300% while also improving efficiency. Circuit plate data representative of the second subcontract period is presented in Figure 10. Efficiency improvements are again demonstrated with a peak in the Gaussian fit at 11.6%. Generally good process control is again demonstrated. The production distribution of modules (Figure 11) is sharply peaked at nearly 11% efficiency with a full width of only ± 0.5%.

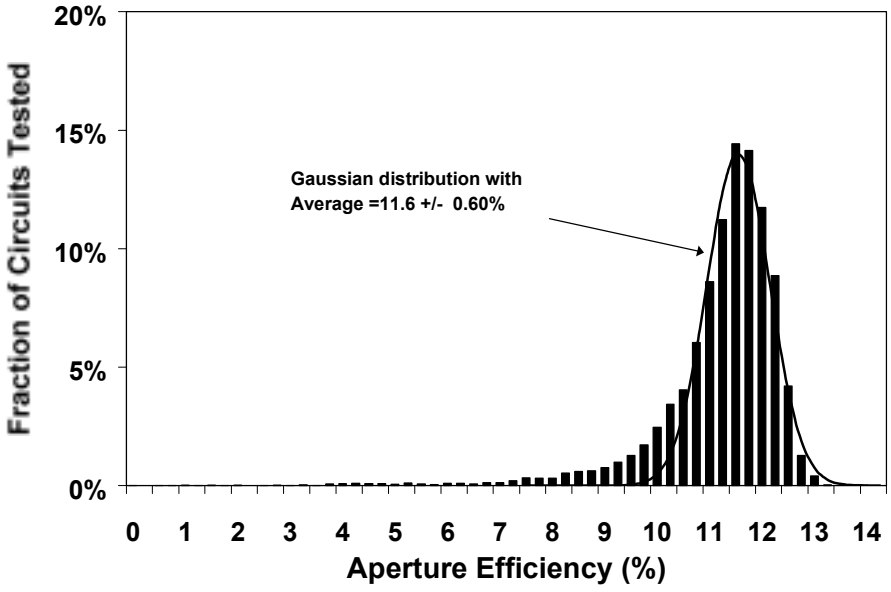

Figure 10. CIS Circuit Efficiency Distribution - September 1999 through August 2000.

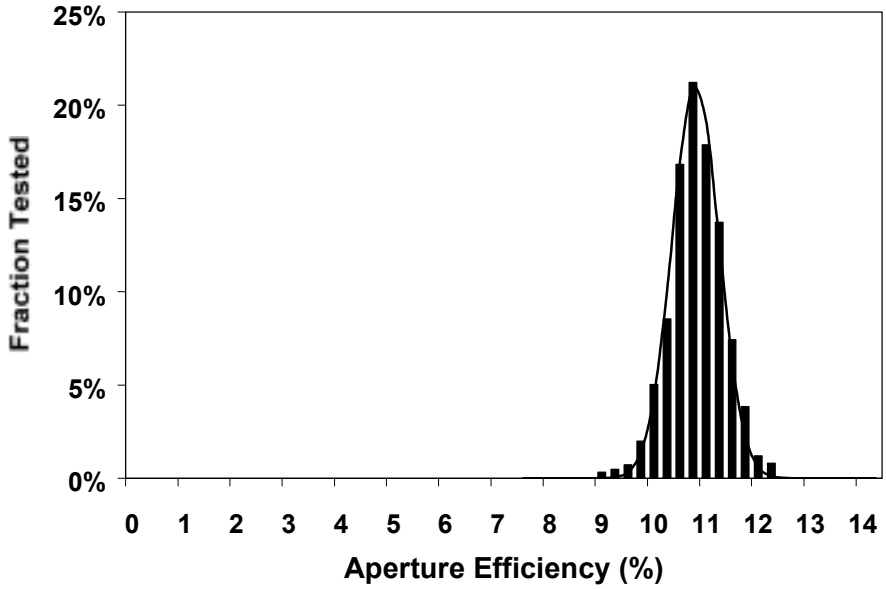

Figure 11. Module production distribution - September 1999 through August 2000.

The distribution of production modules representative of the end of this subcontract (January through September 2001) is presented in Figure 12. The distribution includes data for 7583 laminates for a cumulative power of 292 kWp. The distribution is sharply peaked at nearly 11%. The peak of a Gaussian fit to the main portion of the distribution is at 10.6% with a standard deviation of 0.50%; the full width of the distribution is only 9% of the average.

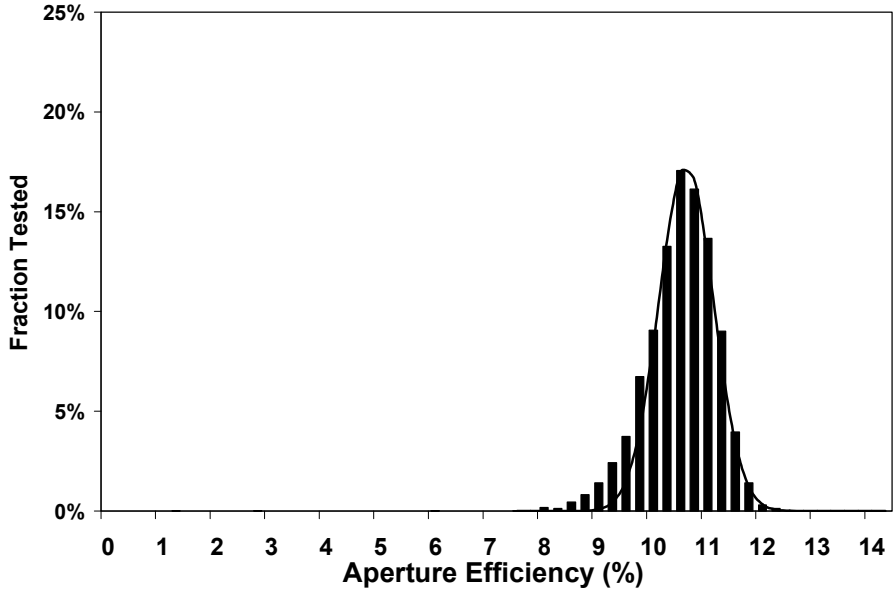

Figure 12. Module production distribution - January through September 2001.

As summarized in the following table (Table 1), circuit plate production capacity has increased by more than an order of magnitude since the beginning of this subcontract while also improving circuit and module efficiencies. Initially lower performance when using new absorber formation reactors and new precursor sputtering equipment is responsible for the slightly lower efficiency and slightly broader distribution during the third phase relative to the second phase of this subcontract. Process development for new equipment and increased production capacity is discussed in later sections.

Table 1. Circuit production capacity and efficiency progress.

Year	Module Production (kW)	Average Aperture Efficiency	
		Unlaminated Circuit	Laminated Module
97-98	15	10.8%	10.3%
98-99	68	11.2%	10.7%
99-00	294	11.6%	10.9%
00-01	486	10.9%	10.6%

Mechanical and electrical yield progress for baseline processing is as important as progress in circuit plate or laminate efficiency. Mechanical yield is defined as the fraction of all glass substrates originally introduced into the baseline circuit production sequence which then successfully pass all intermediate inspection criteria and are IV-tested. With this definition, mechanical yield quantifies the rejection of substrates for failures such as glass breakage, film scratches, or out-of-specification process runs. Overall line yield is the combination of mechanical and electrical yield and, since electrical yield is very high, the overall line yield is primarily limited by mechanical yield. During a timeframe representative of the first phase of this subcontract (May through September 1999), overall line yield analyzed on a monthly basis ranged from 32% to 61%. During a timeframe representative of the last phase of this subcontract (January through November 2001), overall line yield ranged from 56% to 89%. This dramatic improvement through the subcontract, although non-monotonic, was the result of addressing disparate causes of primarily mechanical losses.

Electrical yield is more subjective since it depends upon the choice of a lower specification limit. For example, at 10% minimum circuit efficiency, the yield of non-experimental circuits for the January through September 2001 timeframe (Figure 12) is 84%; at 9% minimum, the yield was over 98%. Electrical yield has been generally high throughout the subcontract with the exception of identified special causes that lowered yield for typically less than one month. Most

production modules have efficiencies above 10% and the overall electrical yield of the CIS production line at the end of this subcontract is nearly 98%!

Yield data for two timeframes, either of which could be considered representative of the end of this subcontract, is presented in the following table (Table 1). Electrical yield is high for both timeframes while the mechanical yield varies. Notably, the relative importance of mechanical loss mechanisms varies for the two timeframes. For example, operator error appears as one of the loss mechanisms exceeding 1% for the first timeframe and not for the second. Similarly, the equipment failure category typically includes failures of different equipment during different timeframes. Pealing is a loss mechanism that appears in both timeframes. Multiple process parameters that impact pealing were identified during this subcontract and process research and development mitigated but did not eliminated peeling losses. These are examples of the disparate special cause loss mechanisms that were addressed throughout this subcontract. Efficiency and yield advancements made during this subcontract are the result of production research and development through multiple cycles of learning.

Table 2. Yield data for two timeframes representative of the end of this subcontract.

	June 2000 through mid August 2001		September 2001 through January 2002	
Line Yield	64%		83%	
Electrical Yield	92%		99%	
Mechanical Yield	72%		84%	
Mecanical Losses				
	Equipment failure	5.3%	**Broken**	3.7%
	Broken	4.9%	**Equipment failure**	2.9%
	Film peeling	4.1%	**Bad snap**	1.9%
	Scratch	3.1%	**Film peeling**	1.7%
	Operator error	1.6%	**Scratch**	1.4%
	Bad snap	1.2%		
	Lamination bubble	1.1%		
	All others	4.4%	**All others**	2.6%

Process Development Examples

This section and the following section titled "Module Packaging and Product Durability" will present examples of subcontract work with emphasis on major subcontract activities and collaboration with NREL. Examples are included for all major process steps. SSI's participation in the National CIS R&D Team is discussed in a later section. Team activities emphasized research topics common to multiple CIS R&D groups whereas the collaborations discussed in this section are generally more specific to SSI activities. Both types of collaborations with NREL have greatly contributed to SSI's progress. The following examples present an overview of subcontract technical accomplishments that were achieved while addressing substrate size and capacity scale-up, pursuing efficiency and yield advancements, and applying process research and development to identify special causes for process variation.

A major loss in production was caused by a serious quality lapse by the H_2Se supplier. Instead of H_2Se, the supplier delivered a cylinder, and subsequently yet another cylinder, of a gas with a much higher vapor pressure. This triggered overpressure relief valves, contaminated gas lines, interrupted production, and resulted in a general interruption of ongoing development activities. Another major loss of circuit plates occurred due to a similar problem with supplied materials. An indium-tin target was supplied instead of an indium target. Poor circuit performance resulted from this inadvertent test of changes in the relative concentrations of precursors and the addition of tin. These events introduced materials with extreme differences from specified materials and illustrated the vigilance required in obtaining the proper materials to achieve high yield.

In addition to being a process issue, the overpressure of gas lines was a potential safety issue. As part of SSI's efforts to promote safe operations throughout the photovoltaics community, SSI communicated results and insights regarding this incident to the photovoltaics community through the leaders of the TFPPP ES&H Team, Paul Moskowitz and Vasilis Fthenakis.

Process development for new absorber formation reactors was a major subcontract activity. In additional to first order requirements such as reasonable temperature uniformity within the absorber formation reactors, the importance of reactor design to the CIS formation process was demonstrated when first scaling from a baseline process in small area reactors to a large area reactor. SSI demonstrated that differences between baseline and the first large area absorber formation reactor design were responsible for differences in absorber layer properties and cell performance. These differences were isolated to differences in the materials of construction and the physical design of the large reactor. As a result of these studies and advances in understanding the influence of reactor design on performance, SSI designed and built a new large area reactor (the prototype large area reactor) based on a more direct scale-up of the baseline reactor. Success with this development effort was demonstrated by comparable performance for baseline and large area circuit plates.

During this subcontract, new production reactors were procured, process development for these reactors was begun and the reactors were ultimately qualified for production. Circuit plate production was increased even though more R&D resources than anticipated were expended on process development for new reactors. Implementation of the new reactors was delayed by late delivery from the equipment vendor. These reactors exhibited poorer reliability than the prototype large area reactor. A longer than anticipated process development cycle was required to qualify the reactors for production. Efforts throughout particularly the second and third

subcontract phases addressed warping and poor CIS to Mo adhesion for some plate locations within the reactors while simultaneously developing processes for increased circuit plate load.

The following is an example of reactor process development efforts in collaboration with NREL to characterize the potential dependence of device performance on reactor position. Small devices fabricated by NREL on completed SSI devices (processing through ZnO at SSI) were used to characterize the potential dependence of device performance on reactor position for one of SSI's newer large area reactors. Performance versus temperature and position were analyzed using typical IV measurements (Eff, Voc, Jsc, FF).

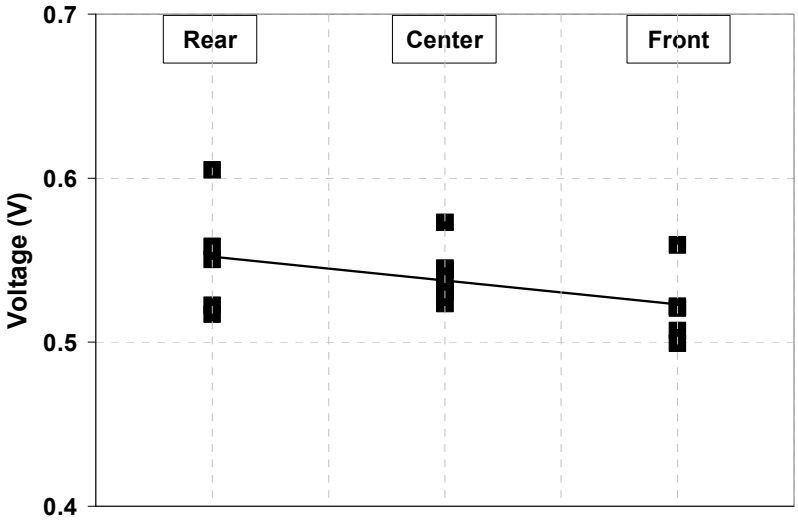

Figure 13. Dependence of Voc on reactor position.

In addition, NREL-supplied quantum efficiency data was used to generate a measure of the potential dependence of bandgap on reactor position. The intercept on the energy axis of the square of quantum efficiency versus photon energy is taken as a measure of optical bandgap. This bandgap data is actually a qualitative measure of device structure since the measured bandgap is a convolution of the affects of absorption and collection through the varying bandgap structure of these absorbers. As with Voc, these bandgap measurements indicate a difference in the absorber structure dependent on position within the reactor; in this case, a statistically significant increase in bandgap from front to rear within the reactor is observed.

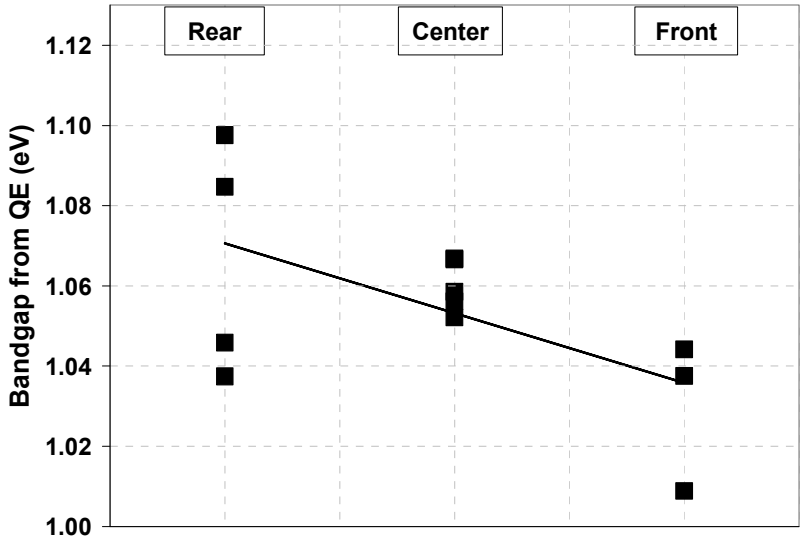

Figure 14. Dependence of bandgap on reactor position.

Temperature variations within the reactor are known from measurements using multiple thermocouples to profile temperatures throughout the reaction process. Although both Voc and bandgap are dependent on position within the reactor, there is no correlation between these parameters and the local temperature within the reactor. As when scaling from a baseline process in a small area reactor to the prototype large area reactor, this data implies that the local environment within the reactor, beyond simply the local thermal history, has an impact on the device structure and performance.

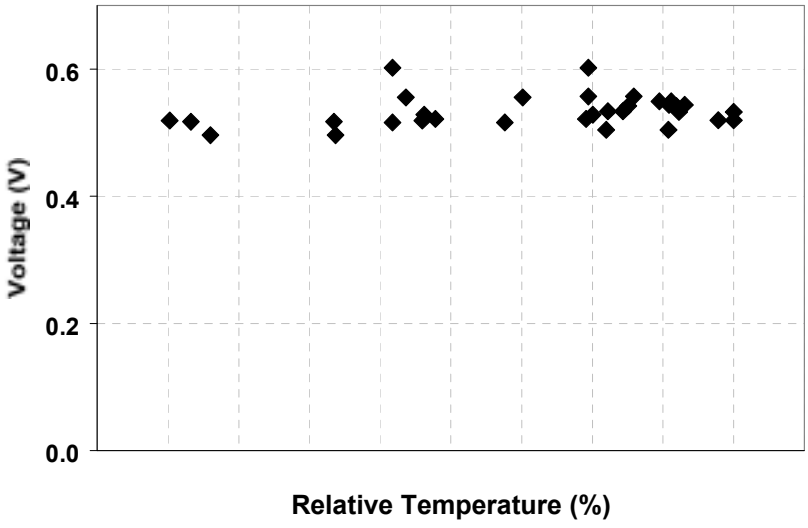

Figure 15. Lack of correlation between Voc and local temperature within the reactor.

Process development related to Mo deposition and the absorber formation process is another example of collaborations between NREL and SSI. SIMS and AES analysis support from NREL [15] was obtained for samples with a factor of two difference in the Mo thickness processed in both a large area reactor and a small area reactor. Minimal differences were seen in the elemental profiles of the major constituents (Cu, Ga, In, S, Se) for the two Mo thicknesses. With the exception of features that are assumed to be anomalous, the samples also exhibit minimal differences in the elemental profiles of the minor constituents. If observed differences by a factor of two to three in sodium and potassium are significant, the differences correlate with the reactors rather than the Mo thickness. The SIMS data set indicates anomalously high O_2 in one sample; however, the Auger data indicates that this high value is still below 1 to 2 atomic percent. The SIMS data also indicates a high Ca concentration in one sample. However, this signal is probably the result of contamination after formation of the absorber since the Ca profiles for all other samples but this sample exhibit structure in the Ca profile that parallels structure for other elements in the graded absorber. Results of this collaboration resulted in support for the decision to decrease Mo thickness and hence increase the capacity of Mo deposition equipment.

Subcontract work first with equipment existing at the start of this subcontract and then with new equipment led to predictable Mo deposition and P1 scribing processes for high throughput processing of large substrates. Process development with existing equipment demonstrated the impact of Mo deposition conditions on laser patterning and the dependence of scribe quality on laser patterning parameters. Through additional cycles of learning, process development for new Mo deposition equipment first demonstrated a process that permitted quality P1 scribes but with limitations on the number of plates that could be consistently processed. Additional process development led to another process modification that mitigated the limitation on the number of plates that could be consistently processed.

Prior to this subcontract work, shunting along laser P1 scribes sporadically caused poor performance. Studies of the interdependence of Mo properties and laser processing using existing equipment were conducted to address this issue. Studies to determine if laser scribing of Mo is affected by a background of O_2 during Mo deposition is an example of this process development. Mo was sputtered with no O_2 (baseline) and with O_2 flowing at 1% and 10% of the Argon flow. Figure 16 illustrates that the visual appearance of scribes is not dramatically affected by 1% O_2 but is distinctly affected by 10% O_2 - the Mo deposited with 10% O_2 is not completely removed. A similar trend was observed for mini-module performance. Performance differences between baseline and a 1% partial pressure of O_2 were not statistically significant for the relatively small number of devices processed. The modules made with Mo deposited with a 10% O_2 background could not be tested since the modules did not have complete P1 scribes.

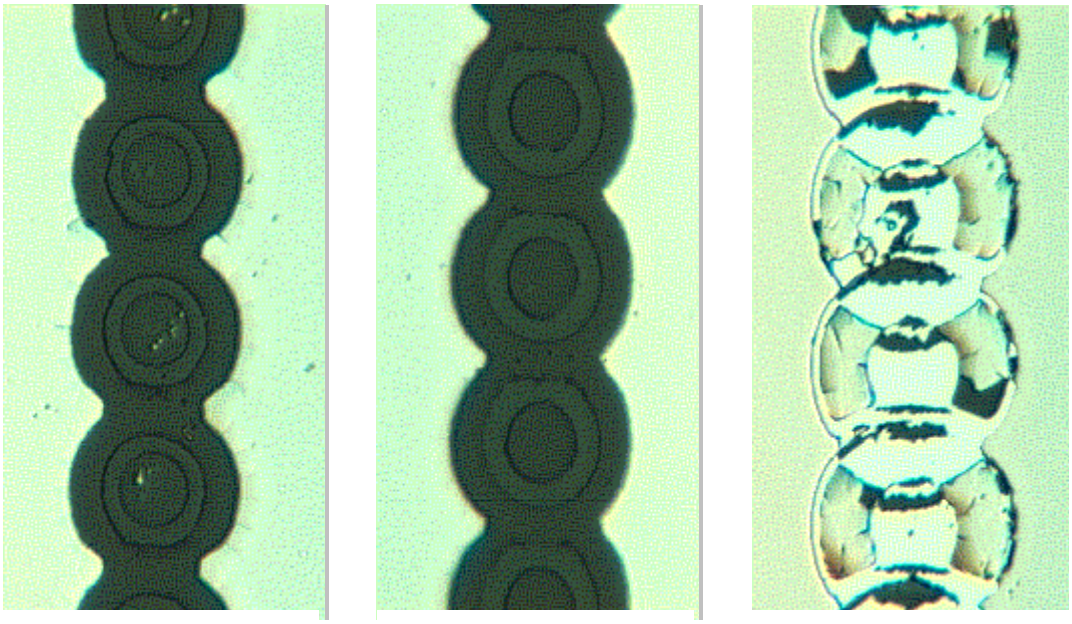

Figure 16. The dependence of Mo scribe appearance on background O_2 during Mo deposition.

Studies of the impact of laser scribing parameters on scribe quality were also conducted. The following figure (Figure 17) represents the major features in Mo that has been affected by an individual laser pulse. A P1 scribe is generated by repeating this interaction forming multiple craters with an offset between adjacent craters. Mo is removed to a radius of R1. The Mo has been affected without removal in the region between R1 and R2 - referred to as the "affected Mo region."

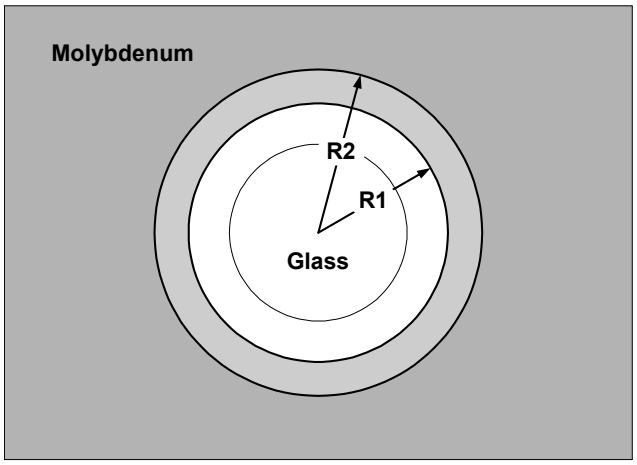

Figure 17. Diagrammatic representation of the effect of an individual laser pulse.

Laser processing studies indicated that the dimensions of the region where Mo is removed are predictably modeled by laser parameters. Correlation between Mo deposition process

parameters and the extent of the affected Mo region were also demonstrated. The following summarizes the results of these studies and observations:

- The baseline process is not critically sensitive to laser focus – the process depth of field is large relative to normally encountered variations in substrate surface position.
- Removal of Mo by a laser pulse is hindered by the presence of the affected Mo region from previous pulses; the presence of the affected Mo region can interfere with continuously connecting well-formed craters to achieve electrical isolation.
- Shunting can be caused by an extensive affected Mo region.
- The extent of the affected Mo region is dependent on Mo properties and laser parameters such as the relative dimensions of the laser beam. This is illustrated in the following chart (Figure 18), which demonstrates monotonically increasing relative dimensions of the affected Mo region as a function of the relative dimensions of the laser beam.
- Variations in quality of the laser-produced pattern are related to variations of the properties of Mo across 1x4 ft. substrates and batch to batch variations in Mo properties.

These Mo deposition and laser parameter studies resulted in the definition of predictable Mo deposition and P1 process for existing equipment.

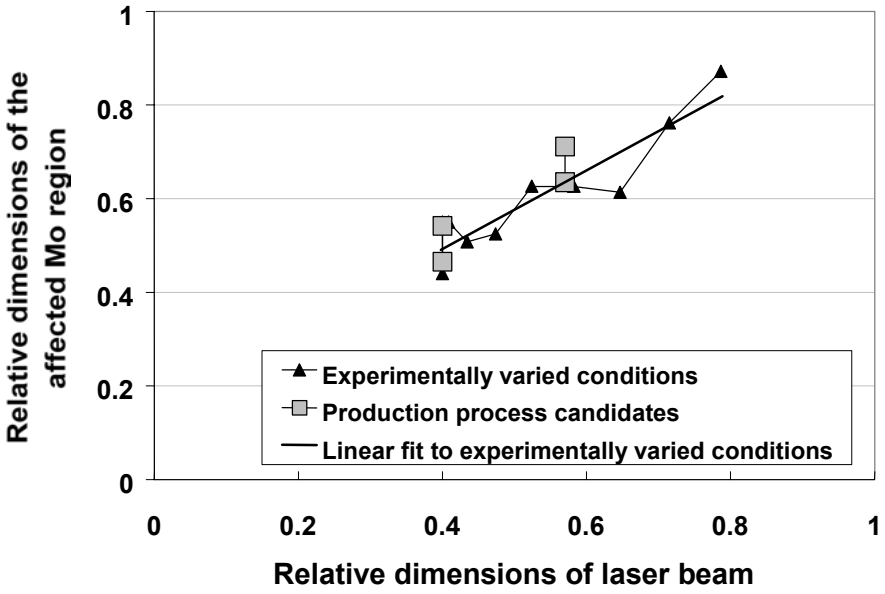

Figure 18. Relative dimensions of the affected Mo region versus normalized laser beam dimensions.

Initially, Mo deposited in a new high capacity sputtering system exhibited poor quality P1 scribes; craters had a more extensive affected Mo region. The following figure (Figure 19) illustrates scribes for Mo deposition conditions leading to poor and high quality P1 scribes. The

image on the left illustrates a poor quality scribe with an extensive affected Mo region. Based on process development using the older equipment, Mo deposition process modifications were made for the new sputtering system and consistently produced quality scribes were demonstrated. This process was adopted by production; however, at the expense of process complexity and process drift that limited throughput. Additional process options were explored and another unique sputtering process was developed. This led to generally well controlled and uniform patterning even at higher throughput.

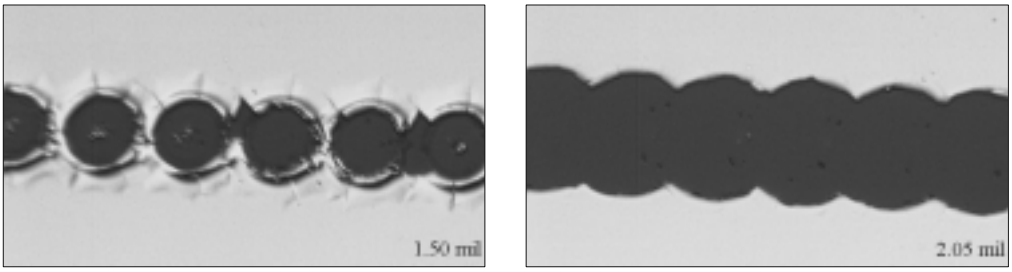

Figure 19. Laser scribes for Mo deposition conditions leading to poor and high quality P1 scribes.

The laser processing discussed for first existing equipment and then new equipment illustrates the importance of multiple cycles of learning in production R&D. R&D to quantify the dependence of scribe quality on laser parameters and Mo deposition conditions was necessary to evaluate sporadic shunting along laser P1 scribes. The know-how derived from these studies in existing equipment was applied to process development for new high throughput production equipment when defining the first process for this equipment. Continuing experience with this process while scaling up production capacity illuminated process complexity and process drift issues that limited throughput. Additional process options based on previous experience were explored and another unique sputtering process was developed. These multiple cycles of learning led to a production qualified high throughput Mo deposition process for the new sputtering equipment and improved circuit electrical yield from about 90% to typically above 95%!

As an example of subcontract activities that did not lead to improvements in the baseline process, an etching technology used in the printed circuit board industry was tested as an alternative to laser scribing. The goals of this study were to demonstrate the process, compare shunting along P1 for laser ("L-P1") and etched ("E-P1") patterning, and demonstrate simultaneous processing of P1 and a wide Mo free border. The Mo free boarder is important for alternative module encapsulation configurations. The E-P1 process was tested in the full module fabrication process and physical features unique to the E-P1 process were analyzed with the help of NREL resources. Smaller than typical circuit plates (~30x30 cm) were used to accommodate available equipment.

The visual appearance of E-P1 scribes motivated analysis of scribe features. A very thin transparent and insulating layer remains within some etched P1 scribes. Also, a narrow strip is present at the edge of all lines that appears to be similar to the thin layer. NREL supplied SEM

micrographs of E-P1 scribe features (Figure 20) and Auger and XPS analysis [16]. Features are numbered as follows in the SEM:

1	- Mo
2, 3, 5, 6	- thin transparent layer
4	- center of the E-P1 scribe

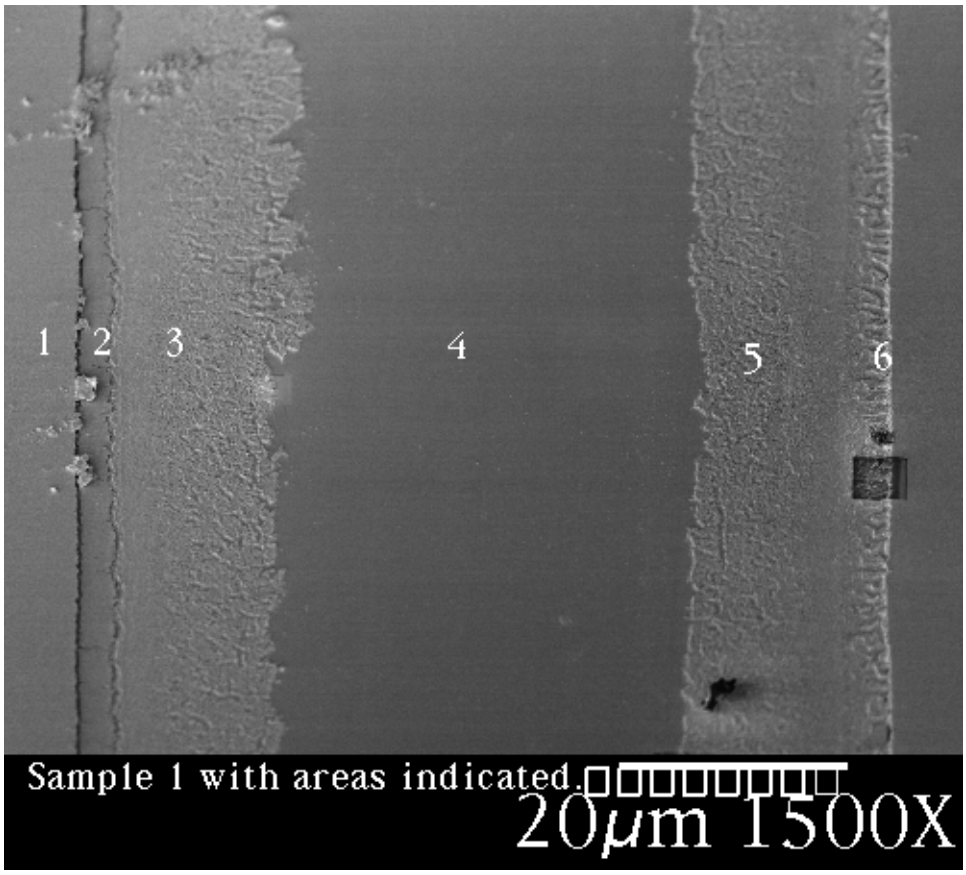

Figure 20. NREL supplied SEM of an etched P1 isolation via.

Auger analysis was complicated by sample charging; however, charging was less of a problem for area 2 than areas 3 through 5 since area 2 is close to the Mo. The following elements were identified for the areas labeled 1 and 2 on the numbered SEM.

Area 1; On the Mo	Mo, C, O
Area 2; On the transparent insulator	Mo, C, O, Ca, N, Fe

NREL also used XPS analysis however the dimensions of the probe beam are larger than the scribe width. Table 3 summarizes the results:

Table 3. XPS analysis of an etched Mo isolation scribe (percent concentration).

Analysis Area	C	O	Mo	Na	Ca	Si	S
Mo	57	25	16	1	1	0	0
Scribe including some Mo	60	23	12	1	trace	2	1

Module performance results are summarized in the following module power chart (Figure 21). The distribution of power for circuit plates with L-P1 is ~4 points better than the distribution for E-P1 and the difference is statistically significant. Differences in FF explain the majority of this difference. No definite but several possible causes for the low performance, including the analyzed narrow strip at the edge of all lines, were determined by observing circuit plates. It is assumed that elimination of these relatively small differences would be possible with in-house process development. The potential advantage of an E-P1 process for reducing sporadic shunting along P1 was not demonstrated since poor adhesion along P1 was not observed for either process during the time frame of this experiment. This alternative to isolation scribes produced with a laser was not adopted due to simultaneous improvements in the laser P1 process and commercialization issues for the etch process.

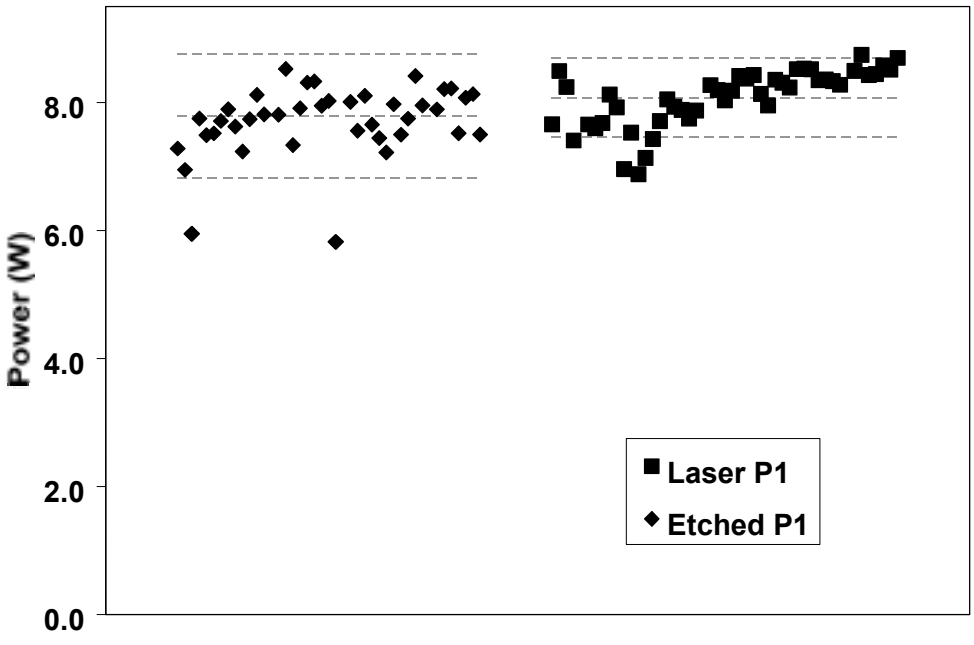

Figure 21. Module performance for laser and etched Mo patterning (abscissa – module identifier).

As another example of SSI/NREL collaborations, analysis at NREL [17] was particularly helpful in SSI's continuing efforts to identify the source of scratches. Scratches degrade performance and it is relatively easy to inspect just degraded modules and at times find scratches. However, it is difficult to inspect all large area modules during each stage of processing to determine when the scratches occur. Figure 22 is an optical micrographs illustrating a scratch across the interconnect patterns (patterns 1, 2 & 3). Acetic acid was used to remove the ZnO electrode. Similar CdS depositions are expected in the scratch and in pattern 2 if the scratch occurred before CdS deposition. EDS analysis did not find evidence of CdS in the scratch. This implies that, at least for this particular scratch, the scratch occurred after CdS deposition and before ZnO deposition.

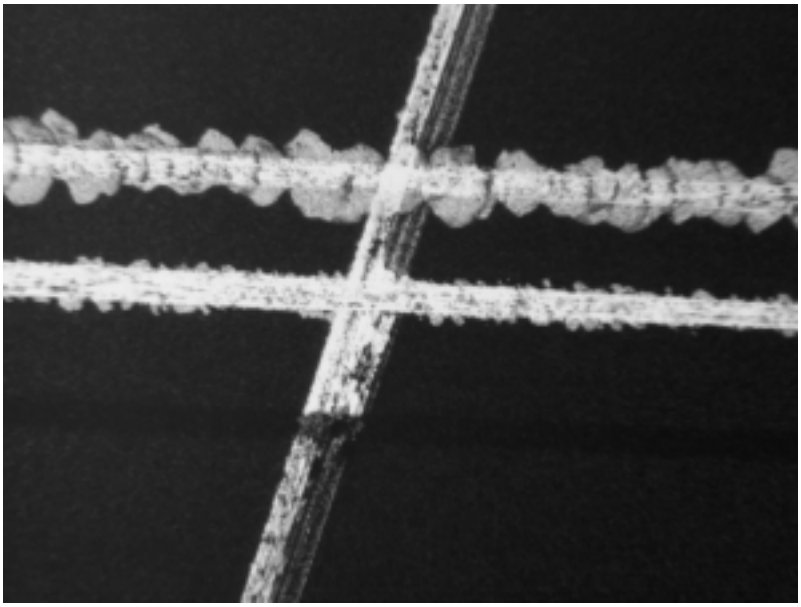

Figure 22. Optical micrograph of a patterned and scratched area analyzed by NREL.

Significant improvements in control of the precursor deposition process were made during this subcontract period [18]. Precursor sputtering diagnostics characterize and lead to the control of the absorber thickness and the Cu/(In+Ga) ratio (CIG ratio) which are critical parameters in production of high efficiency CIS devices. Deposition of the metallic elements of CIS on production substrates occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target (17 at% Ga) and then from a pure indium target. The deposition rate of each target is measured using a modified quartz crystal technique; a quartz crystal is run through the sputtering system twice, the first pass for deposition of the copper-gallium film only, and the second for the indium film only. The resonance frequency of the quartz crystals is measured outside the vacuum system before and after each deposition pass and the thickness of copper-gallium and indium layers are calculated based on frequency differences before and after the depositions.

A set of 10 crystals is distributed across a substrate to characterize the uniformity of deposition across the substrate width. This is especially important since a shift in deposition uniformity for

either deposition can lead to regions of unacceptable CIG ratio even when the average composition appears acceptable. This measurement procedure is executed at the beginning of each production run to set the sputter rates within specifications. The measurement procedure is then repeated after a run of substrates for production. These pre- and post-run deposition rate data are the basis for production process control. A model including the effects of changes in sputter rate with target age predicts how sputter rates and thus CIG ratio drifts during a run of substrates. This model is applied to define the maximum duration for a run of substrates and determine when it is appropriate to change targets [18]. Subsequent R&D indicated that the process control parameters derived in this way are unique to a particular sputtering system.

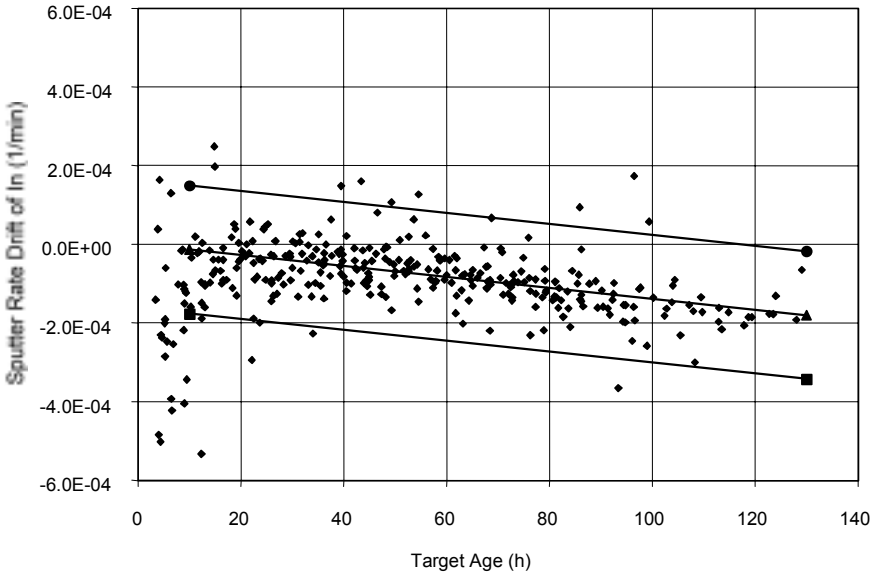

Figure 23. Indium sputter rate drift.

Process development for new high throughput base electrode and precursor sputtering equipment (Figure 24) was required to achieve circuit plate performance similar to the performance for precursors deposited using older and lower throughput equipment. Initial results for precursors from the new sputtering system indicated lower efficiencies primarily due to lower FF. NREL assisted with this process development by supplying SEM and Auger depth profile analysis of precursors from the two sputtering systems. As illustrated in Figure 25, precursor surface morphology differences were observed. Auger analysis (Figure 26) indicates that the achieved elemental depth profiles are independent of the sputtering system used to deposit the precursors. This development work led to a process in the new high throughput base electrode sputtering equipment that achieves FF's similar to (within 4%) results from the older equipment.

Figure 24. New high throughput base electrode and precursor sputtering equipment.

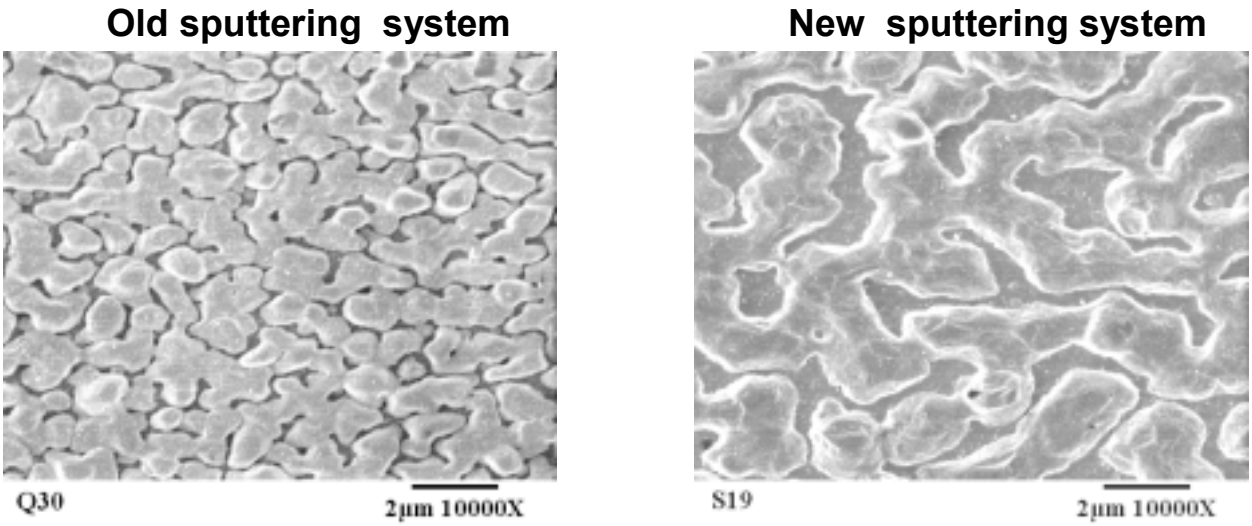

Figure 25. Precursor morphology dependence on sputtering conditions.

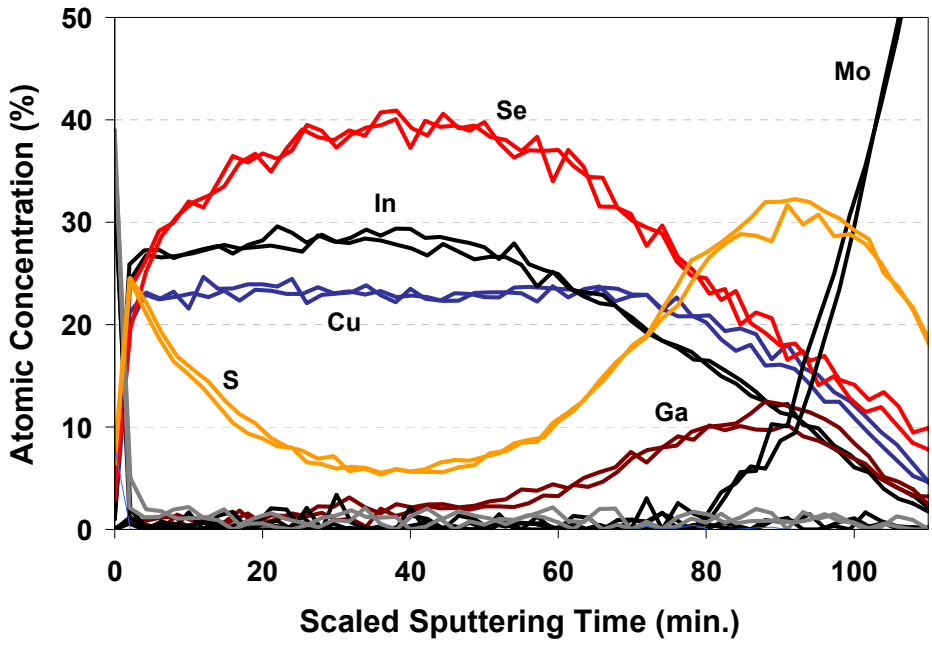

Figure 26. Nearly identical elemental profiles for two samples from two sputtering systems.

Additional precursor process development indicates that efficiency improvements are possible for thicker absorbers after improving adhesion. Increases in efficiency were demonstrated for thicker absorber layers as summarized in Table 4. Efficiency increases of 12% and 15% respectively are observed for absorber layer thickness increases of 125% and 150% of the baseline thickness. These gains based on circuit plate measurements are somewhat inflated relative to the results expected for laminates. Poorer adhesion correlated with both increased thickness and plate position within the reactor.

Table 4. Circuit performance versus absorber thickness.

	Change Relative to Baseline			
Thickness	**Eff**	**FF**	**Jsc**	**Voc**
125% of baseline	12%	9%	3%	0%
150% of baseline	15%	9%	10%	-1%

The following charts illustrate the dependence of module performance on doping concentration during ZnO CVD. Modules with otherwise common process steeps were fabricated with baseline dopant concentrations and dopant concentrations above and below baseline conditions. ICP analysis indicates achieved dopant concentrations relative to baseline conditions of 55%, 100%, and 116%. Performance measurements were made after fabrication, after lamination and after two days of outdoor exposure. Circuit plate measurements were made using a constant light source solar simulator after about 100 seconds of light exposure and biasing near the maximum power point. Laminate measurements were made using a flash lamp solar simulator after biasing near the maximum power point for about seven seconds. The results indicate an approximately five percent performance improvement for the lower doping concentration and these conditions were adopted as updated baseline conditions.

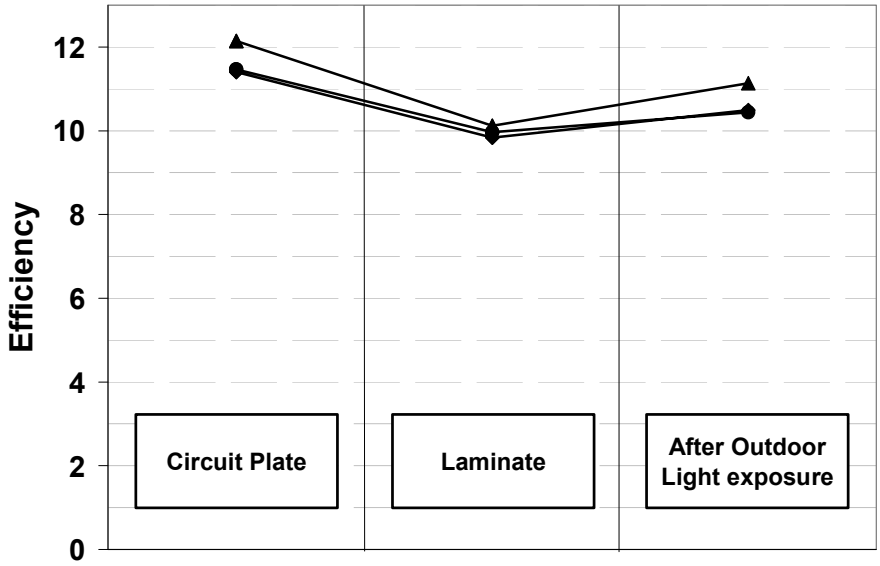

Figure 27. Circuit plate and laminate performance for ZnO doping relative to baseline conditions of 55% (▲), 100% (♦), and 116% (●).

In addition to these examples, process R&D for performance improvements and capacity scale up has included:

- Addressing major yield issues such as scratches, mechanical yield, operator errors, equipment malfunctions and improper setup
- Demonstrating and addressing loss of FF with lamination related to capacity scale up of the CdS deposition process.
- Background exploration of XRF analysis as a replacement for measurements using quartz crystals to monitor the Cu/(In+Ga) ratio for precursors
- Dependence of precursor quality on long term execution of the sputtering process
- Dependence of precursor quality on alternative target configurations, sputtering system hardware and sputtering target vendor selection
- Dependence of electrical performance on the ratio of Cu/(In+Ga)

- Demonstration and addressing performance losses related to the use of plastic boxes for transporting plates.
- Exploring the possibility of replacing CVD ZnO with sputtered ZnO.
- Qualification of a new continuous light-source tester for 1x4 ft. circuit plates and the elimination of an outdoor light exposure prior to circuit plate measurement.
- Process options for Glass/glass packaging of small modules for low-voltage (< 48V) applications.
- Exploration of process options for Mo removal from the edge of circuit plates as one of the process developments necessary to implement glass/glass packaging options

Module Packaging and Product Durability

NREL supports SSI through long term testing of arrays and individual modules at the NREL Outdoor Test Facility. SSI has supplied modules of increasing size and efficiency for testing since 1988. The measurements in Figure 28 were made by bringing modules indoors, performing the measurements under standard test conditions using a pulsed solar simulator, and then returning the modules to their outdoor test location. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over thirteen years.

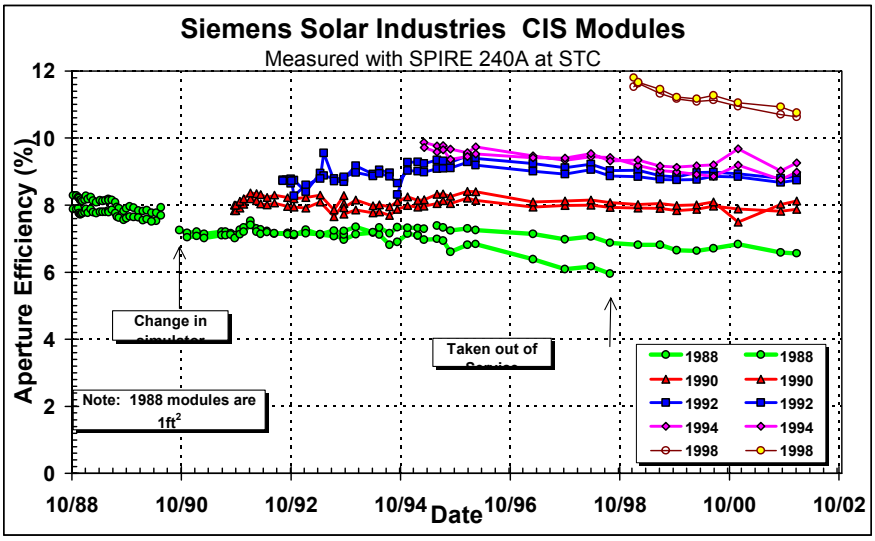

Figure 28. NREL OTF long term outdoor stability measurements - pulsed solar simulator.

NREL measurements for long term stability testing also include outdoors measurements made near standard test conditions. SSI CIS modules exhibit transient effects that can confound the interpretation of data particularly for pulsed solar simulators [3]. Parallel data from NREL outdoors measurements near standard test conditions is presented in Figure 29. As is typical for CIS, continuous illumination measurements such as outdoor measurements indicate less variation in performance with time for all modules tested.

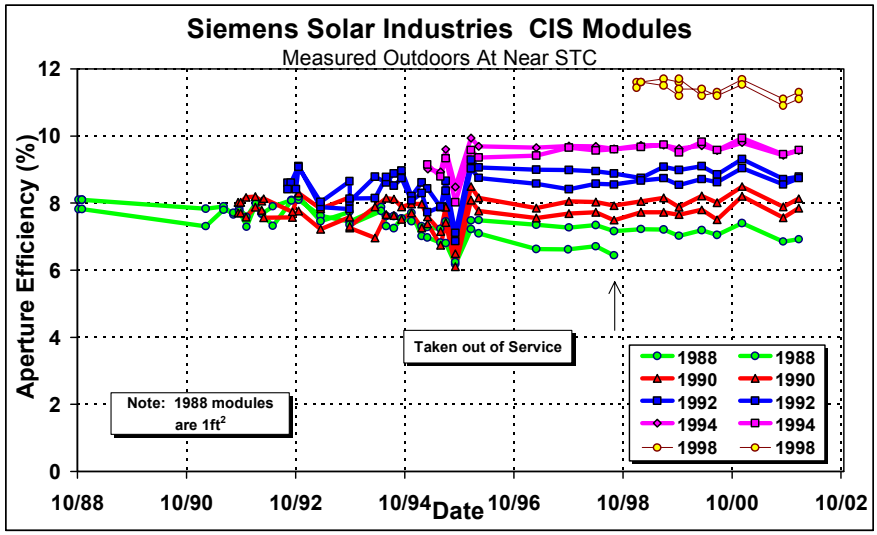

Figure 29. NREL OTF long term outdoor stability measurements - outdoors measurements.

SSI has supplied modules to the NREL OTF for three 1kW arrays. In each case, a newer generation of modules has been used to replace older designs using the same test site. Data acquisition began on November 18, 1998 for the third 1kW array of modules. The system is comprised of 28 modules with an average efficiency of 11.4% at STC. The aperture area of each module is 0.3651m^2 and of the total array is 10.2 m^2. The array is fixed at a 40° tilt aligned true south and is connected to a resistive load through 3 maximum power trackers.

Data from late February of 2000 indicates stability within 2% of the measurements made shortly after array deployment (Ben Kroposki, STR00SSI.001). Figure 30 summarizes NREL measured performance data for operation through June 30, 1999. The data is corrected for temperature and restricted to incident solar irradiance of between 950-1050 W/m^2. The array remained stable and has an average power normalized to standard test conditions of 1028 W. As for previous arrays, both module and the array data show good stability with no seasonal variation in performance. It can not be overemphasized that these studies demonstrate that thermally induced transients, which are observed after exposure to accelerated environmental testing conditions, are not observed in the field despite daily and seasonal changes in module temperature.

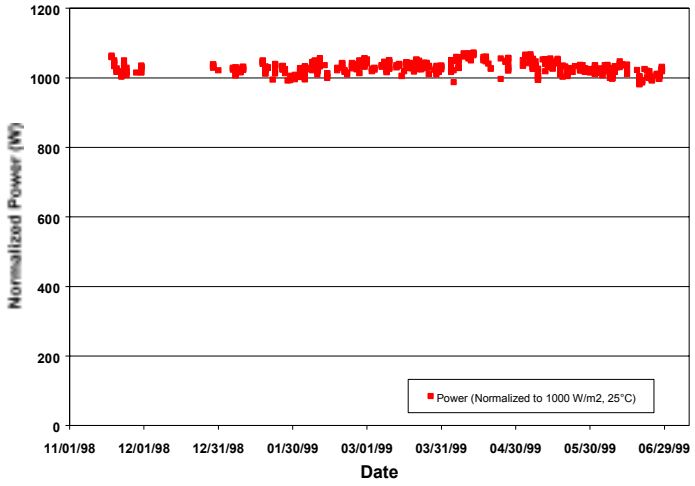

Figure 30. Temperature corrected power vs. time for the third 1kW array delivered to the NREL OTF in 1998.

More recent array data from the OTF analyzed by SSI (Figure 31) indicates that the latest array may exhibit changes with time related to changes in module package design or process changes since deploying earlier arrays. NREL supplied pulsed simulator, continuous illumination simulator, and outdoor measurement data for six of the modules from the array. This data indicates that changes in performance are primarily changes in FF and, typical of CIS, observed changes are smaller for measurements made with continuous illumination or outdoors than for pulsed simulation. For this small sample of six modules, the change in FF is highly variable ranging from within the noise of the initial and recent measurements, 4%, to 18%. All modules do not degrade which may imply that changes are related to the interim package design for these modules. Alternatively, the changes for this array may be related to process changes made since installation of the first array, which was deployed for a similar time and did not exhibit these changes.

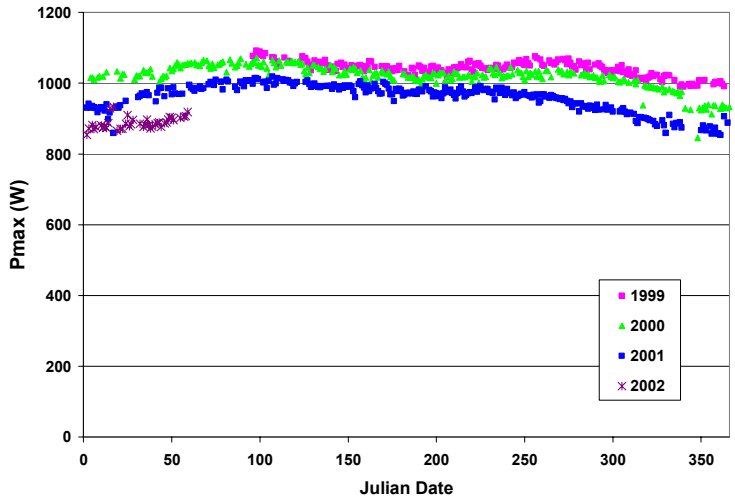

Figure 31. SSI analysis of OTF data for temperature corrected power vs. Julian date for the third 1kW array delivered to the NREL OTF in 1998.

Although long-term outdoor stability has been demonstrated at NREL, SSI fabricated CIS-based devices have failed standard accelerated environmental stress tests. Laminates (Glass/EVA/circuit) have been subjected to thermal cycling (TC) and humidity-freeze cycling (HF) at NREL. The thermally induced losses from TC and HF stress tests recover with outdoor exposure. Although performance recovers after subsequent outdoor exposure, the modules fail the accelerated test based on a strict interpretation of the accelerated test procedures. In addition, water vapor ingress resulting from extended damp heat testing permanently degrades performance for glass/EVA/circuit laminate structures.

SSI has demonstrated packaging designs that protect laminates from water vapor ingress during damp heat testing and allow modules to pass the damp heat test; however, the yield for passing the damp heat test with these packages was lower than acceptable and the package designs were not desirable for commercialization. Multiple package designs including alternative edge seals, desiccants, sealant tapes, circuit protecting coatings, primers and pottants were explored during this subcontract with similar results. The methods used during this subcontract period in conjunction with new package tests were not automated. The ability to reasonably automate a process is a necessity and, from the perspective of performing quality experiments and proper interpretation of experiments, the yield for passing accelerated testing may in part relate to the number of samples available or the consistency of hand operations (particularly edge deletion).

A glass/glass package is key to further progress toward an inexpensive package that protects the circuit. In Figure 32, the module package design presently used for products is compared with future package designs. For CIS products produced during this subcontract, EVA is used to laminate the module components - circuit plates, tempered cover glass and backsheet. The TPAT backsheet and the offset between the circuit plate and the frame provides for electrical isolation from the frame and a semi-hermetic seal. Aluminum extrusions are used to build frames for the modules.

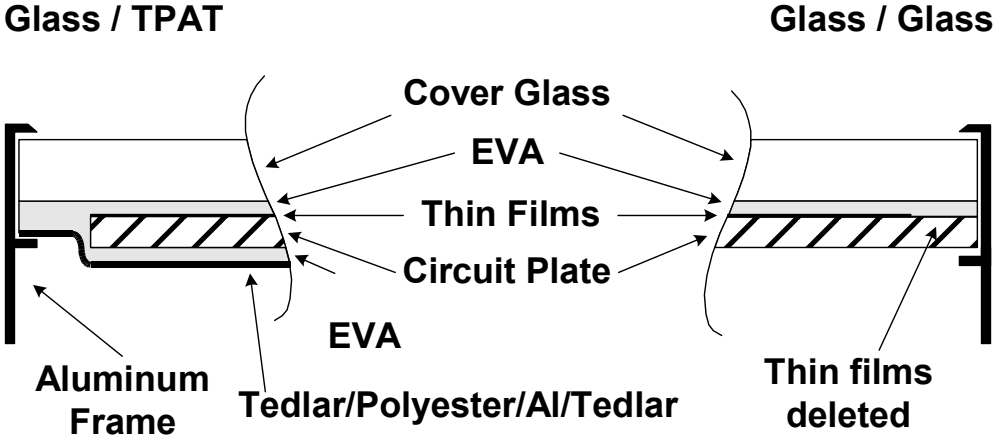

Figure 32. Comparison of present module encapsulation with Glass/Glass encapsulation options including thin film edge deletion.

The proposed future package designs eliminate costs associated with the TPAT backsheet and attaching the backsheet with EVA. A hermetic seal is obtained by bonding a metallic edge seal to the faces, edges or both faces and edges of the cover glass and circuit plate. Alternatives to the EVA potent may be considered for reduced cost, improved durability or for compatibility with particular approaches to edge seal application. If necessary, a desiccant or protective coating over the circuit can be incorporated to augment the edge seal. Alternatively, a protective coating over the circuit may eliminate the need for an edge seal and lead to a more cost-effective package.

A bare glass border on circuit plates is key for relatively simple glass/glass package options (framed or unframed). In addition to providing electrical isolation, a structure with a bare glass border, rather than thin film coated glass surfaces, eliminates multiple possible paths for water vapor ingress. A border can be achieved by inhibiting deposition of the films or removal of the films after completion of the circuit plate. The latter is referred to as edge deletion. Subcontract work included a brief exploration of inhibiting deposition of the thin films. Removal of the films was selected as the preferred approach since this avoids process complexity and allows straightforward product size selection after and independent of circuit plate production steps. Two edge deletion approaches were pursued during this subcontract: etching and laser scribing.

Etchant options for thin film removal were surveyed on a laboratory scale and etching with $FeCl_3$ was chosen for further study. The test fixture inside a walk-in hood pictured in Figure 33 was built to test etching of approximately one square foot circuit plates and to explore the feasibility of an etching process for full size circuit plates with production scale equipment. The test fixture consists of a solution tank with thermocouple-controlled heaters, a recirculating pump and provisions to immerse the edge of a circuit plate to a controlled depth. Circuit plate edges were etched with and without first removing the CIS from the Mo base electrode. The process parameters explored included temperature, time, concentration, and replenishment rate. A successfully etched circuit plate is shown in Figure 34. Problems with this approach include slow etch rate, uneven edge definition for the highest etch rates, extensive handling for etching and rinsing, and condensation on the circuit plate.

Figure 33. Test fixture etching based edge deletion.

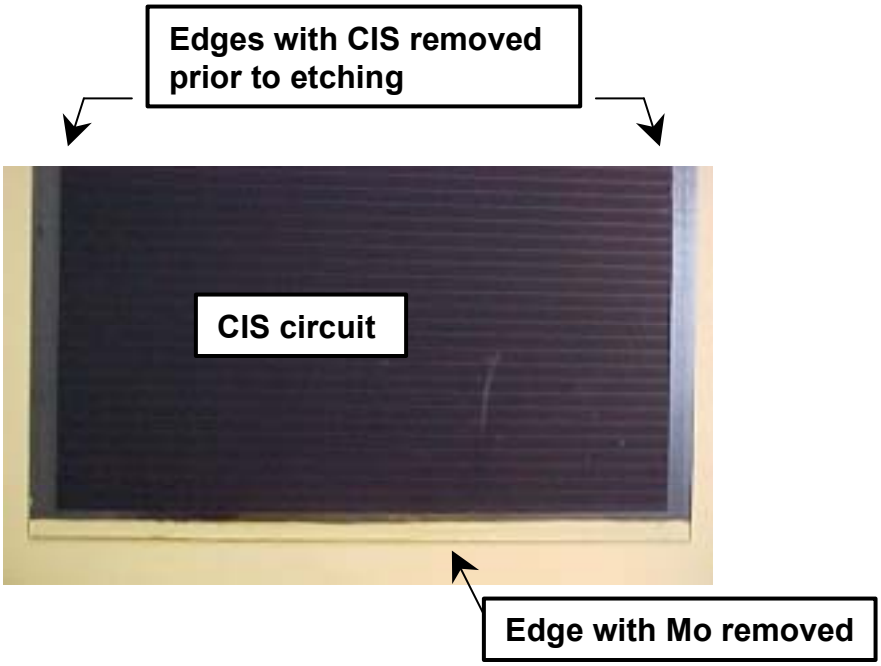

Figure 34. Circuit plate with successful etch based edge deletion.

Based on work during this subcontract, laser processing for edge deletion has been selected as the process to implement for production. Edge deletion via laser processing was tested on small samples in collaboration with laser equipment vendors. A yellow cast relative to unprocessed glass and altered surface features after laser deletion were initially a concern that was explored with the help from NREL (reference Manuel J. Romero). EDS analysis indicated that the yellow cast is probably due to remaining trace amounts of Mo and Se (Figure 35). Small test laminates with the laser edge deletion process passed wet high-pot testing indicated that this residue should not be a problem. Based on these subcontract activities, full scale equipment for laser edge deletion has been ordered.

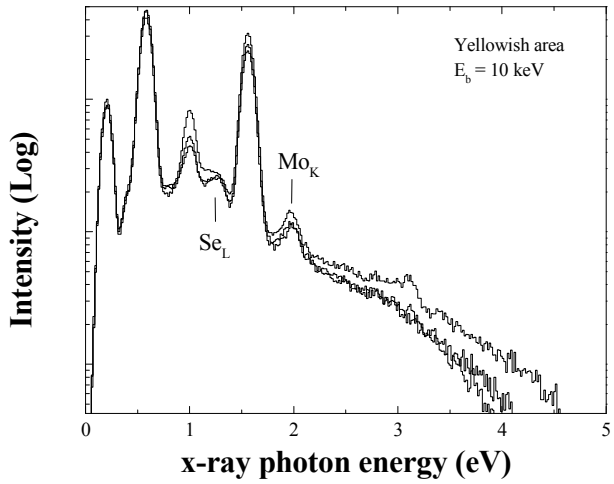

Figure 35. EDS spectra for a laser edge deleted section of a module.

National CIS R&D Team Participation

The dependence of transient effects on circuit fabrication process have been examined in collaboration with NREL TFPPP Teams and as studies at SSI extending Team activities. The NREL TFPPP "Transient Effects Group" is composed of representatives from industry, NREL and universities:

Joe delCueto	NREL
Joe Cuiffi	Pennsylvania State University
Neelkanth Dhere	Florida Solar Energy Center
Keith Emery	NREL
Pamela Johnson	Colorado State University
Rommel Noufi	NREL
Larry Olsen	WSU
Kannan Ramanathan	NREL
Angus Rockett	University of Illinois
William Shafarman	Institute of Energy Conversion
James Sites	Colorado State University
Dale Tarrant	Siemens Solar Industries
Hong Zhu	Penn State University

Transient effects are important in many topics including accelerated testing, process definition, measurement protocols, process predictability, interpretation of experimental test results, and understanding of device structures.

SSI's participation in Team activities was focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of identifying the origin of transient behavior, eliminating or minimizing transient behavior if possible, and defining improved processes. Buffer layer technology is directly related to transient effects and alternative buffer layer approaches are also of particular interest for process scale-up. Therefore, the scope of team activities also included exploring improved buffer layer processes. Summarizing results for all of the extensive team member activities is not attempted in this report since the expertise for most team activities resides with the team members. Instead, the following joint NREL/SSI experiments are discussed as an example of teamwork where SSI has had major involvement in both sample preparation and data analysis. Overall team achievements are also summarized.

Collaborative studies with NREL explored buffer and window layer options with emphasis on the impact of these layers on transient effects [19]. Additional long term objectives of these studies were to improve understanding of the basic roles of the buffer and window layers, and to define a Cd free buffer layer process with minimal transients. Discussed below are studies to explore differences between CdS and ZnO deposited by NREL and SSI on SSI absorbers. Process variations included:

- SSI baseline CdS & ZnO
    - Standard processing time frame and environmental exposures during processing
    - SSI baseline held at SSI - interrupted processing to parallel the processing at NREL
    - SSI baseline shipped to NREL and back to SSI
- NREL baseline CdS & sputtered ZnO
- NREL CdS and SSI ZnO
- NREL CdS & thin sputtered ZnO combined with SSI ZnO

Process variations were tested using SSI mini-modules and small area NREL test structures (0.43 cm^2). Processing at SSI employed baseline processing with the exception of interruptions for shipping. The sputtered ZnO depositions at NREL were a standard NREL process. CdS deposition at NREL required modification of their standard procedures to allow processing 10x10 cm substrates. Relatively long storage times in N_2 occurred while waiting for processing at NREL and while waiting for the redevelopment of a 10x10 lamination process in new equipment at SSI.

Figure 36 and Table 5 summarize the data for circuit plates and cell. Circuit plate data is a measurement after two minutes of exposure at 1 sun illumination in a solar simulator. Poor circuit plate performance and nominal cell performance for the NREL ZnO without the addition of SSI ZnO is not significant since this is simply due to a sheet resistance that is higher than appropriate for circuit plates.

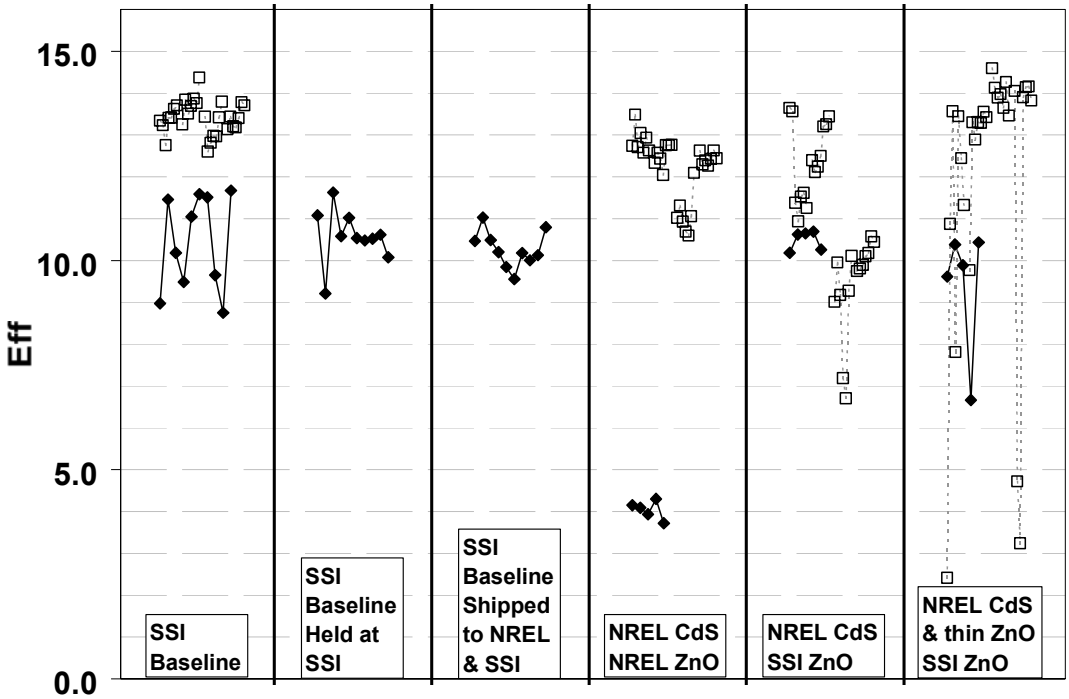

Figure 36. NREL/SSI buffer and window layer comparisons
Eff for circuit plates (◆, two minutes measurements) and cells (□).

Table 5 summarizes the data in terms of average parameters, standard deviations, and T-test results. T-test results are rounded so that only entries that round to 0% probability indicate significant differences at the 95% confidence level. For circuit plates, the SSI baseline process which was shipped to NREL is chosen as the reference group (p = 100%). For NREL cells, the immediately processed SSI baseline is the reference group. The following summarizes the results for circuit plates and cells:

- There is a statistically significant but small (3 to 5 points in Voc and Jsc) difference between immediately processed SSI baseline circuits and those shipped to NREL and returned for SSI baseline processing (the reference group). The differences may be related to differences between CdS/ZnO processing groups at SSI or differences in storage time.

- Statistically significant differences are demonstrated between the Voc for the circuit plate reference group and the circuit plates with NREL CdS & SSI ZnO. This difference in Voc would not have been significant with a different choice for the reference group (the immediately processed SSI baseline circuits). However, also considering the T-tests for NREL cells indicates that there are significant differences between Voc and Jsc for CdS from NREL and SSI. NREL CdS yields a slightly higher Voc (2 to 5 points) and lower Jsc (2 to 7 points).

- The other entries in Table 2 indicating statistically significant differences between groups (typically Voc and Jsc entries) are related to high variability or small group size rather than physically significant observations.

Table 5. Statistical analysis of SSI circuit plates (two minutes measurements) and NREL cells.

Circuit Plate and Cell Measurements

Average, Standard Deviation, P-value

Mini-modules

Description	Group	Eff.		V_{oc}		J_{sc}		FF	
		Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%
SSI Baseline	**1**	**10.4**	1.2 68	**0.51**	0.02 **0**	**34.6**	0.4 **0**	**0.59**	0.1 12
SSI Baseline held at SSI	**2**	**10.6**	0.6 23	**0.49**	0.01 29	**34.5**	0.9 3	**0.62**	0.0 91
SSI Baseline shipped to NREL	**3**	**10.3**	0.4 100	**0.49**	0.01 100	**33.8**	0.6 100	**0.62**	0.0 100
NREL Baseline CdS & ZnO	**4**	**4.0**	0.2 **0**	**0.53**	0.01 **0**	**23.2**	1.1 **0**	**0.33**	0.0 **0**
NREL CdS / SSI ZnO	**5**	**10.5**	0.2 25	**0.52**	0.01 **0**	**32.5**	0.6 1	**0.62**	0.0 95
NREL CdS & thin ZnO / SSI ZnO	**6**	**9.4**	1.6 28	**0.50**	0.03 55	**33.0**	0.4 1	**0.57**	0.1 16

NREL Cells

Description	Group	Eff.		V_{oc}		J_{sc}		FF	
		Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%	Avg.	Dev. p -%
SSI Baseline	**1N**	**13.4**	0.4 100	**0.54**	0.01 100	**34.8**	0.9 100	**0.72**	0.01 100
SSI Baseline held at SSI	2								
SSI Baseline shipped to NREL	3								
NREL Baseline CdS & ZnO	**4N**	**12.2**	0.8 **0**	**0.56**	0.01 **0**	**32.3**	1.1 **0**	**0.68**	0.02 **0**
NREL CdS / SSI ZnO	**5N**	**10.9**	1.8 **0**	**0.54**	0.01 **0**	**32.8**	0.8 **0**	**0.61**	0.09 **0**
NREL CdS & thin ZnO / SSI ZnO	**6N**	**12.0**	3.4 4	**0.52**	0.07 41	**34.0**	0.6 **0**	**0.66**	0.14 3

Transient effect information for the process variations was obtained for circuit plates before lamination, after lamination, after a 12-day outdoor exposure, and after exposure to 85°C for 44 hours. For each of these states, data was obtained by taking multiple measurements during a two-minute exposure (~1.5, 5, 12, 30, and 120 sec.) in a constant light source solar simulator. As an example of this data, Figure 37 is a chart of FF data after exposure to 85°C for 44 hours ("dry dark heat") where the sequential measurements for each circuit are connected as illustrated to the

right of the chart. Differences in transient effects for the process variations were compared for each state using a T-tests for differences in the change in device parameters over the two minute exposure, and differences in the slope calculated by linear regression of FF versus the log of the exposure time [3, 20, 21]. Process variation dependent transient effect differences without a consistent trend are observed before lamination, after lamination, and after a 12 day outdoor exposure. However, there was no statistically significant process dependence after the exposure to 85°C for 44 hours (Figure 37). T-test based comparisons for a relatively small data sets also indicated that there is no difference in transient effects for NREL sputtered ZnO and CVD ZnO.

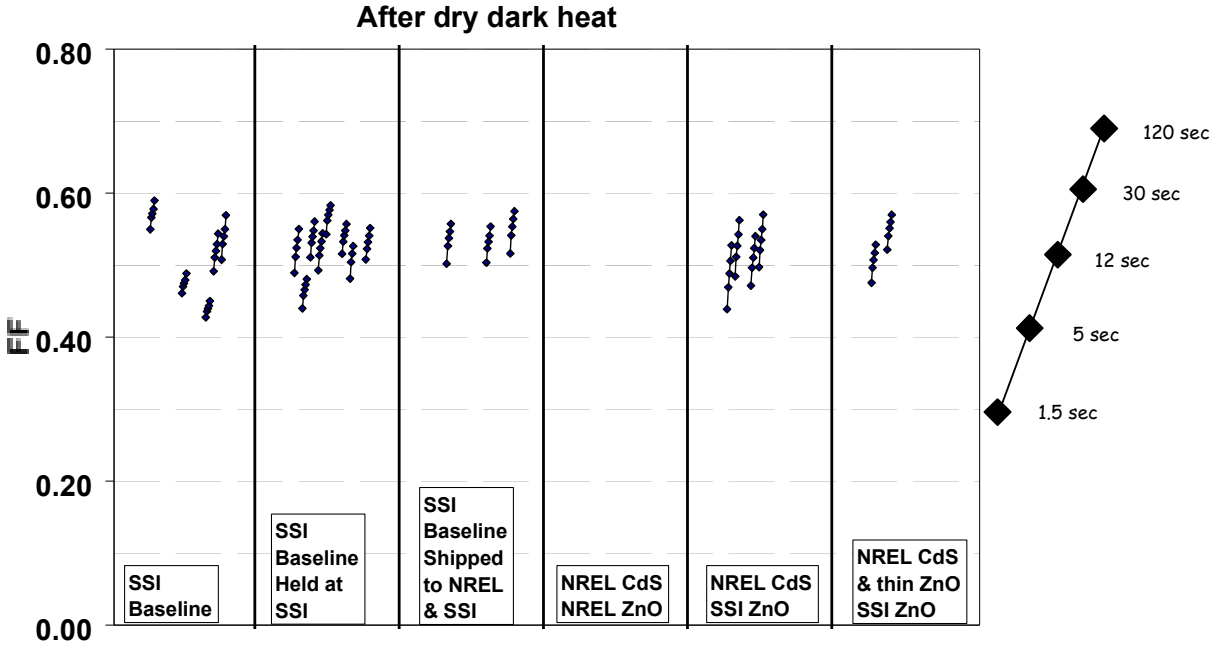

Figure 37. FF for mini-modules after a thermal stress.
(Multiple measurements over the two-minute test are connected for each circuit.).

As another example of team activities, NREL defined and executed an experiment exploring the influences on SSI absorbers of a KCN etch prior to CdS deposition and annealing in air at 200ºC after completion of device structures [22]. The following chart (Figure 28) indicates that FF improves with etching and air annealing. Samples of these devices were distributed to other team members for further study of transients.

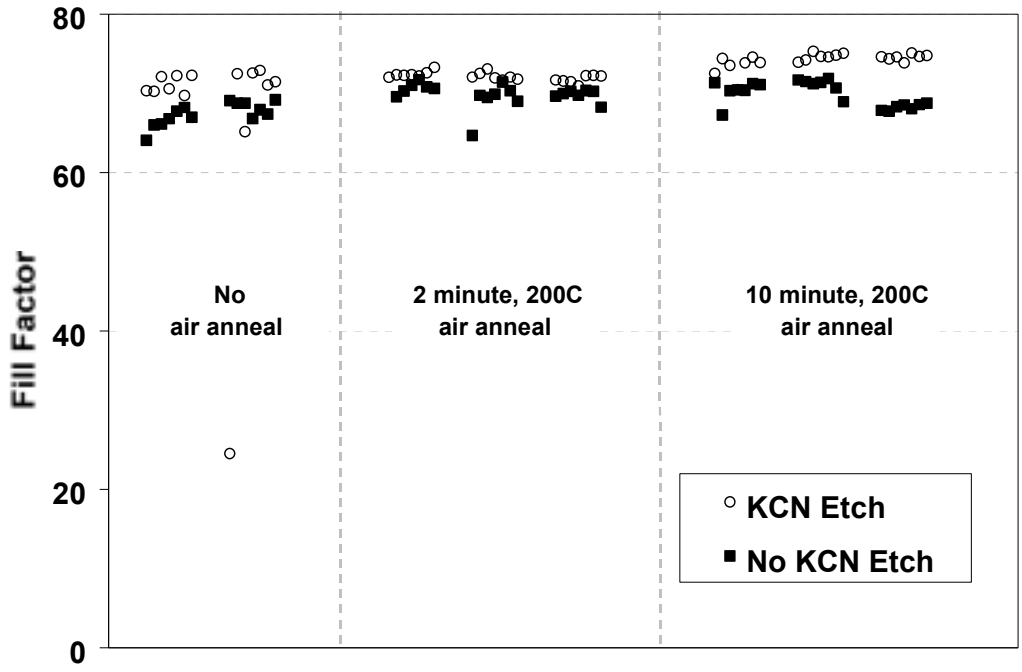

Figure 38. Data from SSI/NREL collaborations related to buffer layers (Abscissa – module Identifier)

The NREL TFPPP "Transient Effects Group" made significant progress studying transient effects in thin-film CIS-based devices. The team objectives were to identify the origin of transient behavior, eliminate transient behavior if possible and define improved processes. Studies included cells, mini-modules, and modules subjected to light exposure, thermal exposure and voltage biases with and without encapsulation. Major emphasis was focused on understanding the fundamental mechanisms responsible for these effects in CIGS-based devices. This understanding was obtained through device measurements and, as appropriate, comparison with computer modeling results. The following outlines the approach take by the Transient Effects Group:

- Team oriented R&D
- Characterize transient behavior
- Identify the origin of transient behavior
- Understand the fundamental mechanisms
- Apply the understanding to define potential solutions and test the solutions
- Apply the understanding and experimental results to achieve additional device performance or process improvements

Successes of the team included:

- Advancement of characterization of transient effects

- Definition of a repeatable measurement methodology for systematic study of transient effects
- Demonstrated that some potential causes for the effect are not dominant and directed efforts accordingly
- Improved understanding of the effect and CIS devices
- Demonstrated and communicated that transients are important to consider when measuring CIS
- Demonstrated long term stability for normal operating conditions
- Demonstrated process approaches that influence this effect and may eventually mitigate or eliminate the effect
- Defined areas for future study

Milestones and Deliverables

Milestones

SSI introduced ST5 (5 Wp) and ST10 (10 Wp) products just prior to this subcontract. During this subcontract, R&D Magazine recognized the significance of this major milestone in the development of photovoltaics by awarding the prestigious R&D 100 Award to the SSI family of CIS modules. This award is shared by the California Energy Commission, NREL and SSI [23].

During the first phase of this subcontract, SSI announced the availability of two new CIS products. These larger area modules expanded the power range of available CIS products from SSI – ST20 (20 Wp) and ST40 (initially rated at 38 Wp and then re-rated as 40Wp). A photo of the expanded product line appears in Figure 39. These four products are fabricated from circuit plates that are processed through all device formation processes in an ~1x4 ft. format. The 1x4 ft. circuit plates are laminated as ST40 modules or cut to smaller sizes to form ~30x70 cm ST20, ~30x36 cm ST10, or ~30x18 cm ST5 products.

Figure 39. SSI's CIS thin-film module products.

SSI completed the necessary engineering investigations and obtained FM and UL approval for the ST series of products. The durability and reliability of the ST family of CIS thin-film products is backed by a 10-year warrantee. As discussed in the previous section titled "Circuit Plate & Module Statistics", process reproducibility was demonstrated based on statistical process control criteria.

NREL confirmed a world-record 12.1 percent conversion efficiency for a large area (3651 cm^2) CIS module.

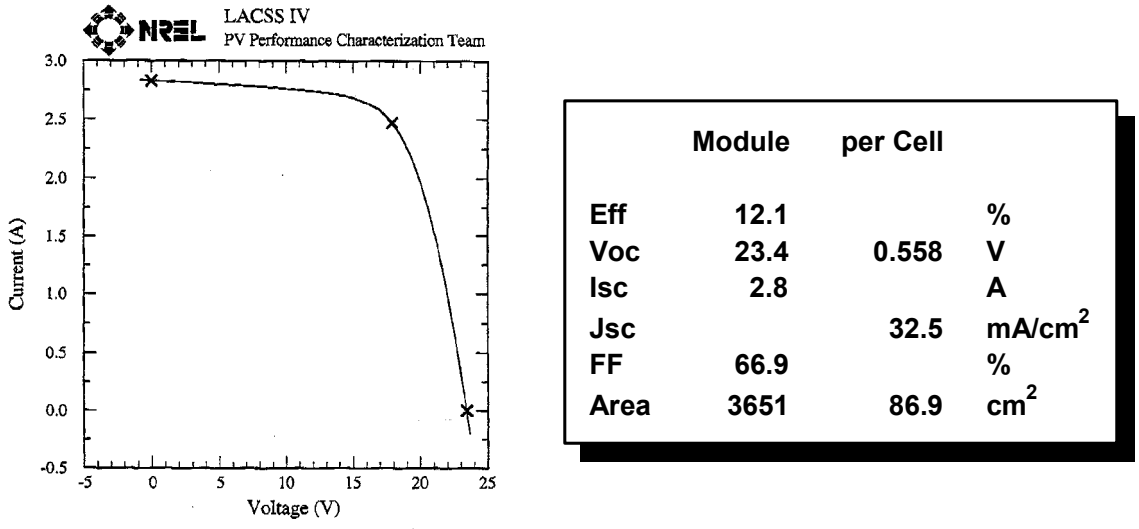

Figure 40. World-record 12.1 percent conversion efficiency large area CIS module.

These subcontract accomplishments fulfilled the first subcontract goal - to scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2) using a process that has been adopted for SSI commercial activities and is reproducible as determined by statistical process control criteria.

The second subcontract goal was also achieved:

> "Achieve a pilot production rate of 500 kW per year by the end of this subcontract"

SSI production rate was first achieved this goal in March of 2001 and the SSI production rate has consistently exceeded this rate since June of 2001.

Deliverables

The following deliverables were defined for the first subcontract phase:

- D1. End of the 12^{th} month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.
- D2. End of the 12^{th} month: Deliver ten (10) 900-cm^2 (1-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

These specifications for commercial modules as deliverables are most closely matched by the 10-Watt ST10 and the 5-Watt ST5 modules that were introduced in 1998. However, activities during the first subcontract period led to the availability of commercial products larger than anticipated at the time the deliverables were defined. As agreed to by the NREL Technical Monitor, SSI delivered the following samples of larger area product as the D1 and D2 deliverables:

- Four 20-Watt "ST20" modules
- Four 40-Watt "ST40" modules

The following deliverables were defined for the second subcontract period:

> D3. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10%.
>
> D4. End of the 24th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 10% for the NREL Module Testing Team.

Twenty (20) ST-40 modules were shipped to the NREL OTF. These modules were taken from the warehouse and were representative of the mid to upper portion of SSI's normal production distribution. NREL personnel discussed the use of these modules and tentatively identified applications for a large portion of the modules (PERT, long-term test bed, outdoor lighting applications). NREL measured the modules [24] outdoors and using continuous and pulsed solar simulators (SOMS, LACSS, SPIRE). The following chart (Figure 41) of NREL (SOMS) versus

SSI measurements indicates excellent agreement between SSI and NREL measurements. All of these modules are over 11% based on an aperture area of 3629 cm^2 and two of these production modules slightly exceed the NREL confirmed 12.1% conversion efficiency for large area modules.

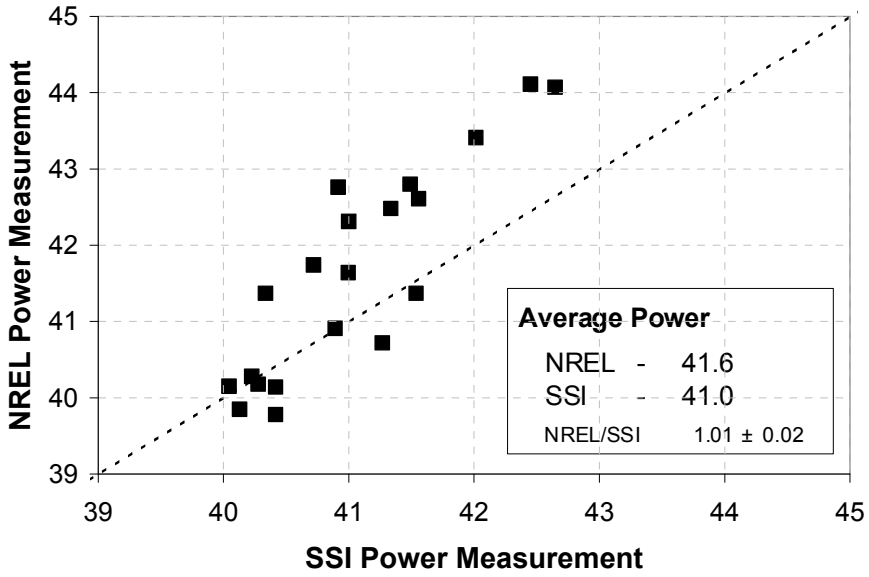

Figure 41. Correspondence between NREL and SSI measurements for deliverables.

The following deliverables were defined for the third subcontract phase:

> D5. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12%.
>
> D6. End of the 36th month: Deliver ten (10) 4000-cm^2 (4-ft^2) CIS-based commercial modules with AM 1.5 aperture-area efficiency of 12% for the NREL Module Testing Team.

As discussed with the Subcontract Monitor, ST5 modules were preferred as readily transportable examples of the technology. Also, NREL had recently purchased ST40 modules and had no need for additional ST40 modules at the NREL OTF. Therefore, 20 ST5 modules were shipped to the NREL OTF to fulfill the D5 and D6 contract requirements. The following table (Table 6) summarizes SOMS measurements at NREL. NREL reported results are for module aperture area, which is the free aperture of the frame. SSI estimates for circuit area efficiency are also included since this presentation of the data is more representative of the present state of production technology and is more appropriate for comparison with other results reported here such as champion devices results from NREL and circuit plate distributions.

Table 6. NREL measurements of at 20 ST5 modules.

	Module	per Cell	
Eff Circuit area *	10.2 ± 0.7		**%**
Eff Module aperture **	8.8 ± 0.6		**%**
Voc	23.7 ± 0.8	0.563 ± 0.018	**V**
Isc**	0.38 ± 0.02		**A**
Jsc*		31.0 ± 1.8	**mA/ cm^2**
FF	58.1 ± 2.4		**%**

* 518.5 cm^2, Includes intereconnect area
** 606.7 cm^2, Includes boarders around circuit

Conclusions

CIS process R&D has achieved outstanding progress toward NREL/DOE goals:

- SSI introduced two new CIS products to the SSI ST family of products including an approximately 1x4 ft, 40Wp module.
- R&D Magazine awarded the prestigious R&D 100 Award to SSI, NREL, and the CEC for the SSI family of CIS modules.
- The first subcontract deliverables were larger and higher in efficiency than specified in the SOW.
- The first subcontract milestone was met by the first deliverables - scale from a substrate size of approximately 900 cm^2 to a substrate size of approximately 4000 cm^2 (4 ft^2).
- NREL confirmed a world-record 12.1% conversion efficiency large area (3651 cm^2) thin-film module. More than a year in advance of the milestone for the 1998-2000 DOE Program Plan, SSI far exceeded the DOE year 2000 goal of 10% for commercial CIS modules.
- Capacity has been increased by nearly an order of magnitude while also increasing the average efficiency of 1x4 ft circuit plates.
- The distribution of production modules is sharply peaked at nearly 11% efficiency with a full width of only ± 0.5%; almost all production module efficiencies are above 10%.
- The second subcontract milestone - pilot production rate 500 kW per year - was first achieved in March of 2001 and the SSI production rate has consistently exceeded this rate since June of 2001.
- Process R&D tasks have been addressed for *all* processes by applying systematic research, development and, production methodologies such as SPC, ANOVA and DOE.
- Performance and capacity scale-up achievements have been made even though more R&D resources than anticipated were expended on process development for new absorber formation reactors.
- Generally good process control has been demonstrated while scaling up capacity. Successes addressing issues at each increment in capacity has demonstrated the importance of cycles of learning for process R&D.
- Yield improvements have been made by implementing improvements in processes and manufacturing protocols.

- Process R&D has led to the demonstration of improved laser scribe quality and consistency for previously existing and new high throughput sputtering equipment. This know-how is largely responsible for defining a Mo deposition process for new sputtering equipment and improved circuit electrical yield from about 90% to typically above 95%.

- FM and UL approval was obtained for the ST series of products.

- Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over twelve years.

- SSI capabilities are leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. Additional NREL support has included specialty device and material measurements, and long term testing of arrays and individual modules at the NREL OTF.

CIS has demonstrated the prerequisites for a commitment to large-scale commercialization – predictable process performance even during scale-up, high efficiency, long-term outdoor stability, and attractive cost projections. Efficiency and yield advancements while scaling up production throughput were the result of systematic research and development through multiple cycles of learning. Continuous improvement will be driven by the application of statistical approaches through additional learning cycles. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over even longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of further efficiency improvements for future products.

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24. Steve Rummel, NREL Test Report #2K0102

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13. ABSTRACT *(Maximum 200 words):* This report describes the primary objectives of this subcontract, which are to scale up substrate size and to scale up production capacity of the baseline Siemens Solar Industries (SSI) CIS-based module process while introducing CIS-based products. The primary goals are to scale the substrate size from about 900 cm^2 (1 ft^2) to approximately 4000 cm^2 by the middle of Phase II, and to achieve pilot production rates of 500 kW per year by the end of Phase III. Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation. SSI will continue mid-term and longer-term thin-film R&D with the goals of:

- Assuring future product competitiveness,
- Improving module performance,
- Reducing cost per watt, and
- Assuring product reliability.

Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over even longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of further efficiency improvements for future products. SSI's thin-film CIS technology is poised to make very significant contributions to the DOE/NREL/NCPV long-term goal of higher-volume, lower-cost commercial products.

14. SUBJECT TERMS: PV; CIS; thin films; manufacturing; scale-up; production capacity; statistical process control (SPC); multinary absorbers; circuit processing sequence; modules

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