Fermilab

Particle Physics Division/CDF Upgrade Project

ADMEM
ADC/Memory Module

CHECKOUT DOCUMENT

Revised
10/20/97

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and
Rodney Klein

Initial Checkout

______ Visually inspect the Board. Board should match Bill of Materials (BOM) below.

______ Program all PLDs and PROMs. These are hi-lited in the BOM.

______ Make sure there is no short between power and ground. Measure ohms across Transorbs **D4 - D9** (page 1) to check for shorts.

______ Power Board **-** Power (red) indicator **D1** (page 1) should be on.

Setting the Jumpers

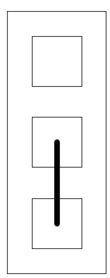
______ Install Jumper **S2** (page 3) to prevent ADMEM from issuing CDF_ERROR*

The ADMEM jumpers are initially set to allow for downloading the Pipeline FPGA from serial PROM. To do this,

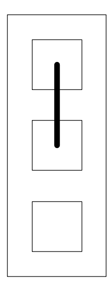
______ Install Jumper **S5** (page 16A)

______ Install Jumpers **S13, S11, S9**, and **S7** (pages 16A-19A)

______ Install Jumpers **J21** and **J22** (page 16A)in the lower position.



______ Install Jumpers **J18, J19, J20** (page 17A) **J15, J16, J17** (page 18A) **J12, J13, J14** (page 19A) and **J9, J10, J11** (page 20A) in the upper position.



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Bill of Materials

<<<From Job: D:\Ppd_Jobs\Analog_Admem\vbdc\admem_pre_prod.prj>>>

VeriBest, Inc.

item	qty	vendor part number	cost	total	description	references
1	2	AMP 173280-3 IPCON CARRIE	0.00	0	IPCON CARRIER - 50 PIN MINI-D	J23,J24
2	1	AMP 352009-1 PLUS SHIELDS	18.75	18.75	AMP 5x19 Z-PACK 2mm Female Conn w/gnd sh	P0
3	8	AMP 536272_1.	16.00	128	AMP 536272_1 40 pin micro_strip male 536	J1-J8
4	**1**	**AM27S19SAPC**	**1.25**	**1.25**	**32x8 PROM**	**U5**
5	1	AM29F200B-75EC	10.00	10	2Mb 5.0V Flash	U24
6	7	Am29F100B-75EC	15.00	105	1 Mb CMOS Flash Memory	U51,U53,U55,U57,U59,U61,U63
7	1	BOT d_strip	.01	0.01	Bottom Discharge strip	X2
8	1	C&K P8121 1160-1890	2.48	2.48	Mom. Push button Panel mnt	S1
9	20	CAFE_MODULE		0	Analog Cafe Module	PB1-PB20
10	15	COTTER PIN	0.01	0.15	test point	TP7,TP20,TP33,TP51,TP72,TP73
*						TP74-TP80,TP123,TP124
11	1	CY7B991-7JC	21.85	21.85	ROBOCLOCK	U66
12	2	CY7C470-15JC	22.00	44	Cypress 8K x 9 FIFO	U3,U17
13	9	CY74FCT16374CTPAC	3.45	31.05	16-bit register	U21,U36,U38,U40,U42,U44,U46
*						U48,U99
14	28	CY74FCT16543CTPAC	5.25	147	16-bit latched tranceiver	U37,U39,U41,U43,U45,U47,U49
*						U78-U98
15	9	CY74FCT162244TTSSOP	3.95	35.55	16-Bit Buffers/Line Drivers	U4,U50,U52,U54,U56,U58,U60
*						U62,U105
16	18	DS26C31TM RS-422 driver N	2.23	40.14	Differential Line Driver RS-422	U15,U20,U23,U32,U35,U64,U65
*						U67,U74,U76,U77,U100,U102
*						U103,U104,U106-U108
17	1	DS90C031TM		0	LVDS QUAD CMOS DIFF LINE DRVR	U112
18	6	ERIE 8121-050-651-103M 14	0.07	0.42	Bypass Cap .01UF	C27,C29,C32,C33,C41,C44
19	1	ERIE 8131-100-651-153M 14	0.07	0.07	Bypass Cap .015UF	C8
20	4	ERJ-8ENF1.00K Digi P1.00	0.0542	0.2168	1/8W 1% 1.0K ohm	R4,R11,R16,R19
21	6	ERJ-8ENF82.5 Digi P82.5	0.0542	0.3252	1/8W 1% 82.5 ohm	R14,R15,R22,R24,R27,R28
22	4	ERJ-8ENF100 Digi P100FB	0.0542	0.2168	1/8W 1% 100 ohm	R30-R33
23	6	ERJ-8ENF124 Digi P124FBK	0.0542	0.3252	1/8W 1% 124 ohm	R9,R10,R21,R25,R26,R29
24	1	ERJ-8ENF267 Digi P267FB	0.0542	0.0542	1/8W 1% 267 ohm	R5
25	7	FCN-235D020-G/E(MH)	2.20	15.4	Fujitsu 20 Pin SCSI II	P4-P10
26	3	HARTING-0201-160-2101	25.29	75.87	VME64 Card Connector	P1-P3
27	2	HP HLMP-1301 1445-0475	0.24	0.48	Red LED	D1,D10
28	2	HP HLMP-1401 1445-0495	0.24	0.48	Yellow LED	D2,D11

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Bill of Materials

<<<From Job: D:\Ppd_Jobs\Analog_Admem\vbdc\admem_pre_prod.prj>>>

VeriBest, Inc.

item	qty	vendor part number	cost	total	description	references
29	14	JUMP3	0.10	1.4	Three Pin Jumper	J9-J22
30	20	KEMET T340B106K015AS	0.53	10.6	10UF 15V Bullet	C2-C6,C18,C21-C23,C34,C35
*						C36-C39,C56-C60
31	7	KEMET T354H336K016AS	0.68	4.76	33UF 16V RADIAL Dip	C17,C26,C28,C30,C31,C40,C43
32	4	LITTLEFUSE 251002 1120-0	0.74	2.96	2 AMP PCB Fuse	F3-F6
33	2	LITTLEFUSE 251010 Newark	0.74	1.48	10 AMP PCB Fuse	F1,F2
34	**2**	**MACH 110-12JC**	**7.00**	**14**	**AMD PLD 44 Pin PLCC**	**U12,U16**
35	1	MC10H350P	7.98	7.98	PECL to TTL Translator	U73
36	4	MOTOROLA 1N5908	1.24	4.96	Transient Suppressor 6.0V	D4-D7
37	2	MOTOROLA 1N6275	0.70	1.4	Transient Suppressor 15V	D8,D9
38	9	PAN ECS-H1CC106R DIG PCT3	0.9765	8.7885	SMT CAP 10.0UF	C45,C48-C55
39	1	PAN ECS-H1CY105R DIG PCT3	0.3955	0.3955	SMT CAP 1.0UF	C46
40	1	PAN ECU-V1H103KBG DIG PCC	0.168	0.168	SMT CAP 0.01UF	C42
41	193	PAN ECU-V1H104KBW DIG PCC	0.5914	114.14	SMT CAP 0.1UF	C1,C7,C9-C16,C19,C20,C24,C25
*						C47,C61-C238
42	3	RC05-270 1487-0290	0.19	0.57	270 ohm 1/8W 5%	R1,R6,R7
43	1	RC05-820K 1487-0497	0.18	0.18	1/8W 820Kohm 5%	R8
44	3	RC07-1.5M 1487-1125	0.14	0.42	1/4W, 5PCT, THRU	R3,R13,R34
45	1	RC07-5.6 Digi 5.6QBK-ND	0.06	0.06	1/4W, 5PCT, THRU	R12
46	5	RC07-4700 1487-0825	0.08	0.4	1/4W, 5PCT, THRU	R2,R17,R18,R20,R23
47	6	SN74ABTE16245SSOP	5.60	33.6	16 Bit Incident Transceiver	U7,U14,U22,U34,U75,U101
48	12	Samtec TSW-12-07-L-D 2pin	0.16	1.92	2 pin jumper - mates with SNT-100-BK-G $	S2-S13
49	4	Spare-IC 24DIP3	0.00	0	Spare Part	U8-U11
50	110	TEST_PIN	.01	1.1	.025 x .025 square post.	1,TP1-TP6,TP8-TP13,TP15,TP16
*						TP17-TP19,TP21,TP25,TP26
*						TP27-TP32,TP34-TP40,TP43
*						TP44-TP50,TP52-TP71,TP81
*						TP82-TP86,TP88-TP122,TP125
*						TP126,TP127,TPCAL1,TPCAL2
*						TPCAL3,TPQCLK1
51	1	TOP d_strip	.01	0.01	Top Discharge strip	X1
52	3	XC4003EPQ100-3	45.75	137.25	Xilinx FPGA XC4003E	U25,U28,U30
53	6	XC4013EPQ240-3	293.60	1761.6	Xilinx FPGA XC4013EPQ240	U13,U68-U72
54	**3**	**XC17128-PD8C**	**9.70**	**29.1**	**Xilinx Serial PROM**	**U26,U29,U31**

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Bill of Materials
<<<From Job: D:\Ppd_Jobs\Analog_Admem\vbdc\admem_pre_prod.prj>>>

VeriBest, Inc.

item	qty	vendor part number	cost	total	description	references
55	**2**	**XC17256-PD8C**	**15.10**	**30.2**	**Xilinx Serial PROM**	**U6,U33**
56	2	shunt10 AMP 1-435704-0	0.62	1.24	10 position shunt	U18,U27
57	1	1N5817	.80	0.8	Shotky diode 1Amp 20V	D3
58	3	10x-2-102	0.34	1.02	Bourns 10 pin 1K SIP pin 1 common	RP1-RP3
59	1	74F38N	0.53	0.53	Nand gate, OC output	U19
60	1	74LS14N 1455-8014	0.31	0.31	Hex Scmitt-trigger Inverters	U2
61	1	74LS123N 1455-8123	0.35	0.35	Multivibrator	U1
62	1	2743021446 PSC ELECTRONIC	1.30	1.3	SMT FERRITE BEAD 10UH	L1

Total Parts Used: 597
Total Parts Cost: 2854.08

Check functioning of RESET Switch

______ Check the RESET PLD. **U16-8** (page 4A) should be high and go low when the front panel reset switch is depressed. **U16-26** should be low and go high when the reset switch is depressed.

```
                        MACH110A

                 R
              P  E  S     p        D     D
              R  S  Y     w        O     O
              O  E  S  s  r        N     N
              G  T  R  w  o        E     E
              _  _  E  r  n        _     _
              P  C  S  e  _        d     d
              I  D  E  s  r        e     e
              P  F  T  e  e        l     l
              E  _  _  t  s        5     4
            /----------------------------------
           /  6  5  4  3  2  1 44 43 42 41 40 |
           |                                  |
           |  7                            39 | DONE_del3
    reset_ |  8                            38 |
    tristx |  9                            37 |
    XDONE1 | 10                            36 |
    XDONE2 | 11                            35 |
           | 12                            34 |
    XDONE3 | 13                            33 | PIPE_DONE
    GLOBSR | 14                            32 | XDONE4
 XPROGRAM_ | 15                            31 |
PIPE_PROG_ | 16                            30 |
    PIPESR | 17                            29 |
           |                                  |
           | 18 19 20 21 22 23 24 25 26 27 28 |
           ------------------------------------
              R  D  D  D        P  P  !
              E  O  O  O        I  I  r
              S  N  N  N        P  P  e
              E  E  E  E        E  E  s
              T     _  _        _  _  e
              _     d  d        d  d  t
              C     e  e        o  o
              D     l  l        n  n
              F     1  2        e  e
                                1  2
```

Check for Proper Download

______ After Power has been applied, the front panel READY (green) indicator, **D10** (page16) should be on. If it is not on, check for a reversed LED or for a download failure of any of the Xilinx FPGAs.

______ Verify that the PLUG (green) indicator, **D11** (page 20A) is off.

Check for Xilinx Download

If the Xilinx download is successful, the following pins should be high.

______ VME Slave **U6-4** (page 3A)

______ FLASH Control **U31-4** (page 3B)

______ Pipeline **U33-4** (page 16A)

______ L2 Header **U29-4** (page 16B)

______ Download **U26-4** (page 16D)

Check of ADMEM Registers

Go into VASE, and

______ Map the crate and verify that the ID PROM **U5** (page5) of the ADMEM reads out in the correct slot and of a form similiar to that below.

0001 003 Analog Admem v1.0

The first number (0001) in the example should match the engraved board number, the rest of the field should read as the example does.

______ Verify that the Select (yellow) indicator, **D2** (page3) comes on when the board is addressed and turns off when it is not.

______ Test the Diagnostic Register. Located in the VME Slave FPGA **U13** (page 3A).

______ Test the Control Register. Located in the VME Slave FPGA **U13** (page 3A).

______ Test the Access Register for FLASH RAM. Located in the VME Slave FPGA **U13** (page 3A).

______ Test the Pipeline Length Register. Located in the Pipeline FPGAs **U68-U72** (pages 16A-20A), and the L2 header FPGA **U28** (page 16B).

______ Test the Pipeline Offset Register. Located in the L2 Header FPGA **U28** (page 16B).

______ Test the Flash RAM Select Register. Located in the VME Slave FPGA **U13** (page 3A).

______ Test the Pipeline Diagnostic Channels Enable Register. Located in the VME Slave FPGA **U13** (page 3A).

______ Test the Diagnostic Pipeline Data FIFO **-** **U3** and **U17** (page 5).

______ Read the L2 Buffer Header word, under the “Decode L2 Header Word” option in VASE. The word should correctly report

______ The slot address

______ The board Serial Number (same as engraved number)
programmed on **U18** page 16

______ The Board Type (should be 003)
programmed on **U27** page 16

Testing the next three registers involves having the **ADMEM Mezzanine Module plugged in**.

______ After plugging in the mezzanine module, check the mezzanine module's **U1-4** and make sure it is high, indicating the Xilinx FPGA has been downloaded.

______ Test the DAC Data Register. Located in Mezzanine FPGA **U2**.

______ Test the DAC Control Register. Located in Mezzanine FPGA **U2**.

______ Test the CAFE Control Register. Located in Mezzanine FPGA **U2**.

Checkout of Flash RAM spaces

There are 28 Flash RAM spaces on the ADMEM module. The first twenty spaces are alocated to the CAFE modules, the next 7 to the trigger sum lookup tables, and the final space is for downloading the pipeline FPGAs.

To Check the CAFE Module Address Space, make sure the ADMEM Mezzanine module is inserted and, rlogin to MVME162. At the prompt, type **ld <anadmem.o**, this loads the MVME612 with the anadmem object code. Then type **cd "pathname to your test directory"** , make sure the quotes are around the directory pathname. Then type **anadmem_menu** to start the program.

Make sure test directory is read/writeable to the world. To do this, go back one directory and type **chmod 777 directory name**, this needs to be done from the sun or from an xwin window on a PC.

Select option 7 **-** CAFÉ Allocated Flash Ram Test from the Checkout Menu.
This test is done automatically, user needs to check screen for errors and verification of the below steps:

______ "Enable VMEbus access to Flash RAM data lookup tables" in the Control Register is set.

______ Write BEAD (hex) to the Access Register for Flash RAM.

______ Write a "0" to the Flash RAM select register and insert a Digital Paddle board in module slot PB20.

______ Within VASE, go into the Flash RAM Word submenu.

______ step A. Erase the Flash RAM

______ step B. Verify that you can write the value 0x5a5a into address 0,

______ step C. read it back ,

______ step D. and erase it

______ step E. read address 0 **-** the value will be 0xFFFF upon erase

______ step F. now download sequential data to the FLASH RAM

______ step G. verify the sequential download.

______ Now write "1" to the Flash RAM Select register, insert a Digital Paddle board in module slot PB19 and repeat steps A thru G above.

______ Now write "2" to the Flash RAM Select register, insert a Digital Paddle board in module slot PB18 and repeat steps A thru G above.

______ Now write "3" to the Flash RAM Select register, insert a Digital Paddle board in module slot PB17 and repeat steps A thru G above.

______ Now write "4" to the Flash RAM Select register, insert a Digital Paddle board in module slot PB16 and repeat steps A thru G above.

______ Now write “5” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB15 and repeat steps A thru G above.

______ Now write “6” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB14 and repeat steps A thru G above.

______ Now write “7” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB13 and repeat steps A thru G above.

______ Now write “8” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB12 and repeat steps A thru G above.

______ Now write “9” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB11 and repeat steps A thru G above.

______ Now write “A” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB10 and repeat steps A thru G above.

______ Now write “B” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB9 and repeat steps A thru G above.

______ Now write “C” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB8 and repeat steps A thru G above.

______ Now write “D” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB7 and repeat steps A thru G above.

______ Now write “E” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB6 and repeat steps A thru G above.

______ Now write “F” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB5 and repeat steps A thru G above.

______ Now write “10” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB4 and repeat steps A thru G above.

______ Now write “11” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB3 and repeat steps A thru G above.

______ Now write “12” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB2 and repeat steps A thru G above.

______ Now write “13” to the Flash RAM Select register, insert a Digital Paddle board in module slot PB1 and repeat steps A thru G above.

Next we will test the Trigger Sum Flash RAMs

Select option 8 **-** Trigger Sum Flash Ram Test
This test is done automatically, user needs to check screen for errors and verification of the below steps:

______ Write a "14" to the Flash RAM Select register. Test Flash RAM **U63** (page 16C)by repeating steps A **-** E.

______ Write a "15" to the Flash RAM Select register. Test Flash RAM **U61** (page 17B) by repeating steps A **-** E.

______ Write a "16" to the Flash RAM Select register. Test Flash RAM **U59** (page 18B) by repeating steps A **-** E.

______ Write a "17" to the Flash RAM Select register. Test Flash RAM **U57** (page 19B) by repeating steps A **-** E.

______ Write a "18" to the Flash RAM Select register. Test Flash RAM **U55** (page 20B) by repeating steps A **-** E.

______ Write a "19" to the Flash RAM Select register. Test Flash RAM **U53** (page 20C) by repeating steps A **-** E.

______ Write a "1A" to the Flash RAM Select register. Test Flash RAM **U51** (page 20D) by repeating steps A **-** E.

Finally, the Pipeline Download Flash RAM will be tested.

Select option 9 **-** Pipeline Download Flash Ram Test
This test is done automatically, user needs to check screen for errors and verification of the below steps:

______ Write a "1B" to the Flash RAM Select register.

______ Within VASE, go into the Flash RAM **BYTE** submenu.

______ step A. Erase the Flash RAM

______ step B. Verify that you can write the value 0x5a into address 0,

______ step C. read it back ,

______ step D. and erase it

______ step E. read address 0 **-** the value will be 0xFF upon erase

______ step F. now download sequential data to the FLASH RAM

______ step G. verify the sequential download.

Test of downloading Pipeline FPGA from Flash RAM

Select option 10 - Pipeline Download S-Record Test
The program will do the first part automatically except for the file name which is done interactively.

Now, we will download the Flash RAM which will be used to program the Pipeline FPGA.

______ Set the "Enable VMEbus access to Flash RAM data lookup tables" in the Control Register.

______ Write BEAD (hex) to the Access Register for Flash RAM.

______ Write a "1B" to the Flash RAM Select register.

______ Erase the Flash RAM

______ Download Motorola S-records, download the file /network/projects/prod_software/plug1.exo and /network/projects/prod_software/plug2.exo

______ Verify Motorola S-record download

The ADMEM jumpers must now be set to allow for download from the Flash RAM.
To do this,

______ Insert Jumper **S3** (page 16D)

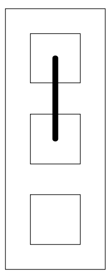
______ Remove Jumper **S5** (page 16A)

______ Install Jumper **S4** (page 16A)

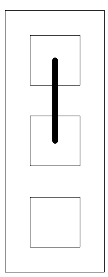
______ Remove Jumpers **S13, S11, S9**, and **S7** (pages 16A-19A)

______ Install Jumpers **S12, S10, S8**, and **S6** (pages 16A-19A)

______ Install Jumpers **J21** and **J22** (page 16A)in the upper position.



______ Leave Jumpers **J18, J19, J20** (page 17A) **J15, J16, J17** (page 18A) **J12, J13, J14** (page 19A) and **J9, J10, J11** (page 20A) in the upper position.



______ When download is complete, toggle the "Program Pipeline" bit high then low in the Control register. When you do this observe **U33-2** for clock activity (it will be brief).

______ Verify that the download is complete, by observing a high on **U33-4**.

______ The front panel READY (green) indicator, **D10** (page16) should be on.

______ Verify that the PLUG (green) indicator, **D11** (page 20A) is on.

______ Now verify Front Panel Reset switch will download the Pipeline FPGA **-** Push the RESET button and observe **U33-2** for clock activity (it will be brief).

______ Verify that the download is complete, by observing a high on **U33-4**.

______ The front panel READY (green) indicator, **D10** (page16) should be on.

______ Verify that the PLUG (green) indicator, **D11** (page 20A) is on.

______ Finally, verify that a power-up reset will produce a proper download. Pull the board out of the crate and re-insert it.

______ The front panel READY (green) indicator, **D10** (page16) should be on.

______ Verify that the PLUG (green) indicator, **D11** (page 20A) is on.

Check PLL

_____ Insert the Testclk Module into slot 4. The TESTCLK jumpers should be set to allow for the backplane clock to be driven.

_____ Turn on the Backplane clock on the TESTCLK.

_____ Observe the following pins on **U66: 10, 11, 14, 15** (page 4). You should observe a 132 ns clock with 50%duty cycle (66ns up, 66ns down) at these pins.

_____ Observe **U66-20.** You should observe a 66 ns clock with 50%duty cycle (33ns up, 33ns down) at these pins.

_____ Connect the Logic Analyzer to the test point TPQIECLK1 (page 4) (located near U101) and have the analyzer trigger on the rising edge of the signal with ACCUMULATE ON and triggering in REPETITIVE mode. There should be no significant shift in the clock signal.

Check of Diagnostic Mode Data

In this test we will pump data from the Diagnostic FIFO into the Pipeline FPGAs. This diagnostic data will be used in place of the data normally coming from CAFÉ modules.

From VASE, Admem Checkout menu, Select option 11 - Diagnostic Mode Data Test
This test is done automatically, user needs to check screen for errors and verification of the below steps:

_____ The Testclk Module is needed for this test. The TESTCLK jumpers should be set to allow for the backplane clock to be driven.

_____ Turn on the Backplane clock on the TESTCLK.

______ Turn on the TSIE Backplane Enable.

______ Turn on the TSIE Wait.

______ Send the tsi pattern /people/tshaw/test_admem/send_halt.tsi

Go to the ADMEM menu

______ set the Pipeline depth to 2A (hex)

______ set the Pipeline offset to 03 (hex)

______ select all channels in the Pipeline Diagnostic Channles Enable Register - (toggle to high)

______ clear the Diagnostic FIFO by issuing a software reset in the Control Register

______ Fill the Diagnostic data with sequential data

______ Turn on the “Enable Diagnostic Pipeline Data” bit in the Control Register.

At the TESTCLK.

______ send the tsi pattern /people/tshaw/test_admem/diag_fifo_test.tsi

At the ADMEM,

______ Dump the L2 buffer information, the data you get should match the following hi-lited text:

Channel	L2 Buffer 0	L2 Buffer 1	L2 Buffer 2	L2 Buffer 3
Header	00001382	00001383	00001384	00001385
0	01C2	01C3	01C4	01C5
1	01C2	01C3	01C4	01C5
2	01C2	01C3	01C4	01C5
3	01C2	01C3	01C4	01C5
4	01C2	01C3	01C4	01C5
5	01C2	01C3	01C4	01C5
6	01C2	01C3	01C4	01C5
7	01C2	01C3	01C4	01C5
8	01C2	01C3	01C4	01C5
9	01C2	01C3	01C4	01C5
10	01C2	01C3	01C4	01C5
11	01C2	01C3	01C4	01C5
12	01C2	01C3	01C4	01C5
13	01C2	01C3	01C4	01C5
14	01C2	01C3	01C4	01C5
15	01C2	01C3	01C4	01C5
16	01C2	01C3	01C4	01C5
17	01C2	01C3	01C4	01C5
18	01C2	01C3	01C4	01C5
19	01C2	01C3	01C4	01C5

Check the readout of the Digital Pipeline

Directly following the above test,

At the TESTCLK,

______ Send the tsi pattern /people/tshaw/test_admem/send_halt.tsi

At the ADMEM,

______ Set the “Enable VMEbus Read of Pipeline data” bit in the Control register

______ Now select the the ADMEM Register option, which allows you to view the contents of the digital pipeline.

Look at all 20 channels. The user will need to do this from the VASE Register Access Menu.

They should contain identical data which is incremented by 1 count for each word.

Check of the Digital Pipeline data with Digital Paddle Cards

For this test, a TESTCLK (capable of driving the backplane clock) must be in the crate.

The ADMEM module must have digital Paddle cards loaded in all 20 slots. The digital Paddle cards should have sequential data loaded in them.

______ First load the ADMEM with Digital Paddle Boards which have been downloaded **with sequential data**.

______ Run the TAM program.

______ Now load the ADMEM with Digital Paddle cards which have been loaded **with pattern data** (AAAA,55555,0000,FFFF)

______ Run the TAM Program.

Quick Check of the Trigger Sums

From VASE in the Checkout Menu, select option 12 **-** Pipeline Trigger Sum Test. Prior to running the test, connect the trigger sum cable as stated below. Thereafter, the program will prompt user to either continue test or quit. At that time the user should change the cable as necessary. The user will need to perform the ADMEM setup individually, the rest is performed by the program.

This test requires the use of a TESTCLK and TSCR.

______ Connect a trigger sum cable from the top (first) connector to the top (first) connector of the TSCR board.

_____ The TESTCLK jumpers should be set to allow for the backplane clock to be driven.

_____ Turn on the Backplane clock on the TESTCLK.

______ Turn on the TSIE Backplane Enable.

______ ADMEM setup, the user will need to do this individually,

  ______ fill CAFÉ Slots PB 18, 19, 20 with “sequential data” digital paddle boards

  ______ fill CAFÉ Slot 17 with “zero data” digital paddle board.

______ TSCR setup,

  ______ from the Control Register, reset the FIFOs

  ______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 300 (hex) locations.

______ Compare readout results to the following results (start with **BOLD** numbers):

Addr								
0000	00D6	00DC	00E2	0000	**0000**	**0001**	**0003**	**0004**
0008	**0006**	**0007**	**0009**	**000A**	**000C**	**000D**	**000F**	**0010**
0010	**0012**	**0013**	**0015**	**0016**	**0018**	**0019**	**001B**	**001C**
0018	**001E**	**001F**	**0021**	**0022**	**0024**	**0025**	**0027**	**0028**
0020	**002A**	**002B**	**002D**	**002E**	**0030**	**0031**	**0033**	**0034**
0028	**0036**	**0037**	**0039**	**003A**	**003C**	**003D**	**003F**	**0040**
0030	**0042**	**0043**	**0045**	**0046**	**0048**	**0049**	**004B**	**004C**
0038	**004E**	**004F**	**0051**	**0052**	**0054**	**0055**	**0057**	**0058**
0040	**005A**	**005B**	**005D**	**005E**	**0060**	**0061**	**0063**	**0064**
0048	**0066**	**0067**	**0069**	**006A**	**006C**	**006D**	**006F**	**0070**
0050	**0072**	**0073**	**0075**	**0076**	**0078**	**0079**	**007B**	**007C**
0058	**007E**	**007F**	**0081**	**0082**	**0084**	**0085**	**0087**	**0088**
0060	**008A**	**008B**	**008D**	**008E**	**0090**	**0091**	**0093**	**0094**
0068	**0096**	**0097**	**0099**	**009A**	**009C**	**009D**	**009F**	**00A0**
0070	**00A2**	**00A3**	**00A5**	**00A6**	**00A8**	**00A9**	**00AB**	**00AC**
0078	**00AE**	**00AF**	**00B1**	**00B2**	**00B4**	**00B5**	**00B7**	**00B8**
0080	**00BA**	**00BB**	**00BD**	**00BE**	**00C0**	**00C1**	**00C3**	**00C4**
0088	**00C6**	**00C7**	**00C9**	**00CA**	**00CC**	**00CD**	**00CF**	**00D0**
0090	**00D2**	**00D3**	**00D5**	**00D6**	**00D8**	**00D9**	**00DB**	**00DC**
0098	**00DE**	**00DF**	**00E1**	**00E2**	**00E4**	**00E5**	**00E7**	**00E8**
00A0	**00EA**	**00EB**	**00ED**	**00EE**	**00F0**	**00F1**	**00F3**	**00F4**
00A8	**00F6**	**00F7**	**00F9**	**00FA**	**00FC**	**00FD**	**00FF**	**0100**
00B0	**0102**	**0103**	**0105**	**0106**	**0108**	**0109**	**010B**	**010C**
00B8	**010E**	**010F**	**0111**	**0112**	**0114**	**0115**	**0117**	**0118**
00C0	**011A**	**011B**	**011D**	**011E**	**0120**	**0121**	**0123**	**0124**
00C8	**0126**	**0127**	**0129**	**012A**	**012C**	**012D**	**012F**	**0130**
00D0	**0132**	**0133**	**0135**	**0136**	**0138**	**0139**	**013B**	**013C**
00D8	**013E**	**013F**	**0141**	**0142**	**0144**	**0145**	**0147**	**0148**
00E0	**014A**	**014B**	**014D**	**014E**	**0150**	**0151**	**0153**	**0154**
00E8	**0156**	**0157**	**0159**	**015A**	**015C**	**015D**	**015F**	**0160**
00F0	**0162**	**0163**	**0165**	**0166**	**0168**	**0169**	**016B**	**016C**
00F8	**016E**	**016F**	**0171**	**0172**	**0174**	**0175**	**0177**	**0178**
0100	**017A**	**017B**	**017D**	**017E**	**0180**	**0181**	**0183**	**0184**
0108	**0186**	**0187**	**0189**	**018A**	**018C**	**018D**	**018F**	**0190**
0110	**0192**	**0193**	**0195**	**0196**	**0198**	**0199**	**019B**	**019C**
0118	**019E**	**019F**	**01A1**	**01A2**	**01A4**	**01A5**	**01A7**	**01A8**
0120	**01AA**	**01AB**	**01AD**	**01AE**	**01B0**	**01B1**	**01B3**	**01B4**
0128	**01B6**	**01B7**	**01B9**	**01BA**	**01BC**	**01BD**	**01BF**	**01C0**
0130	**01C2**	**01C3**	**01C5**	**01C6**	**01C8**	**01C9**	**01CB**	**01CC**
0138	**01CE**	**01CF**	**01D1**	**01D2**	**01D4**	**01D5**	**01D7**	**01D8**
0140	**01DA**	**01DB**	**01DD**	**01DE**	**01E0**	**01E1**	**01E3**	**01E4**
0148	**01E6**	**01E7**	**01E9**	**01EA**	**01EC**	**01ED**	**01EF**	**01F0**
0150	**01F2**	**01F3**	**01F5**	**01F6**	**01F8**	**01F9**	**01FB**	**01FC**
0158	**01FE**	**01FF**	**0201**	**0202**	**0204**	**0205**	**0207**	**0208**
0160	**020A**	**020B**	**020D**	**020E**	**0210**	**0211**	**0213**	**0214**
0168	**0216**	**0217**	**0219**	**021A**	**021C**	**021D**	**021F**	**0220**
0170	**0222**	**0223**	**0225**	**0226**	**0228**	**0229**	**022B**	**022C**
0178	**022E**	**022F**	**0231**	**0232**	**0234**	**0235**	**0237**	**0238**
0180	**023A**	**023B**	**023D**	**023E**	**0240**	**0241**	**0243**	**0244**
0188	**0246**	**0247**	**0249**	**024A**	**024C**	**024D**	**024F**	**0250**
0190	**0252**	**0253**	**0255**	**0256**	**0258**	**0259**	**025B**	**025C**
0198	**025E**	**025F**	**0261**	**0262**	**0264**	**0265**	**0267**	**0268**
01A0	**026A**	**026B**	**026D**	**026E**	**0270**	**0271**	**0273**	**0274**
01A8	**0276**	**0277**	**0279**	**027A**	**027C**	**027D**	**027F**	**0280**
01B0	**0282**	**0283**	**0285**	**0286**	**0288**	**0289**	**028B**	**028C**
01B8	**028E**	**028F**	**0291**	**0292**	**0294**	**0295**	**0297**	**0298**
01C0	**029A**	**029B**	**029D**	**029E**	**02A0**	**02A1**	**02A3**	**02A4**
01C8	**02A6**	**02A7**	**02A9**	**02AA**	**02AC**	**02AD**	**02AF**	**02B0**
01D0	**02B2**	**02B3**	**02B5**	**02B6**	**02B8**	**02B9**	**02BB**	**02BC**
01D8	**02BE**	**02BF**	**02C1**	**02C2**	**02C4**	**02C5**	**02C7**	**02C8**
01E0	**02CA**	**02CB**	**02CD**	**02CE**	**02D0**	**02D1**	**02D3**	**02D4**
01E8	**02D6**	**02D7**	**02D9**	**02DA**	**02DC**	**02DD**	**02DF**	**02E0**
01F0	**02E2**	**02E3**	**02E5**	**02E6**	**02E8**	**02E9**	**02EB**	**02EC**

01F8	02EE	02EF	02F1	02F2	02F4	02F5	02F7	02F8
0200	02FA	02FB	02FD	02FE	0300	0301	0303	0304
0208	0306	0307	0309	030A	030C	030D	030F	0310
0210	0312	0313	0315	0316	0318	0319	031B	031C
0218	031E	031F	0321	0322	0324	0325	0327	0328
0220	032A	032B	032D	032E	0330	0331	0333	0334
0228	0336	0337	0339	033A	033C	033D	033F	0340
0230	0342	0343	0345	0346	0348	0349	034B	034C
0238	034E	034F	0351	0352	0354	0355	0357	0358
0240	035A	035B	035D	035E	0360	0361	0363	0364
0248	0366	0367	0369	036A	036C	036D	036F	0370
0250	0372	0373	0375	0376	0378	0379	037B	037C
0258	037E	037F	0381	0382	0384	0385	0387	0388
0260	038A	038B	038D	038E	0390	0391	0393	0394
0268	0396	0397	0399	039A	039C	039D	039F	03A0
0270	03A2	03A3	03A5	03A6	03A8	03A9	03AB	03AC
0278	03AE	03AF	03B1	03B2	03B4	03B5	03B7	03B8
0280	03BA	03BB	03BD	03BE	03C0	03C1	03C3	03C4
0288	03C6	03C7	03C9	03CA	03CC	03CD	03CF	03D0
0290	03D2	03D3	03D5	03D6	03D8	03D9	03DB	03DC
0298	03DE	03DF	03E1	03E2	03E4	03E5	03E7	03E8
02A0	03EA	03EB	03ED	03EE	03F0	03F1	03F3	03F4
02A8	03F6	03F7	03F9	03FA	03FC	03FD	03FF	0000
02B0	0002	0003	0005	0006	0008	0009	000B	000C
02B8	000E	000F	0011	0012	0014	0015	0017	0018
02C0	001A	001B	001D	001E	0020	0021	0023	0024
02C8	0026	0027	0029	002A	002C	002D	002F	0030
02D0	0032	0033	0035	0036	0038	0039	003B	003C
02D8	003E	003F	0041	0042	0044	0045	0047	0048
02E0	004A	004B	004D	004E	0050	0051	0053	0054
02E8	0056	0057	0059	005A	005C	005D	005F	0060
02F0	0062	0063	0065	0066	0068	0069	006B	006C
02F8	006E	006F	0071	0072	0074	0075	0077	0078

______ ADMEM setup,

- ______ Connect a trigger sum cable from the second (from the top) ADMEM Trigger Sum connector to the top (first) connector of the TSCR board.
- ______ fill CAFÉ Slots PB 14, 15, 16 with "sequential data" digital paddle boards
- ______ fill CAFÉ Slot 13 with "zero data" digital paddle board.

______ TSCR setup,

- ______ from the Control Register, reset the FIFOs
- ______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 300 (hex) locations.

______ Compare readout results to the above results

______ ADMEM setup,

- ______ Connect a trigger sum cable from the third (from the top) ADMEM Trigger Sum connector to the top (first) connector of the TSCR board.
- ______ fill CAFÉ Slots PB 10, 11, 12 with "sequential data" digital paddle boards
- ______ fill CAFÉ Slot 9 with "zero data" digital paddle board.

______ TSCR setup,

- ______ from the Control Register, reset the FIFOs
- ______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 300 (hex) locations.

______ Compare readout results to the above results

______ ADMEM setup,

- ______ Connect a trigger sum cable from the fourth (from the top) ADMEM Trigger Sum connector to the top (first) connector of the TSCR board.
- ______ fill CAFÉ Slots PB 6, 7, 8 with “sequential data” digital paddle boards
- ______ fill CAFÉ Slot 5 with “zero data” digital paddle board.

______ TSCR setup,

- ______ from the Control Register, reset the FIFOs
- ______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 300 (hex) locations.

______ Compare readout results to the above results

______ ADMEM setup,

- ______ Connect a trigger sum cable from the fifth (from the top) ADMEM Trigger Sum connector to the top (first) connector of the TSCR board.
- ______ fill CAFÉ Slots PB 2, 3, 4 with “sequential data” digital paddle boards
- ______ fill CAFÉ Slot 1 with “zero data” digital paddle board.

______ TSCR setup,

- ______ from the Control Register, reset the FIFOs
- ______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 800 (hex) locations.

______ Compare readout results to the below results (start with **BOLD** numbers):

Addr								
0000	039E	03A0	03A2	0000	0000	0000	0001	0001
0008	0002	0002	0003	0003	0004	0004	0005	0005
0010	0006	0006	0007	0007	0008	0008	0009	0009
0018	000A	000A	000B	000B	000C	000C	000D	000D
0020	000E	000E	000F	000F	0010	0010	0011	0011
0028	0012	0012	0013	0013	0014	0014	0015	0015
0030	0016	0016	0017	0017	0018	0018	0019	0019
0038	001A	001A	001B	001B	001C	001C	001D	001D
0040	001E	001E	001F	001F	0020	0020	0021	0021
0048	0022	0022	0023	0023	0024	0024	0025	0025
0050	0026	0026	0027	0027	0028	0028	0029	0029
0058	002A	002A	002B	002B	002C	002C	002D	002D
0060	002E	002E	002F	002F	0030	0030	0031	0031
0068	0032	0032	0033	0033	0034	0034	0035	0035
0070	0036	0036	0037	0037	0038	0038	0039	0039
0078	003A	003A	003B	003B	003C	003C	003D	003D
0080	003E	003E	003F	003F	0040	0040	0041	0041
0088	0042	0042	0043	0043	0044	0044	0045	0045
0090	0046	0046	0047	0047	0048	0048	0049	0049
0098	004A	004A	004B	004B	004C	004C	004D	004D
00A0	004E	004E	004F	004F	0050	0050	0051	0051
00A8	0052	0052	0053	0053	0054	0054	0055	0055
00B0	0056	0056	0057	0057	0058	0058	0059	0059
00B8	005A	005A	005B	005B	005C	005C	005D	005D
00C0	005E	005E	005F	005F	0060	0060	0061	0061
00C8	0062	0062	0063	0063	0064	0064	0065	0065
00D0	0066	0066	0067	0067	0068	0068	0069	0069
00D8	006A	006A	006B	006B	006C	006C	006D	006D
00E0	006E	006E	006F	006F	0070	0070	0071	0071
00E8	0072	0072	0073	0073	0074	0074	0075	0075
00F0	0076	0076	0077	0077	0078	0078	0079	0079
00F8	007A	007A	007B	007B	007C	007C	007D	007D
0100	007E	007E	007F	007F	0080	0080	0081	0081
0108	0082	0082	0083	0083	0084	0084	0085	0085
0110	0086	0086	0087	0087	0088	0088	0089	0089
0118	008A	008A	008B	008B	008C	008C	008D	008D
0120	008E	008E	008F	008F	0090	0090	0091	0091
0128	0092	0092	0093	0093	0094	0094	0095	0095
0130	0096	0096	0097	0097	0098	0098	0099	0099
0138	009A	009A	009B	009B	009C	009C	009D	009D
0140	009E	009E	009F	009F	00A0	00A0	00A1	00A1
0148	00A2	00A2	00A3	00A3	00A4	00A4	00A5	00A5
0150	00A6	00A6	00A7	00A7	00A8	00A8	00A9	00A9
0158	00AA	00AA	00AB	00AB	00AC	00AC	00AD	00AD
0160	00AE	00AE	00AF	00AF	00B0	00B0	00B1	00B1
0168	00B2	00B2	00B3	00B3	00B4	00B4	00B5	00B5
0170	00B6	00B6	00B7	00B7	00B8	00B8	00B9	00B9
0178	00BA	00BA	00BB	00BB	00BC	00BC	00BD	00BD
0180	00BE	00BE	00BF	00BF	00C0	00C0	00C1	00C1
0188	00C2	00C2	00C3	00C3	00C4	00C4	00C5	00C5
0190	00C6	00C6	00C7	00C7	00C8	00C8	00C9	00C9
0198	00CA	00CA	00CB	00CB	00CC	00CC	00CD	00CD
01A0	00CE	00CE	00CF	00CF	00D0	00D0	00D1	00D1
01A8	00D2	00D2	00D3	00D3	00D4	00D4	00D5	00D5
01B0	00D6	00D6	00D7	00D7	00D8	00D8	00D9	00D9
01B8	00DA	00DA	00DB	00DB	00DC	00DC	00DD	00DD
01C0	00DE	00DE	00DF	00DF	00E0	00E0	00E1	00E1
01C8	00E2	00E2	00E3	00E3	00E4	00E4	00E5	00E5
01D0	00E6	00E6	00E7	00E7	00E8	00E8	00E9	00E9
01D8	00EA	00EA	00EB	00EB	00EC	00EC	00ED	00ED
01E0	00EE	00EE	00EF	00EF	00F0	00F0	00F1	00F1
01E8	00F2	00F2	00F3	00F3	00F4	00F4	00F5	00F5
01F0	00F6	00F6	00F7	00F7	00F8	00F8	00F9	00F9

01F8	00FA	00FA	00FB	00FB	00FC	00FC	00FD	00FD
0200	00FE	00FE	00FF	00FF	0100	0100	0101	0101
0208	0102	0102	0103	0103	0104	0104	0105	0105
0210	0106	0106	0107	0107	0108	0108	0109	0109
0218	010A	010A	010B	010B	010C	010C	010D	010D
0220	010E	010E	010F	010F	0110	0110	0111	0111
0228	0112	0112	0113	0113	0114	0114	0115	0115
0230	0116	0116	0117	0117	0118	0118	0119	0119
0238	011A	011A	011B	011B	011C	011C	011D	011D
0240	011E	011E	011F	011F	0120	0120	0121	0121
0248	0122	0122	0123	0123	0124	0124	0125	0125
0250	0126	0126	0127	0127	0128	0128	0129	0129
0258	012A	012A	012B	012B	012C	012C	012D	012D
0260	012E	012E	012F	012F	0130	0130	0131	0131
0268	0132	0132	0133	0133	0134	0134	0135	0135
0270	0136	0136	0137	0137	0138	0138	0139	0139
0278	013A	013A	013B	013B	013C	013C	013D	013D
0280	013E	013E	013F	013F	0140	0140	0141	0141
0288	0142	0142	0143	0143	0144	0144	0145	0145
0290	0146	0146	0147	0147	0148	0148	0149	0149
0298	014A	014A	014B	014B	014C	014C	014D	014D
02A0	014E	014E	014F	014F	0150	0150	0151	0151
02A8	0152	0152	0153	0153	0154	0154	0155	0155
02B0	0156	0156	0157	0157	0158	0158	0159	0159
02B8	015A	015A	015B	015B	015C	015C	015D	015D
02C0	015E	015E	015F	015F	0160	0160	0161	0161
02C8	0162	0162	0163	0163	0164	0164	0165	0165
02D0	0166	0166	0167	0167	0168	0168	0169	0169
02D8	016A	016A	016B	016B	016C	016C	016D	016D
02E0	016E	016E	016F	016F	0170	0170	0171	0171
02E8	0172	0172	0173	0173	0174	0174	0175	0175
02F0	0176	0176	0177	0177	0178	0178	0179	0179
02F8	017A	017A	017B	017B	017C	017C	017D	017D
0300	017E	017E	017F	017F	0180	0180	0181	0181
0308	0182	0182	0183	0183	0184	0184	0185	0185
0310	0186	0186	0187	0187	0188	0188	0189	0189
0318	018A	018A	018B	018B	018C	018C	018D	018D
0320	018E	018E	018F	018F	0190	0190	0191	0191
0328	0192	0192	0193	0193	0194	0194	0195	0195
0330	0196	0196	0197	0197	0198	0198	0199	0199
0338	019A	019A	019B	019B	019C	019C	019D	019D
0340	019E	019E	019F	019F	01A0	01A0	01A1	01A1
0348	01A2	01A2	01A3	01A3	01A4	01A4	01A5	01A5
0350	01A6	01A6	01A7	01A7	01A8	01A8	01A9	01A9
0358	01AA	01AA	01AB	01AB	01AC	01AC	01AD	01AD
0360	01AE	01AE	01AF	01AF	01B0	01B0	01B1	01B1
0368	01B2	01B2	01B3	01B3	01B4	01B4	01B5	01B5
0370	01B6	01B6	01B7	01B7	01B8	01B8	01B9	01B9
0378	01BA	01BA	01BB	01BB	01BC	01BC	01BD	01BD
0380	01BE	01BE	01BF	01BF	01C0	01C0	01C1	01C1
0388	01C2	01C2	01C3	01C3	01C4	01C4	01C5	01C5
0390	01C6	01C6	01C7	01C7	01C8	01C8	01C9	01C9
0398	01CA	01CA	01CB	01CB	01CC	01CC	01CD	01CD
03A0	01CE	01CE	01CF	01CF	01D0	01D0	01D1	01D1
03A8	01D2	01D2	01D3	01D3	01D4	01D4	01D5	01D5
03B0	01D6	01D6	01D7	01D7	01D8	01D8	01D9	01D9
03B8	01DA	01DA	01DB	01DB	01DC	01DC	01DD	01DD
03C0	01DE	01DE	01DF	01DF	01E0	01E0	01E1	01E1
03C8	01E2	01E2	01E3	01E3	01E4	01E4	01E5	01E5
03D0	01E6	01E6	01E7	01E7	01E8	01E8	01E9	01E9
03D8	01EA	01EA	01EB	01EB	01EC	01EC	01ED	01ED
03E0	01EE	01EE	01EF	01EF	01F0	01F0	01F1	01F1
03E8	01F2	01F2	01F3	01F3	01F4	01F4	01F5	01F5
03F0	01F6	01F6	01F7	01F7	01F8	01F8	01F9	01F9

03F8	01FA	01FA	01FB	01FB	01FC	01FC	01FD	01FD
0400	01FE	01FE	01FF	01FF	0200	0200	0201	0201
0408	0202	0202	0203	0203	0204	0204	0205	0205
0410	0206	0206	0207	0207	0208	0208	0209	0209
0418	020A	020A	020B	020B	020C	020C	020D	020D
0420	020E	020E	020F	020F	0210	0210	0211	0211
0428	0212	0212	0213	0213	0214	0214	0215	0215
0430	0216	0216	0217	0217	0218	0218	0219	0219
0438	021A	021A	021B	021B	021C	021C	021D	021D
0440	021E	021E	021F	021F	0220	0220	0221	0221
0448	0222	0222	0223	0223	0224	0224	0225	0225
0450	0226	0226	0227	0227	0228	0228	0229	0229
0458	022A	022A	022B	022B	022C	022C	022D	022D
0460	022E	022E	022F	022F	0230	0230	0231	0231
0468	0232	0232	0233	0233	0234	0234	0235	0235
0470	0236	0236	0237	0237	0238	0238	0239	0239
0478	023A	023A	023B	023B	023C	023C	023D	023D
0480	023E	023E	023F	023F	0240	0240	0241	0241
0488	0242	0242	0243	0243	0244	0244	0245	0245
0490	0246	0246	0247	0247	0248	0248	0249	0249
0498	024A	024A	024B	024B	024C	024C	024D	024D
04A0	024E	024E	024F	024F	0250	0250	0251	0251
04A8	0252	0252	0253	0253	0254	0254	0255	0255
04B0	0256	0256	0257	0257	0258	0258	0259	0259
04B8	025A	025A	025B	025B	025C	025C	025D	025D
04C0	025E	025E	025F	025F	0260	0260	0261	0261
04C8	0262	0262	0263	0263	0264	0264	0265	0265
04D0	0266	0266	0267	0267	0268	0268	0269	0269
04D8	026A	026A	026B	026B	026C	026C	026D	026D
04E0	026E	026E	026F	026F	0270	0270	0271	0271
04E8	0272	0272	0273	0273	0274	0274	0275	0275
04F0	0276	0276	0277	0277	0278	0278	0279	0279
04F8	027A	027A	027B	027B	027C	027C	027D	027D
0500	027E	027E	027F	027F	0280	0280	0281	0281
0508	0282	0282	0283	0283	0284	0284	0285	0285
0510	0286	0286	0287	0287	0288	0288	0289	0289
0518	028A	028A	028B	028B	028C	028C	028D	028D
0520	028E	028E	028F	028F	0290	0290	0291	0291
0528	0292	0292	0293	0293	0294	0294	0295	0295
0530	0296	0296	0297	0297	0298	0298	0299	0299
0538	029A	029A	029B	029B	029C	029C	029D	029D
0540	029E	029E	029F	029F	02A0	02A0	02A1	02A1
0548	02A2	02A2	02A3	02A3	02A4	02A4	02A5	02A5
0550	02A6	02A6	02A7	02A7	02A8	02A8	02A9	02A9
0558	02AA	02AA	02AB	02AB	02AC	02AC	02AD	02AD
0560	02AE	02AE	02AF	02AF	02B0	02B0	02B1	02B1
0568	02B2	02B2	02B3	02B3	02B4	02B4	02B5	02B5
0570	02B6	02B6	02B7	02B7	02B8	02B8	02B9	02B9
0578	02BA	02BA	02BB	02BB	02BC	02BC	02BD	02BD
0580	02BE	02BE	02BF	02BF	02C0	02C0	02C1	02C1
0588	02C2	02C2	02C3	02C3	02C4	02C4	02C5	02C5
0590	02C6	02C6	02C7	02C7	02C8	02C8	02C9	02C9
0598	02CA	02CA	02CB	02CB	02CC	02CC	02CD	02CD
05A0	02CE	02CE	02CF	02CF	02D0	02D0	02D1	02D1
05A8	02D2	02D2	02D3	02D3	02D4	02D4	02D5	02D5
05B0	02D6	02D6	02D7	02D7	02D8	02D8	02D9	02D9
05B8	02DA	02DA	02DB	02DB	02DC	02DC	02DD	02DD
05C0	02DE	02DE	02DF	02DF	02E0	02E0	02E1	02E1
05C8	02E2	02E2	02E3	02E3	02E4	02E4	02E5	02E5
05D0	02E6	02E6	02E7	02E7	02E8	02E8	02E9	02E9
05D8	02EA	02EA	02EB	02EB	02EC	02EC	02ED	02ED
05E0	02EE	02EE	02EF	02EF	02F0	02F0	02F1	02F1
05E8	02F2	02F2	02F3	02F3	02F4	02F4	02F5	02F5
05F0	02F6	02F6	02F7	02F7	02F8	02F8	02F9	02F9

05F8	02FA	02FA	02FB	02FB	02FC	02FC	02FD	02FD
0600	02FE	02FE	02FF	02FF	0300	0300	0301	0301
0608	0302	0302	0303	0303	0304	0304	0305	0305
0610	0306	0306	0307	0307	0308	0308	0309	0309
0618	030A	030A	030B	030B	030C	030C	030D	030D
0620	030E	030E	030F	030F	0310	0310	0311	0311
0628	0312	0312	0313	0313	0314	0314	0315	0315
0630	0316	0316	0317	0317	0318	0318	0319	0319
0638	031A	031A	031B	031B	031C	031C	031D	031D
0640	031E	031E	031F	031F	0320	0320	0321	0321
0648	0322	0322	0323	0323	0324	0324	0325	0325
0650	0326	0326	0327	0327	0328	0328	0329	0329
0658	032A	032A	032B	032B	032C	032C	032D	032D
0660	032E	032E	032F	032F	0330	0330	0331	0331
0668	0332	0332	0333	0333	0334	0334	0335	0335
0670	0336	0336	0337	0337	0338	0338	0339	0339
0678	033A	033A	033B	033B	033C	033C	033D	033D
0680	033E	033E	033F	033F	0340	0340	0341	0341
0688	0342	0342	0343	0343	0344	0344	0345	0345
0690	0346	0346	0347	0347	0348	0348	0349	0349
0698	034A	034A	034B	034B	034C	034C	034D	034D
06A0	034E	034E	034F	034F	0350	0350	0351	0351
06A8	0352	0352	0353	0353	0354	0354	0355	0355
06B0	0356	0356	0357	0357	0358	0358	0359	0359
06B8	035A	035A	035B	035B	035C	035C	035D	035D
06C0	035E	035E	035F	035F	0360	0360	0361	0361
06C8	0362	0362	0363	0363	0364	0364	0365	0365
06D0	0366	0366	0367	0367	0368	0368	0369	0369
06D8	036A	036A	036B	036B	036C	036C	036D	036D
06E0	036E	036E	036F	036F	0370	0370	0371	0371
06E8	0372	0372	0373	0373	0374	0374	0375	0375
06F0	0376	0376	0377	0377	0378	0378	0379	0379
06F8	037A	037A	037B	037B	037C	037C	037D	037D
0700	037E	037E	037F	037F	0380	0380	0381	0381
0708	0382	0382	0383	0383	0384	0384	0385	0385
0710	0386	0386	0387	0387	0388	0388	0389	0389
0718	038A	038A	038B	038B	038C	038C	038D	038D
0720	038E	038E	038F	038F	0390	0390	0391	0391
0728	0392	0392	0393	0393	0394	0394	0395	0395
0730	0396	0396	0397	0397	0398	0398	0399	0399
0738	039A	039A	039B	039B	039C	039C	039D	039D
0740	039E	039E	039F	039F	03A0	03A0	03A1	03A1
0748	03A2	03A2	03A3	03A3	03A4	03A4	03A5	03A5
0750	03A6	03A6	03A7	03A7	03A8	03A8	03A9	03A9
0758	03AA	03AA	03AB	03AB	03AC	03AC	03AD	03AD
0760	03AE	03AE	03AF	03AF	03B0	03B0	03B1	03B1
0768	03B2	03B2	03B3	03B3	03B4	03B4	03B5	03B5
0770	03B6	03B6	03B7	03B7	03B8	03B8	03B9	03B9
0778	03BA	03BA	03BB	03BB	03BC	03BC	03BD	03BD
0780	03BE	03BE	03BF	03BF	03C0	03C0	03C1	03C1
0788	03C2	03C2	03C3	03C3	03C4	03C4	03C5	03C5
0790	03C6	03C6	03C7	03C7	03C8	03C8	03C9	03C9
0798	03CA	03CA	03CB	03CB	03CC	03CC	03CD	03CD
07A0	03CE	03CE	03CF	03CF	03D0	03D0	03D1	03D1
07A8	03D2	03D2	03D3	03D3	03D4	03D4	03D5	03D5
07B0	03D6	03D6	03D7	03D7	03D8	03D8	03D9	03D9
07B8	03DA	03DA	03DB	03DB	03DC	03DC	03DD	03DD
07C0	03DE	03DE	03DF	03DF	03E0	03E0	03E1	03E1
07C8	03E2	03E2	03E3	03E3	03E4	03E4	03E5	03E5
07D0	03E6	03E6	03E7	03E7	03E8	03E8	03E9	03E9
07D8	03EA	03EA	03EB	03EB	03EC	03EC	03ED	03ED
07E0	03EE	03EE	03EF	03EF	03F0	03F0	03F1	03F1
07E8	03F2	03F2	03F3	03F3	03F4	03F4	03F5	03F5
07F0	03F6	03F6	03F7	03F7	03F8	03F8	03F9	03F9

07F8	**03FA**	**03FA**	**03FB**	**03FB**	**03FC**	**03FC**	**03FD**	**03FD**
0800	**03FE**	**03FE**	**03FF**	**03FF**	**0000**	**0000**	**0001**	**0001**

______ ADMEM setup,

______ Connect a trigger sum cable from the sixth (from the top) ADMEM Trigger Sum connector to the top (first) connector of the TSCR board.

______ TSCR setup,

______ from the Control Register, reset the FIFOs

______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 800 (hex) locations.

______ Compare readout results to the above results

______ ADMEM setup,

______ Connect a trigger sum cable from the seventh (bottom) ADMEM Trigger Sum connector to the top (first) connector of the TSCR board.

______ TSCR setup,

______ from the Control Register, reset the FIFOs

______ make sure VMEbus access to the FIFOs is NOT enabled (should be zero).

______ From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi

______ Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs

______ Note that the TSCR FIFOs should all read Full

______ Go to the TSCR FIFO access menu, use option 8 to read out 800 (hex) locations.

______ Compare readout results to the above results

Test of Signals from Mezzanine Card

The following tests make use of a specially adapted Digital Paddle Board with wired on test points.

______ With the Special Digital Paddle Board inserted in PB20, observe the signals CAFÉ_PATH_SEL, CAFÉ_SMON_ENABLE, and CAFÉ_CAL_EN1.

______ Writing to the CAFÉ Control register, verify that you can

  ______ Toggle CAFÉ_PATH_SEL

  ______ Toggle CAFÉ_SMON_ENABLE

  ______ Toggle CAFÉ_CAL_EN1 (observe CAFÉ_CAL_EN)

______ Move the Special Digital Paddle Board to PB15.

  ______ Toggle CAFÉ_CAL_EN2 (observe CAFÉ_CAL_EN)

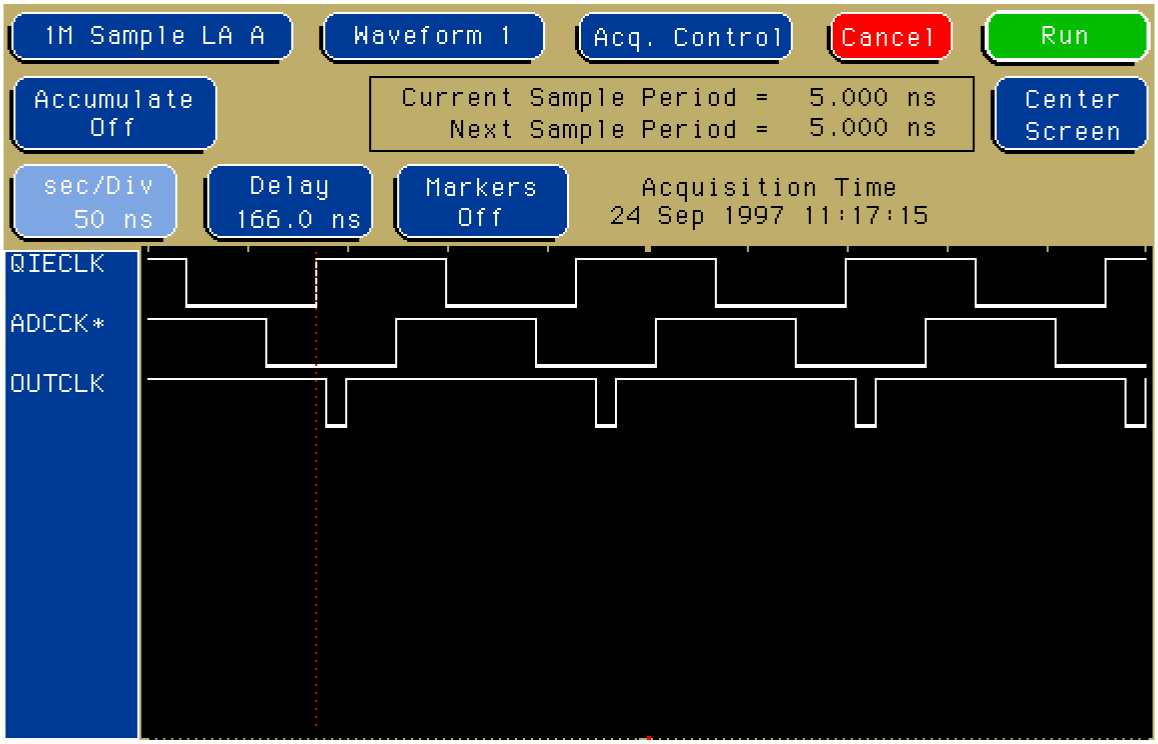
______ Move the Special Digital Paddle Board to PB10.

  ______ Toggle CAFÉ_CAL_EN3 (observe CAFÉ_CAL_EN)

______ Move the Special Digital Paddle Board to PB55.

  ______ Toggle CAFÉ_CAL_EN4 (observe CAFÉ_CAL_EN)

Now, with the TESTCLK driving the backplane clock, Observe the below signals. Trigger the LA on QIE_CLOCK and verify that the clock signals you observe match the picture.



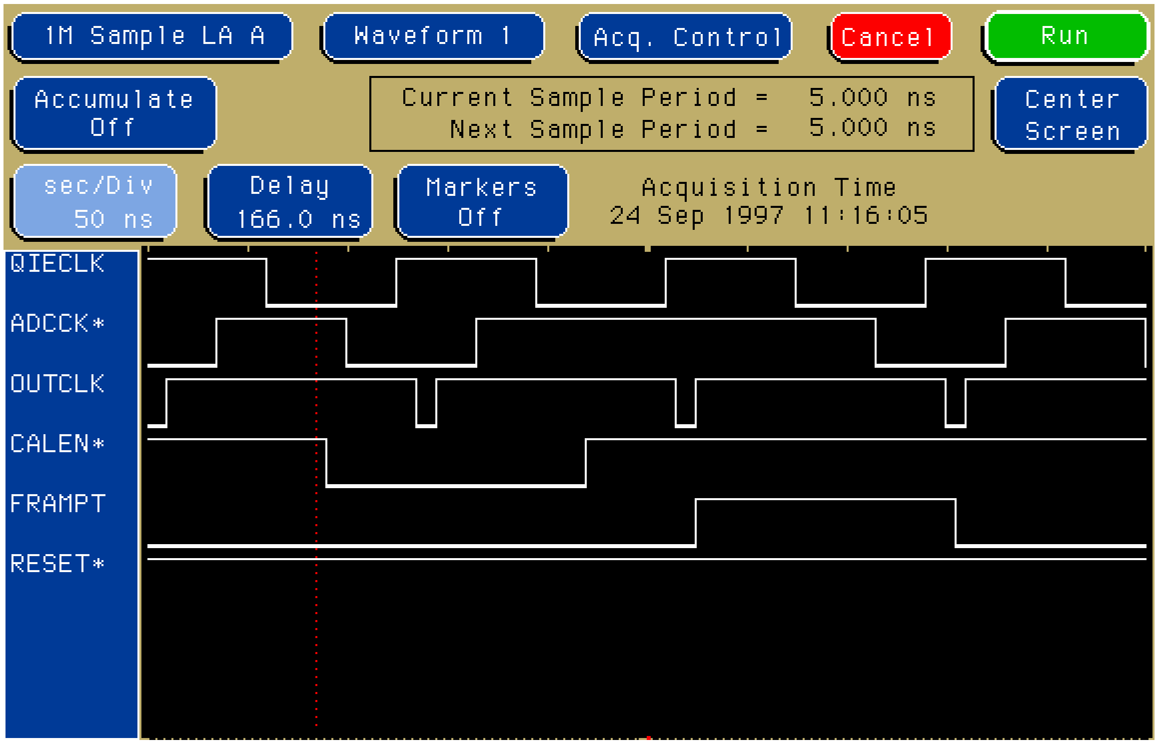
The Next step requires you observe the additional signals below.

______ The TESTCLK must be on, with the backplane clock running.

______ The TSIE Backplane driver must be enabled.

______ The TSI pattern /people/tshaw/test_admem/send_cal.tsi must be sent.

______ You must trigger on the falling edge of CALEN* (test point labled as "1") and should observe the following waveforms. NOTE the missing ADCCK* following a calibration.



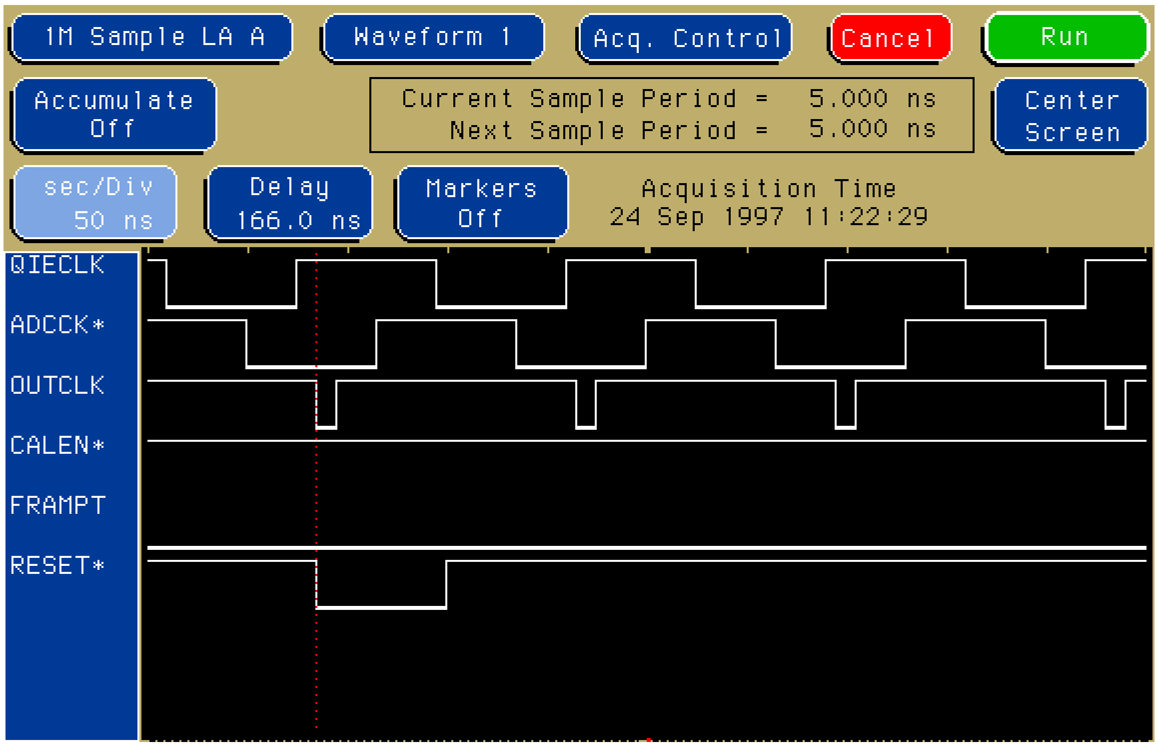
The Next step requires you observe the RESET* signal to the CAFÉ modules.

______ The TESTCLK must be on, with the backplane clock running.

______ The TSIE Backplane driver must be enabled.

______ The TSI pattern /people/tshaw/test_admem/h_r_r.tsi must be sent.

______ You must trigger on the falling edge of RESET* and should observe the following waveforms. NOTE the missing ADCCK* following a calibration.



Testing the DAC

To test the DAC on the mezzanine module, you must be in a crate which provides the analog voltages.

______ Go to the Analog Admem's functional submenu.

______ Make sure the DAC is calibrated **-** DAC CAL OK should be high. If it is not, within the DAC Control Register

1) set the CS low,
2) set the CALIBRATE bit low,
3) set the CALIBRATE bit high,
4) then set the CS high.

The DAC CAL_OK bit should now be high.

______ Download a "0" to the DAC, and observe the voltage on pin 62 of a Café Module slot. The voltage should be around 0 volts.

______ Download a "FFFF" to the DAC, and observe the voltage on pin 62 of a Café Module slot. The voltage should be around 10 volts.

______ Download a "8000" to the DAC, and observe the voltage on pin 62 of a Café Module slot. The voltage should be around 5 volts.

Other Tests

How do we test connection of Analog signal to PB slots?

Check with real CAFE? requires Analog power