

Optical Flatness Metrology for 300 mm Silicon Wafers

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Abstract. The National Institute of Standards and Technology (NIST) is developing two interferometric methods for measuring the thickness, thickness variation, and flatness of free-standing and chucked silicon wafers with diameters up to 300 mm. The “eXtremely accurate CALIBration InterferometerR” (XCALIBIR) is a precision phase measuring interferometer with an operating wavelength of 633 nm and a test beam of 300 mm diameter. XCALIBIR is used to evaluate the flatness of chucked wafers. NIST’s Infrared Interferometer (IR²) is a phase measuring interferometer that operates at 1.55 μm and is used to measure the thickness variation of free-standing 300 mm silicon wafers.

Keywords: 300 mm silicon wafers, wafer thickness variation (TTV and GBIR), wafer flatness

PACS: 42.70.Km, 07.60.Ly

INTRODUCTION

This paper describes interferometric tools and methods for the characterization of flatness, thickness variation, and nanotopography of 300 mm silicon wafers. The International Technology Roadmap for Semiconductors (ITRS) [1] projects a die site flatness requirement of ≤ 51 nm and a nanotopography requirement of ≤ 13 nm by 2010. (Nanotopography is the component of the flatness error with spatial frequencies below 0.05 mm^{-1} .) These stringent requirements for wafer flatness at the exposure site are imposed by the physics of the lithography process. For diffraction limited exposure objectives, the minimum linewidth L is determined by the exposure wavelength λ and numerical aperture NA :

$$L = k_1 \frac{\lambda}{NA}, \quad (1)$$

where k_1 is a process dependent factor. The desire to create smaller integrated circuit features thus compels a move to shorter wavelengths and larger numerical apertures in exposure tools. The depth of focus D ,

$$D = k_2 \frac{\lambda}{NA^2}, \quad (2)$$

is thereby reduced, which - in turn - limits the allowable flatness variation at the exposure site. Again, k_2 is a process dependent factor. The tight limits on flatness and nanotopography create new challenges at

two stages in the integrated circuit (IC) manufacturing process. Wafer manufacturers must improve the polishing processes to meet the requirements for wafer flatness and nanotopography. Manufacturers of wafer testing equipment must create tools that allow measurement of flatness and nanotopography with sufficient accuracy and spatial resolution. Optical tools are therefore beginning to replace wafer flatness metrology tools based on capacitance gages. Our research addresses the needs of both wafer manufacturers and wafer testing equipment manufacturers for 300 mm wafers with calibrated thickness variation, measured with low uncertainty, that can be used for calibration and validation purposes.

The wafer flatness at the exposure site is determined by the flatness of the wafer chuck, the Total Thickness Variation (TTV), or Global Back Ideal Range (GBIR), of the chucked wafer, and any deformation caused by the forces that make the wafer conform to the chuck. In the following sections, we describe the “eXtremely accurate CALIBration InterferometerR” (XCALIBIR) at the National Institute of Standards and Technology (NIST). This interferometer measures flatness and nanotopography of free-standing and chucked silicon wafers with diameters up to 300 mm. We also describe the NIST Infrared Interferometer (IR²) which measures the thickness of low-doped silicon wafers up to 300 mm diameter.

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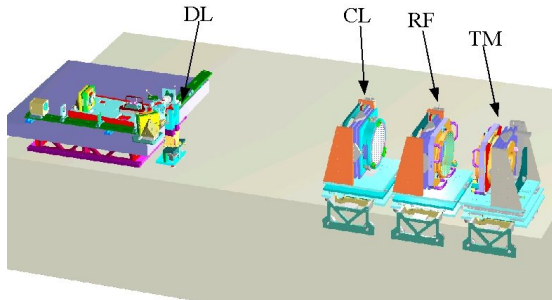


FIGURE 1. XCALIBIR interferometer configured for flatness measurements. The main components of the interferometer, from left to right, are: breadboard with source and imaging optics, diverger lens (DL), collimator lens (CL), reference flat (RF), and test mount (TM). For silicon wafer flatness measurements a wafer chuck was mounted on the test mount.

THE XCALIBIR INTERFEROMETER

A solid model of the interferometer is shown in Figure 1. The interferometer is built on a granite table. Source and imaging components of the interferometer are set up on an elevated optical breadboard to create sufficient clearance for the testing of large parts. Light from the laser source is delivered to the interferometer with optical fibers. An off-axis parabolic mirror collimates the center of the light cone that is emitted by the optical fiber and creates a collimated beam parallel to the top surface of the granite table. A beam splitter directs a fraction of the return beam from the part under test to the imaging arm of the interferometer and the camera. A beam expander, consisting of an f/4 diverger lens and an f/4 collimator lens, creates a collimated test beam with a diameter of just over 300 mm. For the measurements described here, an uncoated 300 mm reference flat is used to set up the Fizeau interferometer that is shown in Figure 1. XCALIBIR is an interferometer designed for the light from a He-Ne laser at 632.8 nm. At this wavelength silicon is not transparent. Therefore, the interferometer is well suited for measurements of the flatness of chucked wafers and to evaluate wafer surface deformations caused by the interaction with the wafer chuck. For the measurement of chucking deformations a ceramic pin chuck was installed on the test mount of the interferometer. When measuring a silicon wafer against the uncoated reference flat, the fringe visibility is approximately 0.5 which permits surface height measurements with an uncertainty of about 1 nm *rms*. XCALIBIR is housed in a class 1000 clean room which is maintained at a temperature of $(20 \pm 0.02)^\circ\text{C}$ to achieve the necessary structural stability.

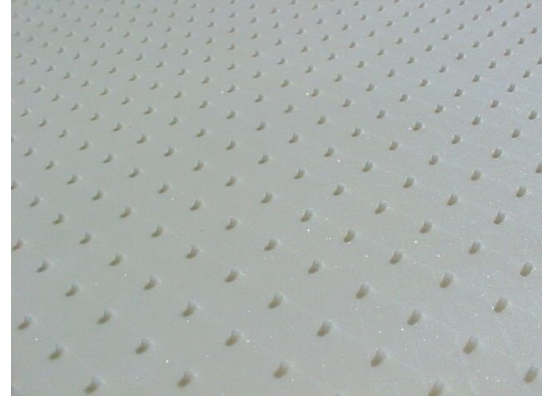


FIGURE 2. 300 mm ceramic pin vacuum chuck surface detail. The chuck is machined from alumina. The pins have a cross section of $1\text{ mm} \times 1\text{ mm}$ and are 1 mm high. They are located on a square grid with a spacing of 6 mm.

WAFERS ON PIN CHUCKS

Wafer chucks are critical components of lithography exposure systems and consequently the details of chuck designs are usually held proprietary. However, some features of vacuum chuck designs are common because they address problems that every chuck design must overcome. For example, many designs attempt to minimize the contact area between chuck and wafer surfaces to make it less likely that particle contamination between chuck and wafer will create bumps on the wafer surface. One type of vacuum chuck with low contact area is a ceramic pin chuck like the one shown in Figure 2. With this chuck the wafer rests on small, 1 mm high ceramic pins that have a $1\text{ mm} \times 1\text{ mm}$ cross section. Two problems of pin chuck designs are immediately obvious. One is that it is very difficult to measure the flatness of the chuck surface directly. Although the pin tops are polished, interferometry cannot be used to measure the flatness

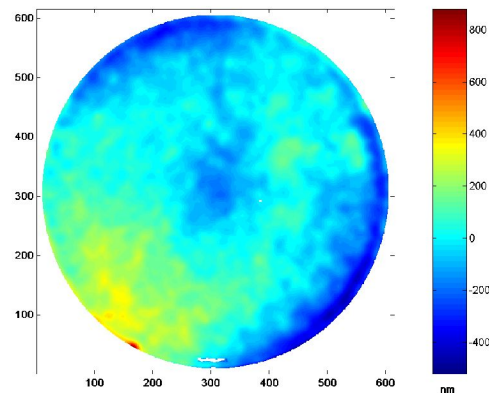


FIGURE 3. Flatness error of a 200 mm silicon wafer on a ceramic pin vacuum chuck measured with XCALIBIR. The height unit is nm. The peak-to-valley flatness error of the chucked wafer is approximately $1\text{ }\mu\text{m}$.

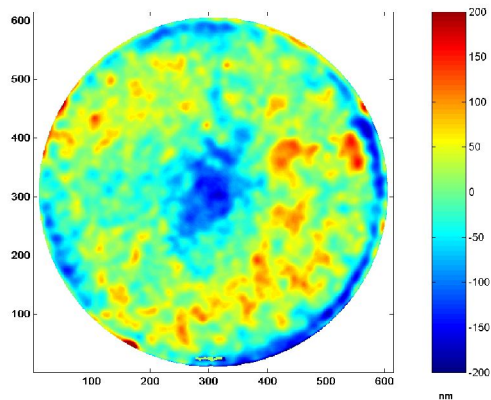


FIGURE 4. Nanotopography of the chucked wafer shown in Figure 3. The height unit is nm. The coordinates in x- and y-direction are pixel numbers. The diameter of the wafer is 200 mm.

because the pins are not connected. Pin chucks can also make it difficult to simultaneously achieve good wafer flatness and good nanotopography. Good flatness requires the application of sufficient force to ensure that the wafer, which may have considerable bow, rests on all pins. The wafer will then sag between the pins and a nanotopography error with the period of the pin spacing is introduced.

We have investigated the geometry of silicon wafers on pin chucks. Figure 3 shows a 200 mm diameter silicon wafer on a ceramic pin vacuum chuck similar to the one shown in Figure 2. The flatness error shown in Figure 3 is a combination of the flatness error of the vacuum chuck and the thickness variation of the chucked wafer. The nanotopography of the chucked wafer surface was calculated from the flatness error measurement by high-pass filtering and is shown in Figure 4. Clearly, the pin chuck causes considerable deformation at higher spatial frequencies. The data shown in Figures 3 and 4 were used to validate a finite-element model of the wafer on the pin chuck. The numerical model can be employed to optimize the location of wafer support pins and chucking conditions to minimize the deformation of the chucked wafer.

THE IR² INTERFEROMETER

Silicon is transparent for light at wavelengths larger than 1.1 μm if the dopant concentration is sufficiently low. The thickness variation of wafers made from such silicon, or other infrared optical materials, can then be characterized using optical interferometry with wavelengths $>1.1 \mu\text{m}$ which is known to achieve very low measurement uncertainties. For the NIST Infrared

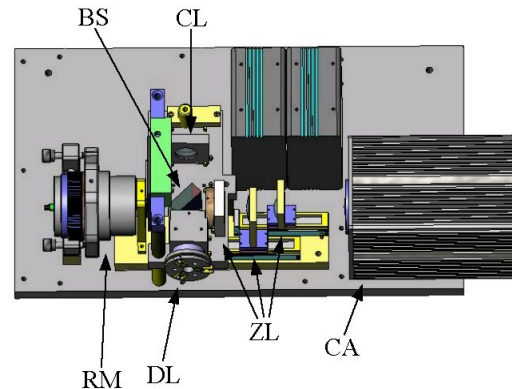


FIGURE 5. NIST's Infrared Interferometer (IR²). The main components of the interferometer are: collimator lens (CL), polarizing beam splitter (BS), phase-shifting reference mirror mount (RM), diverger lens (DL), zoom lens system (ZL), and camera (CA).



FIGURE 6. Test end of the IR² setup for TTV measurements of 300 mm wafers. The picture shows the collimator lens together with a silicon wafer and a return flat.

Interferometer (IR²) an operating wavelength of 1.552 μm was chosen. At this wavelength, which is within the C-band of fiber-optics communication, powerful lasers are readily available. A solid model of the IR² interferometer is shown in Figure 5. Light from a single frequency diode laser is delivered to the interferometer through a polarization maintaining fiber. After collimation, a polarizing beam splitter creates a reference beam that is directed to the phase-shifting reference mount and a test beam that is turned into an $f/3$ diverging light cone by a diverger lens. A large collimating lens, shown in Figures 6 and 7, generates the collimated test beam that is needed to make full-aperture measurements of 300 mm wafers. The return beams from the test and reference arms are sent to the camera by the beam splitter, and an image of the wafer is created at the detector array. Further details of earlier versions of IR² and applications to wafer thickness variation measurements have been published by Schmitz *et al.* [2] and Parks *et al.* [3].

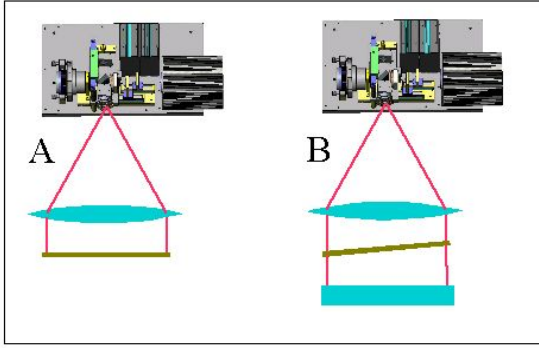


FIGURE 7. Two configurations of the IR² interferometer for wafer TTV measurements. A is a Fizeau configuration with the wafer as interferometer cavity, B is a Twyman-Green interferometer configuration.

IR² is a flexible tool that can be set up in a number of ways for wafer characterizations. Figure 7 shows two different setups of IR² for measuring the total thickness variation (TTV) of wafers. In the Fizeau configuration A the interferometer's test beam is expanded to 300 mm by a collimator lens. The wafer itself becomes the Fizeau cavity of the interferometer. Reflections from both wafer surfaces are returned to the interferometer and brought to interference. In this configuration, phase-shifting interferometry is implemented by varying the wavelength of the laser. The thickness variation can be calculated from the interference fringes if the refractive index of the wafer is known. Obviously, this measurement method can only be applied when the wafer under test is polished on both sides. When the wafer under test is only polished on one side, the thickness variation can still be measured with the Twyman-Green configuration B. This setup is similar to setup A, but the wafer is slightly tilted to prevent light reflected by the wafer from returning to the interferometer. Instead, the test beam is returned to the interferometer with a return flat after passing through the wafer a second time. Phase-shifting in this configuration is done mechanically by moving the Twyman-Green reference mirror. Two measurements are now required, one with the wafer in the interferometer and one without. These are subtracted, and the thickness variation can be calculated once the refractive index is known.

WAFER TTV

We have used IR² to measure the TTV of 300 mm diameter silicon wafers. Most of our TTV measurements were made using method B of Figure 7. The TTV is:

$$TTV = \frac{1}{2} \frac{O_e - O_w}{n_{Si} - 1} \quad (3)$$

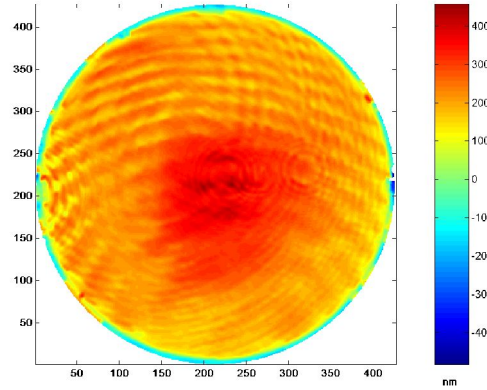


FIGURE 8. Thickness variation (TTV) of a 300 mm double-side polished silicon wafer measured with IR². The height unit is nm. (The coordinates in x- and y- direction are pixel numbers.)

where O_e is the optical path difference for the empty interferometer, O_w the optical path difference with wafer inserted and n_{Si} the refractive index of silicon at $1.552 \mu\text{m}$ [4]. Figure 8 represents the thickness variation of a low-doped 300 mm double-side polished silicon wafer. With the exception of the wafer edge, where roll-off is clearly visible, the thickness of the wafer varies only by approximately 400 nm peak-to-valley. The ripples visible in Figure 8 are artifacts that are caused by internal reflections in the interferometer. This limits the uncertainty for thickness variation at each pixel to about 200 nm. Our current work with IR² is concentrating on reducing the measurement uncertainty by eliminating measurement artifacts in the interferometer.

ACKNOWLEDGMENTS

We gratefully acknowledge financial support by NIST's Office of Microelectronics Programs (OMP) and unfailing encouragement by its directors Dr. Stephen Knight and Dr. Joaquin V. Martinez. We thank Dr. Paul Langer, Komatsu Inc., for 300 mm wafers. Prof. Z. J. Pei, Kansas State University, has never hesitated to answer our many questions about wafer grinding and polishing.

This publication was prepared by a Guest Researcher with the United States Government, was funded through Government support, and is, therefore, a work of the U.S. Government and not subject to copyright.

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