Fermilab

Accelerator Division
BLM Upgrade Proposal

Preliminary Testing of the Burr Brown ACF2101

Summary of Test Data

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03/23/2004

New BLM Front-end Electronics using the ACF2101 Dual Integrator.

The plan for the new BLM system is to use the Burr-Brown ACF2101 dual integrator, and to "ping-pong" (switch rapidly) between the A and B channels so as to never miss any losses. The integration times are planned to be 20 μsec minimum. Significant features and a diagram (shown in Figure 1.) of the ACF2101 device are from the Burr-Brown datasheet and given below.

DESCRIPTION

The ACF2101 is a dual switched integrator for precision applications. Each channel can convert an input current to an output voltage by integration, using either an internal or external capacitor. Included on the chip are precision 100 pF integration capacitors, hold and reset switches, and output multiplexers.

FEATURES

Includes Integration Capacitor, Reset and Hold Switches, and Output Multiplexer
Low Noise: 10 μVrms
Low Charge Transfer: 0.1 pC
Wide Dynamic Range: 120 dB
Low Bias Current: 100 fA

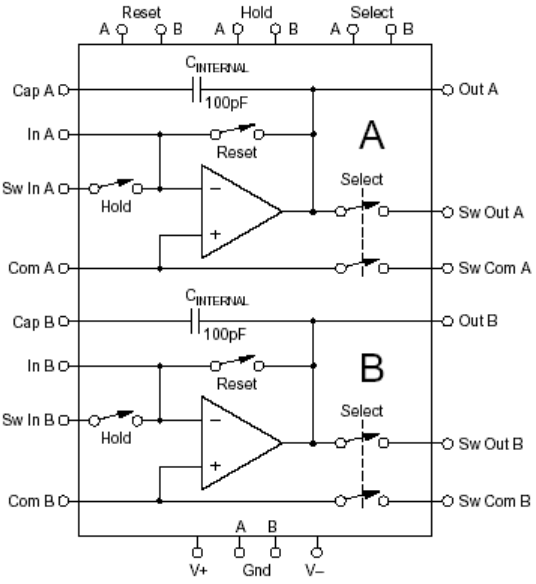

Figure 1. The Burr-Brown ACF2101

The ASIC Test System shown in Figure 2 was used as convenient platform for conducting the initial tests of the Burr-Brown dual integrator. The system provided all of the necessary timing and control signals, plus power supply voltages. It also allowed easy collection and processing of test data on a standard PC.

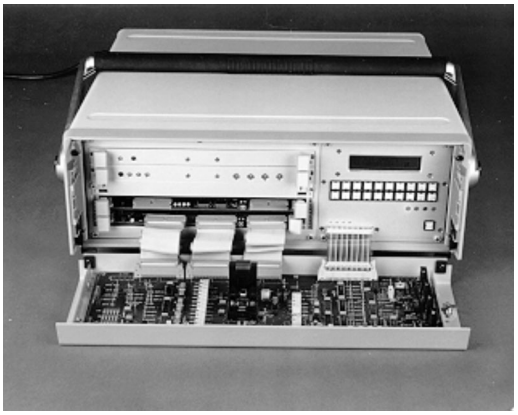

Figure 2. The ASIC Test System

An existing BLM system daughter card (Beam Line) was obtained from the Accelerator Division Instrumentation Department and used for all testing. The card had several modifications made to it to make it similar to the new system. It was modified to allow the use of both integrators in the ACF2101 at the same time. The current BLM system uses one integrator or the other. The daughter cards external integration capacitor (1000 pf) was removed and only the internal capacitors (100 pf) of the ACF2101 were used. Other modifications were made to allow the individual control of the following signals, Reset A, Reset B, Hold A, Hold B, Track/Hold. The final change made was to the analog power supply voltages, they were lowered from the standard +15, -15, volts to +12, -12. The +5 volt logic power supply voltage remained the same.

The different test circuits used are shown in Figures 3, 4, and 5. The current source used was a Datel DVC-8500 precision voltage source and a 1.0 Meg ohm metal film leaded or surface mount resistor. Timing signals for the ACF2101 were provided by a free running pattern generator available in the ASIC Test System. A 16-Bit ADC available in the ASIC test system was used to make measurements of the integrator output. Figure 3 shows the current source at the far end of 550 ft. of RG-58 cable. Figure 4 shows the current source at the very input to the two integrators, and Figure 5 shows the cable in parallel with the current source. This last mode lets us easily switch between cable and no cable. After some effort we were able to trigger the ADC in the test system synchronously with the Track and Hold signal (part of the free running pattern). This allows us to make measurements in exactly the same way as we are proposing for the new BLM system, although not quite as fast. A timing diagram for the integrators is shown in Figure 6, we are able to free run both the A and B channels, and selectively digitize either A only, B only, or A and B both.

What we found was that the A and B channels have a slightly different input offset voltage and input resistance value which causes the two channels to be different. With no cable capacitance this difference is about .04% on a 10μA signal (see Figure 7). However, when a long cable with a large capacitance is attached, the different offset voltages at the input either charge or discharge the cable as the system "ping-pongs" (for the effect of different cable lengths see Figure 8). The result is that the A channel reads high by approximately 200 nA and the B channel reads low by the same amount (Figures 9 and 10). Figure 11 shows the data for reading both A and B sides, note the two separate peaks. We believe this to be solely due to the capacitance of the cable and the different offset voltages of the two inputs. If we vary the input voltage, (see Figure 12) we also see a slight effect due to the different input resistor values. The reader should note that the noise in the system has an RMS of 15 counts which is equivalent to and RMS of 3 nA on a 10 μA signal.

In an effort to reduce or eliminate the differences between the two integrator channels two more circuit modification were made. At the suggestion of Craig Drennan an input offset voltage nulling circuit was added to the ACF2101. The "Nulling" Circuit, which is bi-polar only needed to be added to one of the two integrators. This allowed us to adjust the offset of the two integrators to be equal at zero input current. This reduced the maximum A-B difference from 2000 counts to 859 counts (Figure 13). The remaining effect is the difference of the "ON" resistance of the two input switches. These switches are about 1.5 kOhm in the ON state. By temporarily adding a fixed resistor to A and measuring the shift in A-B, we were able to calculate the difference of the two switches. The B switch had 43 Ohms less resistance, by adding a 43 Ohm resistor to the B side we were able to match the two integrators over a very large range. After adding the nulling circuit and the 43 Ohm resistor (see Fig. 14), we now have matched A-B to –10 to 35 counts (Figure 15) over the entire range of 0 to 10 μA. We now believe that we can "Tune" the integrators quite nicely and thus eliminate the need for a cable receiver.

We now have a very nice system for making these measurements and will continue to study the front end.

ACF2101 Test Setup Schematic

(Long Cable Configuration)

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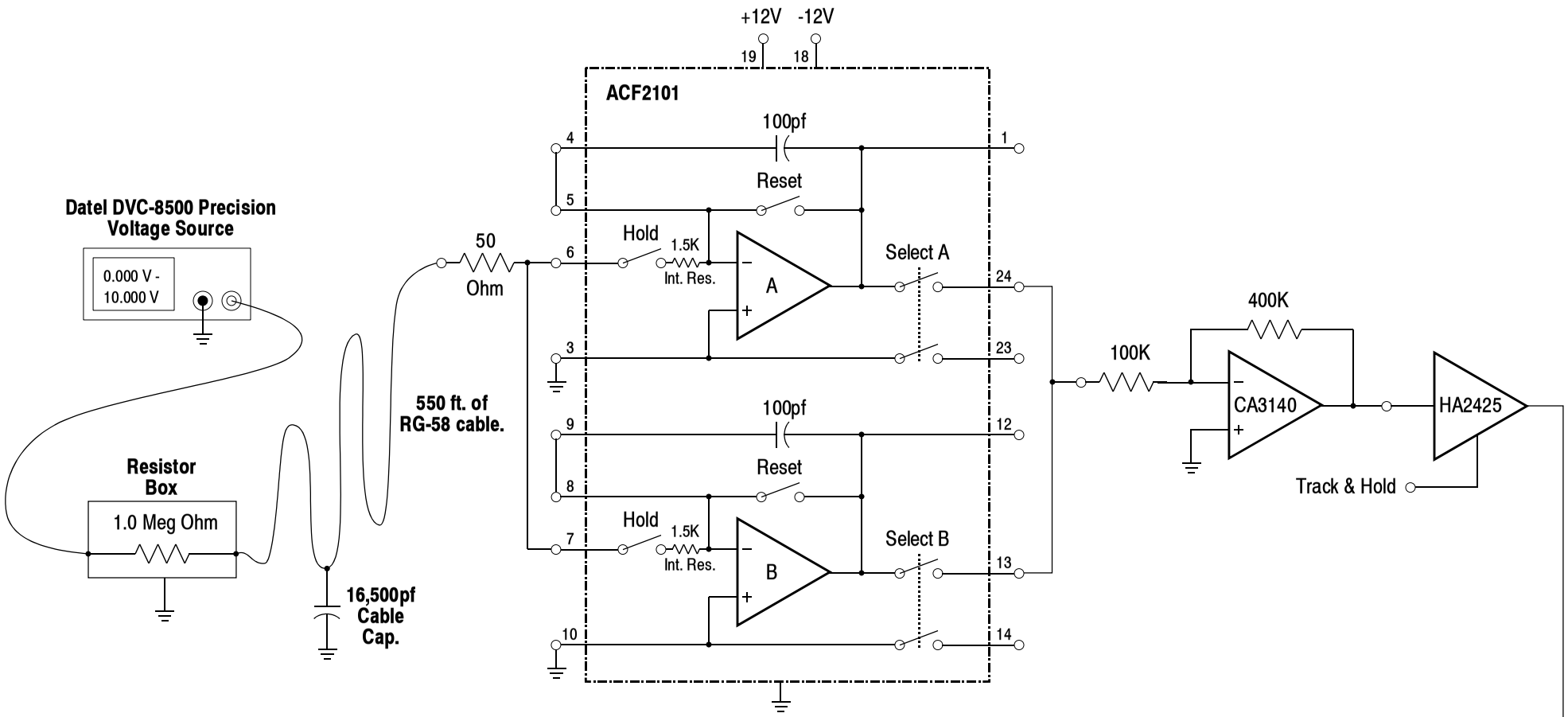


Figure 3.

ACF2101 Test Setup Schematic

03/23/2004

(Surface Mount Resistor (No Cable) Configuration)

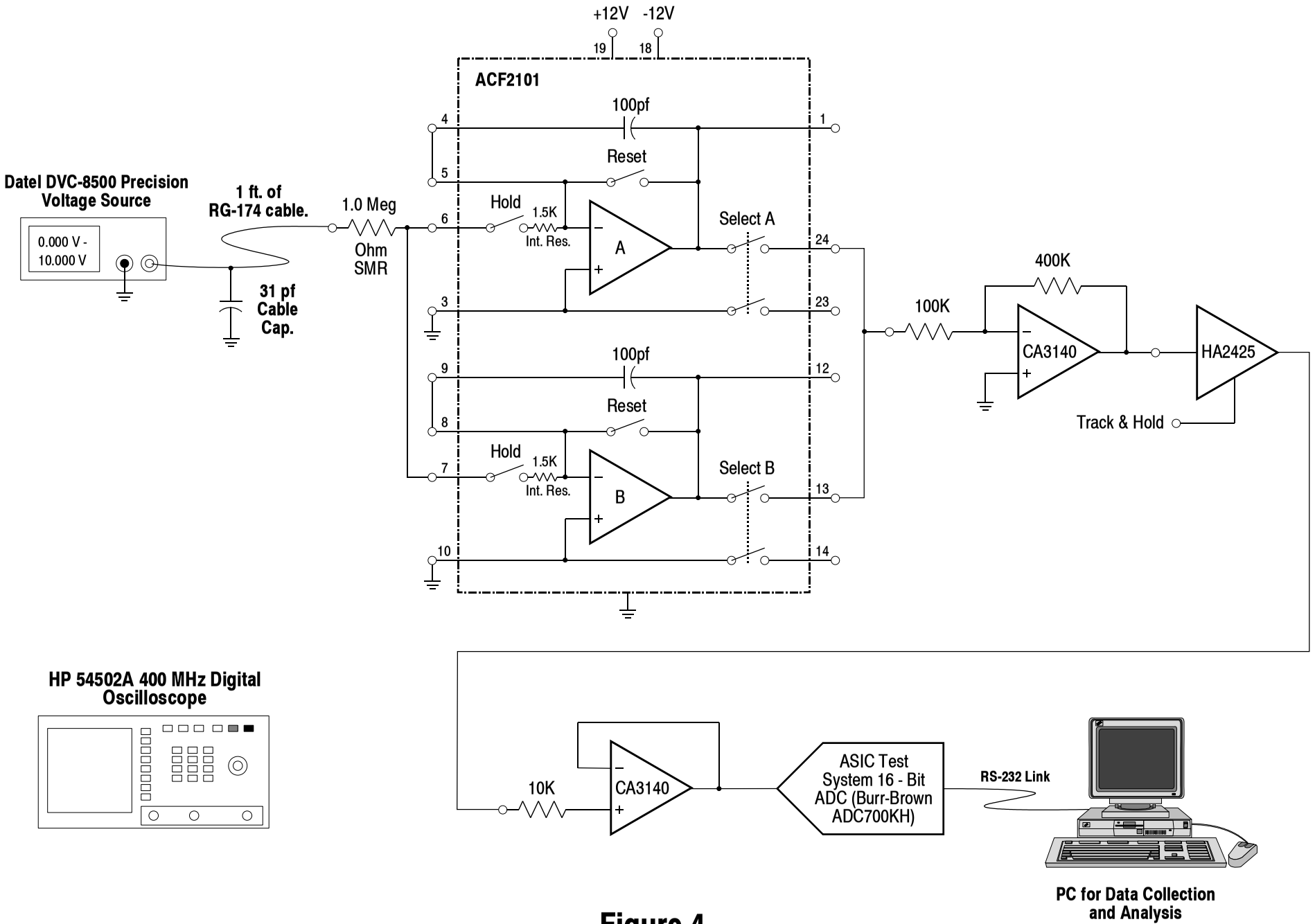


Figure 4.

ACF2101 Test Setup Schematic

03/23/2004

(Surface Mount Resistor (Optional Cable) Configuration)

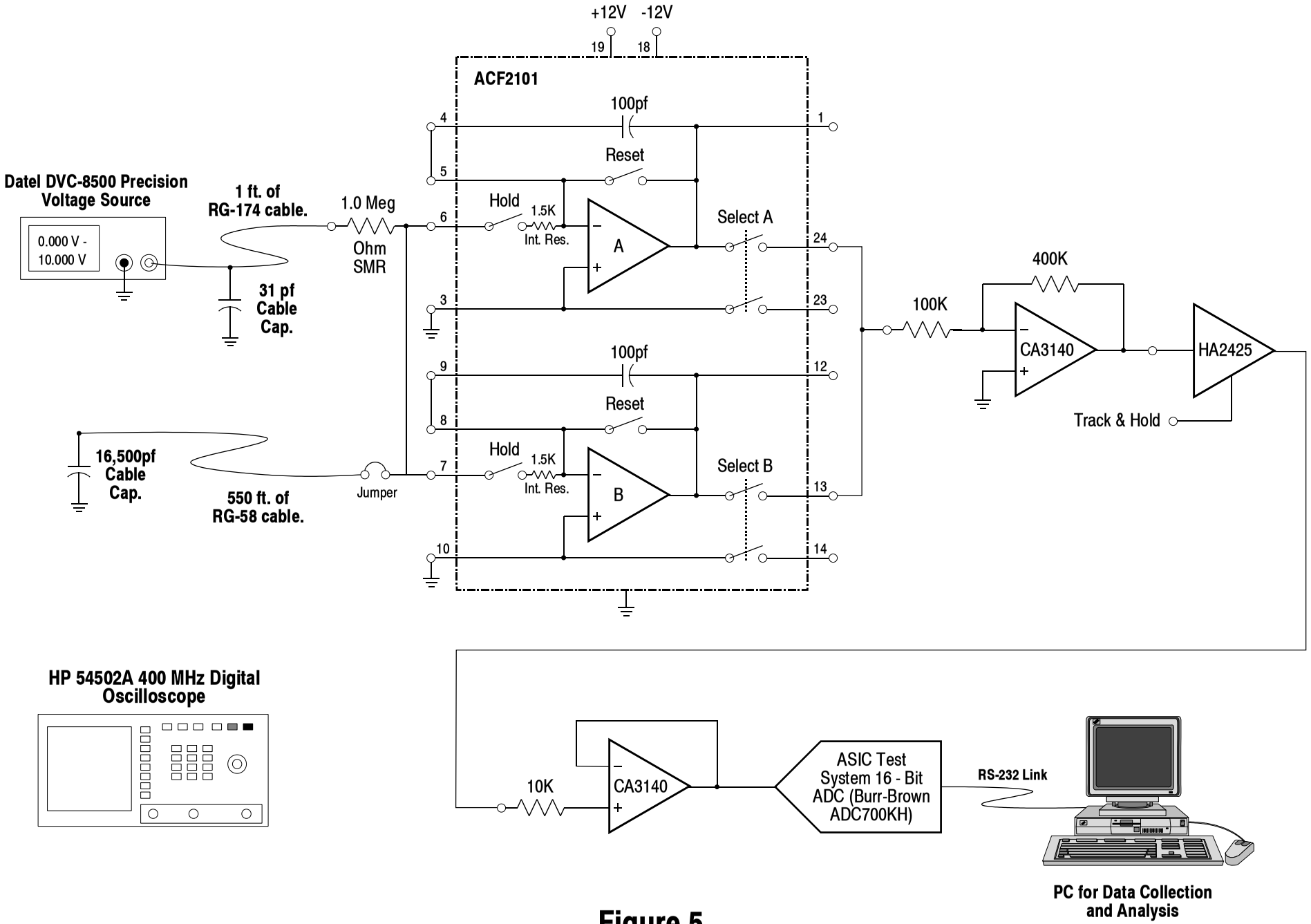
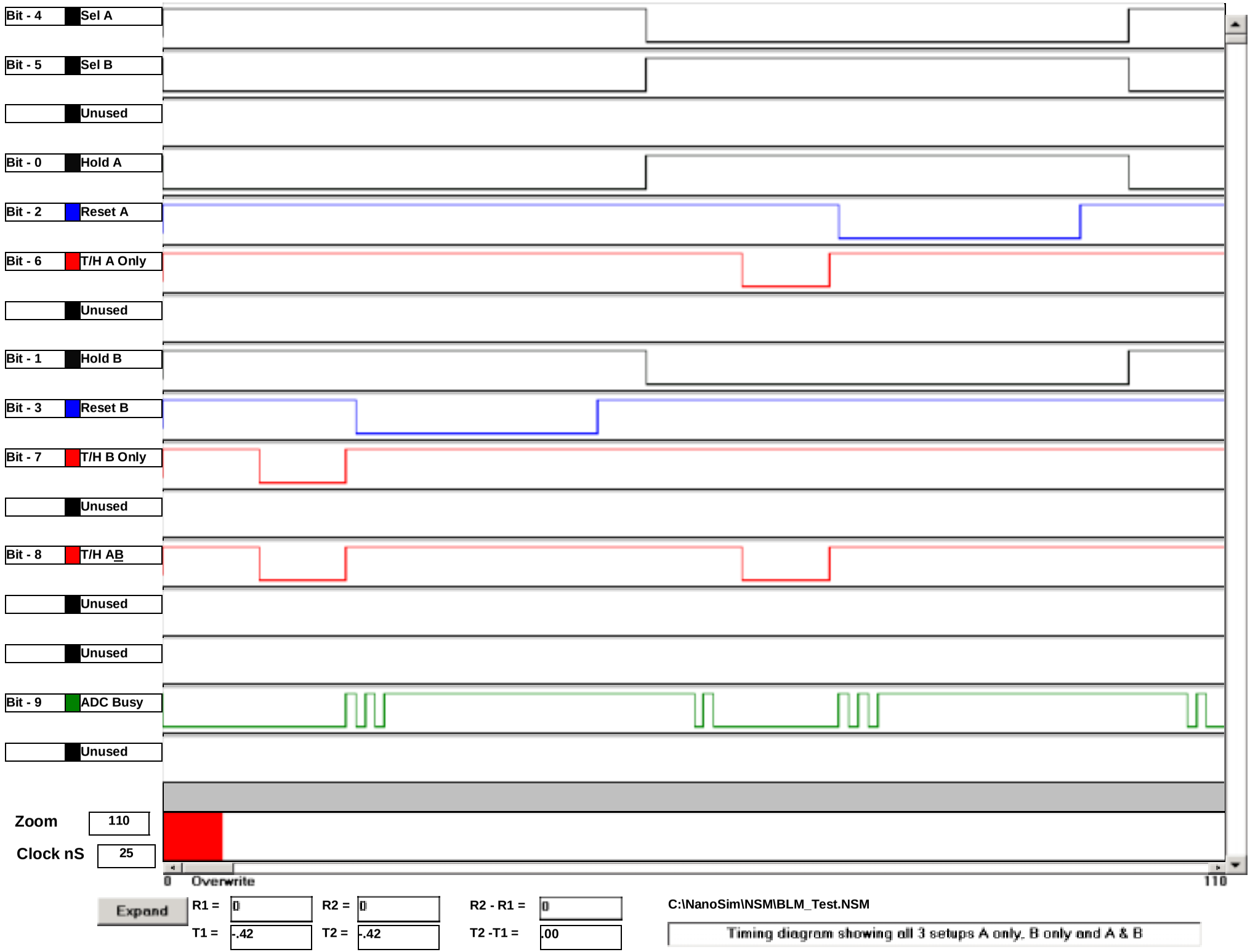


Figure 5.



Expand

R1 = 0

R2 = 0

R2 - R1 = 0

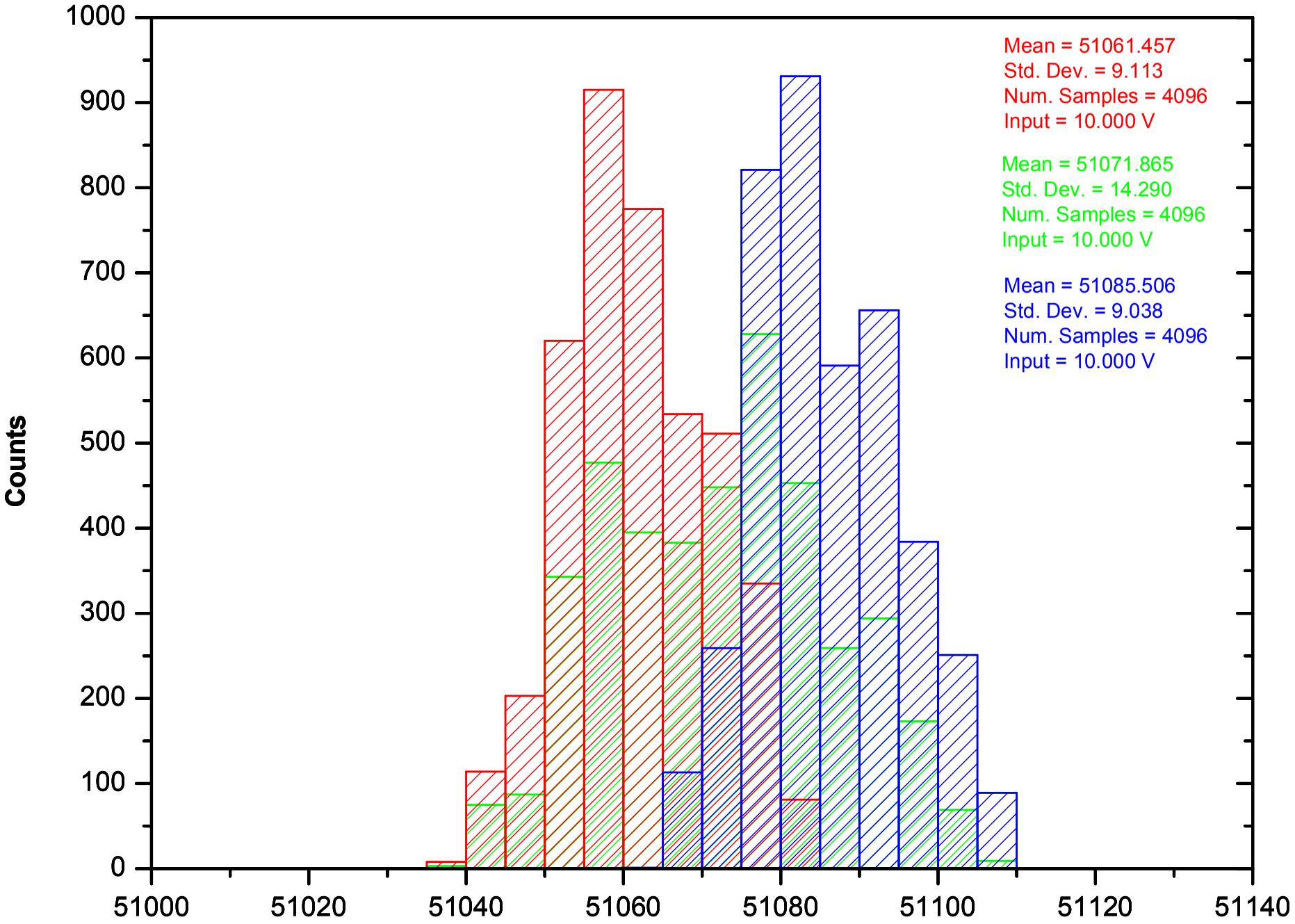
T1 = -.42

T2 = -.42

T2 -T1 = .00

C:\NanoSim\NSM\BLM_Test.NSM

Timing diagram showing all 3 setups A only, B only and A & B



Ch. A, B, A&B, No Cable/1 Meg SMR, Input 10.000V, Sync ADC, (Files: BLM_XX_SMR_10000.DAT)

Figure 7.

Channel A and B plotted with different lengths of coaxial cable (RG-58) attached.

Red, Cable Length = 550 ft., Blue, Cable Length = 1 ft., Green, Cable Length = 0 ft.

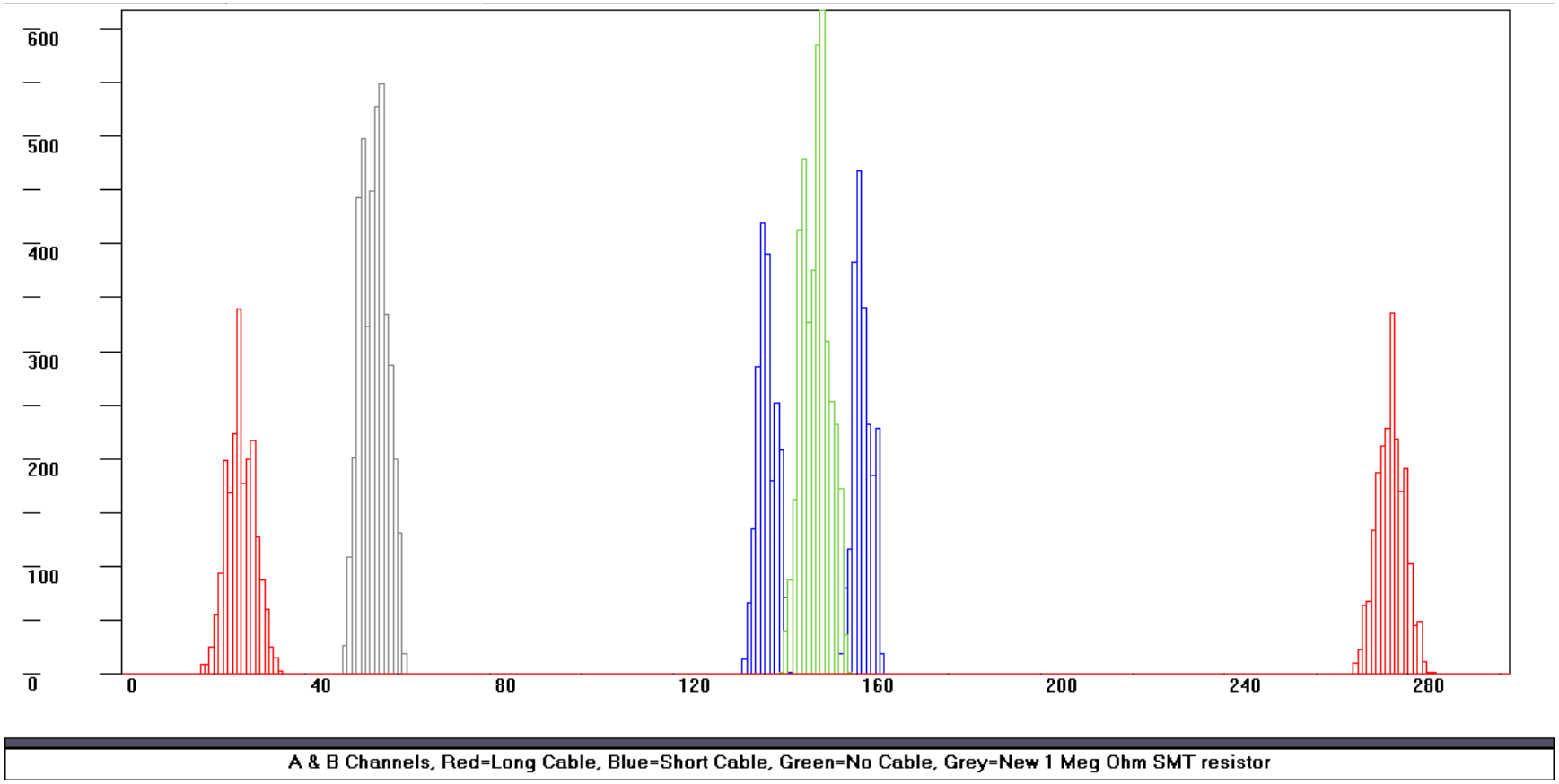
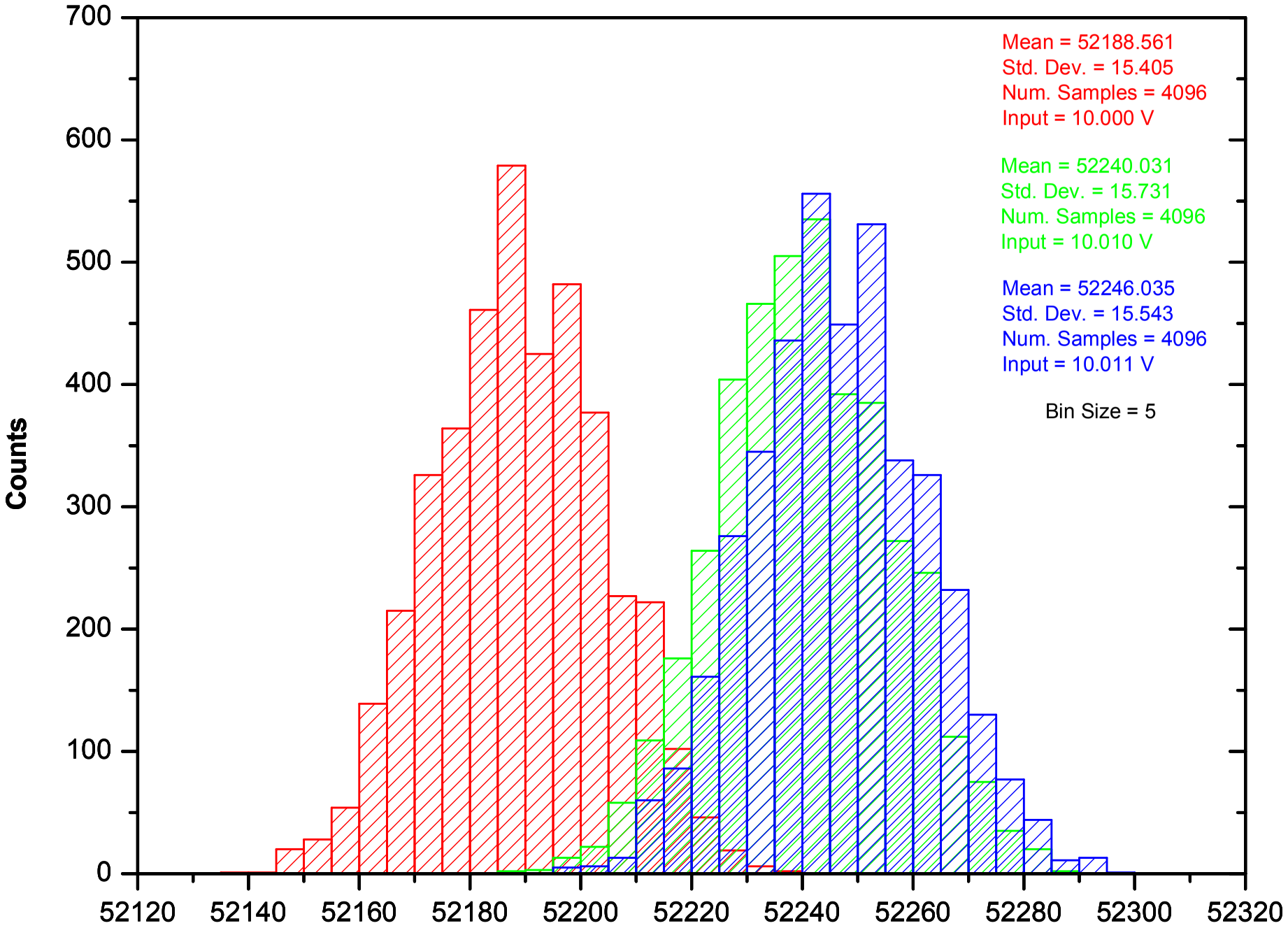
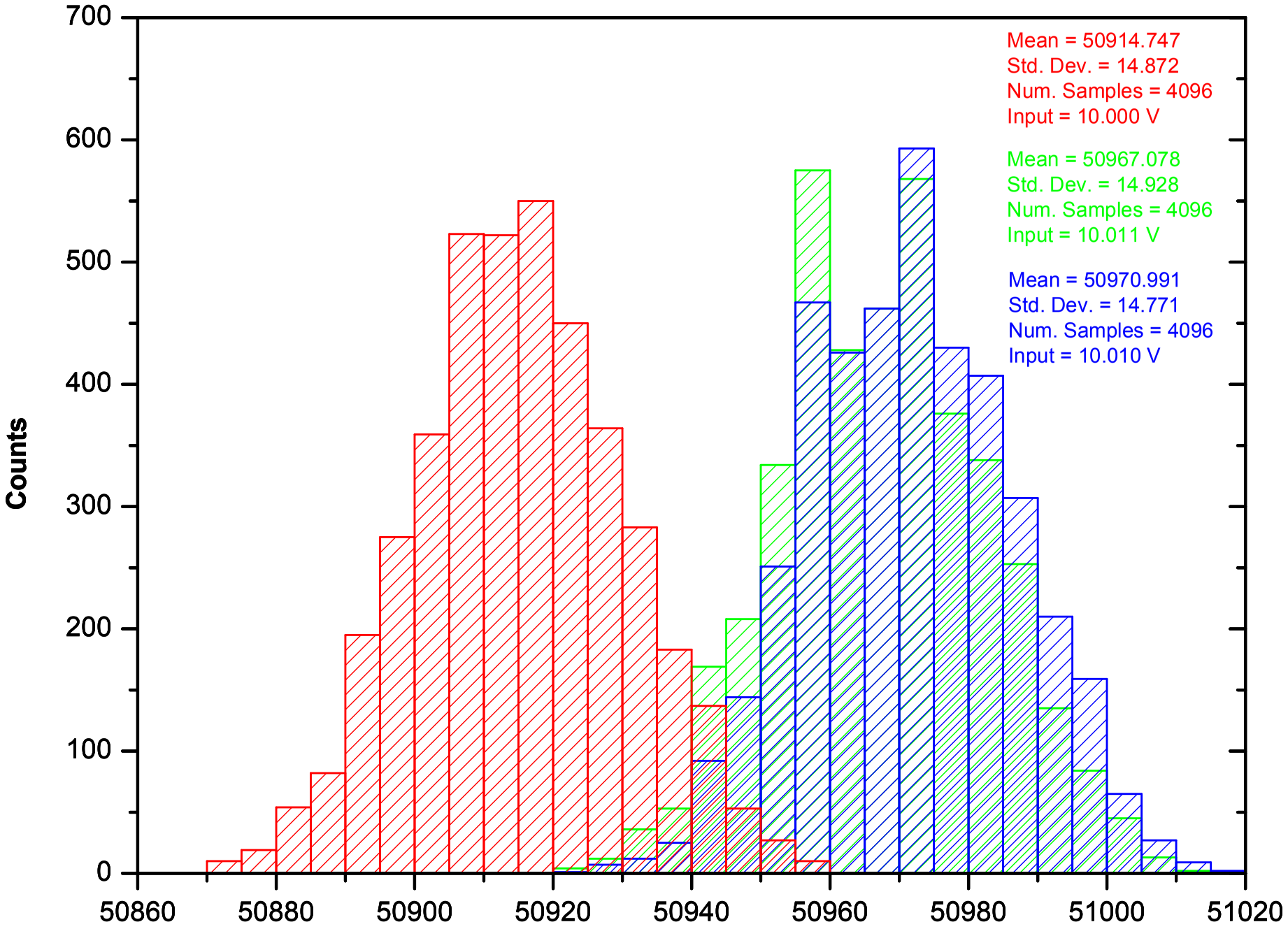


Figure 8.



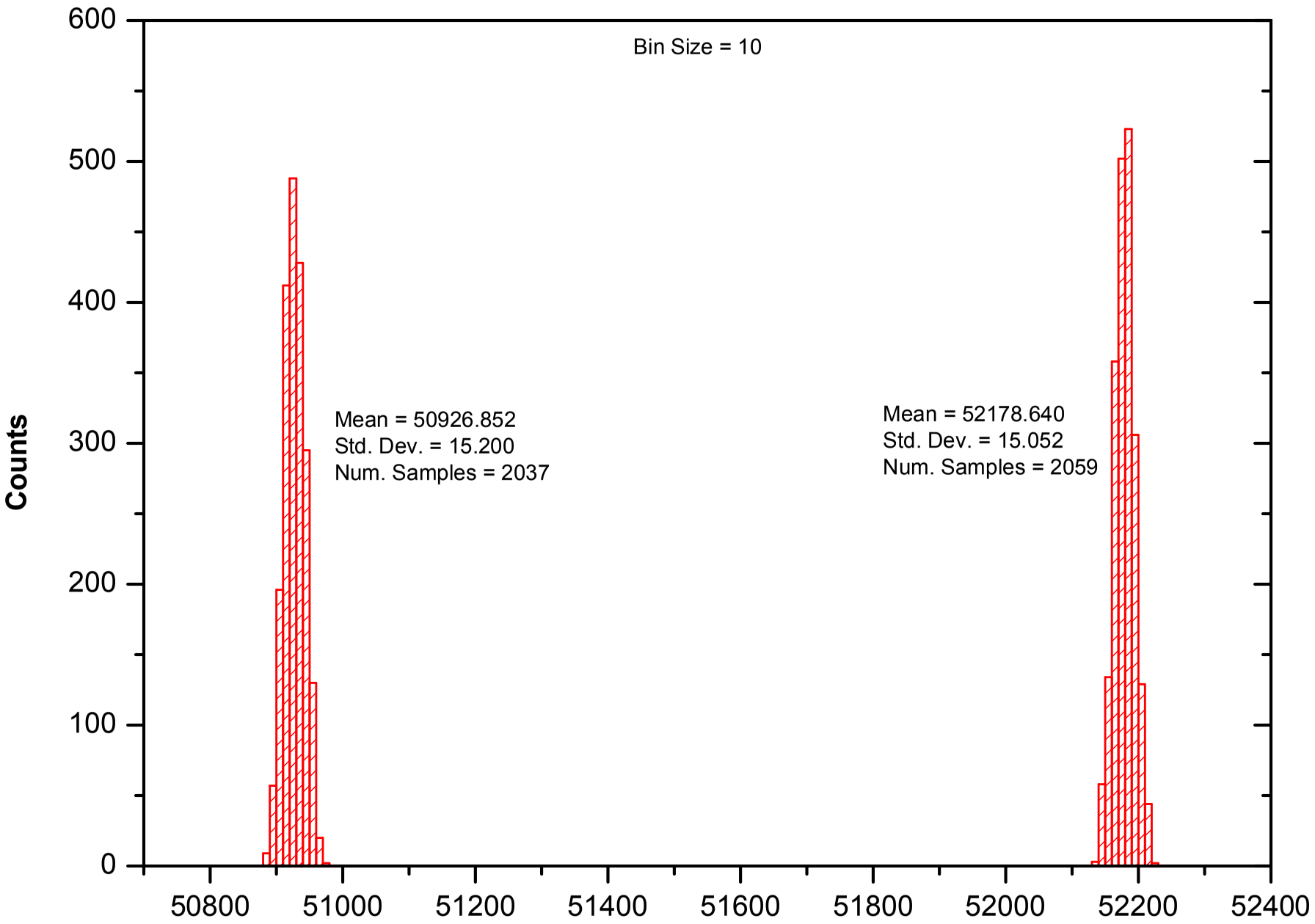
Ch. A, 550 ft. Cable, Input 10 + .000V, .010V, .011V, Sync ADC, (Files: BLM_A_L_100XX.DAT)

Figure 9.



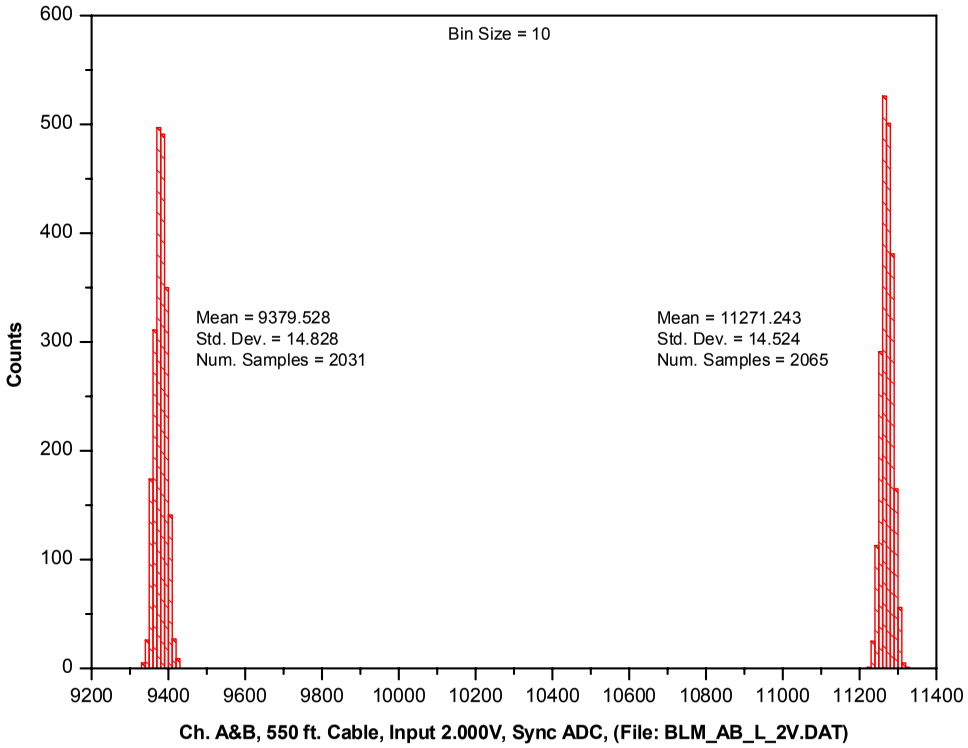
Ch. B, 550 ft. Cable, Input 10 - .000V, .010V, .011V, Sync ADC, (File: BLM_B_L_100XX.DAT)

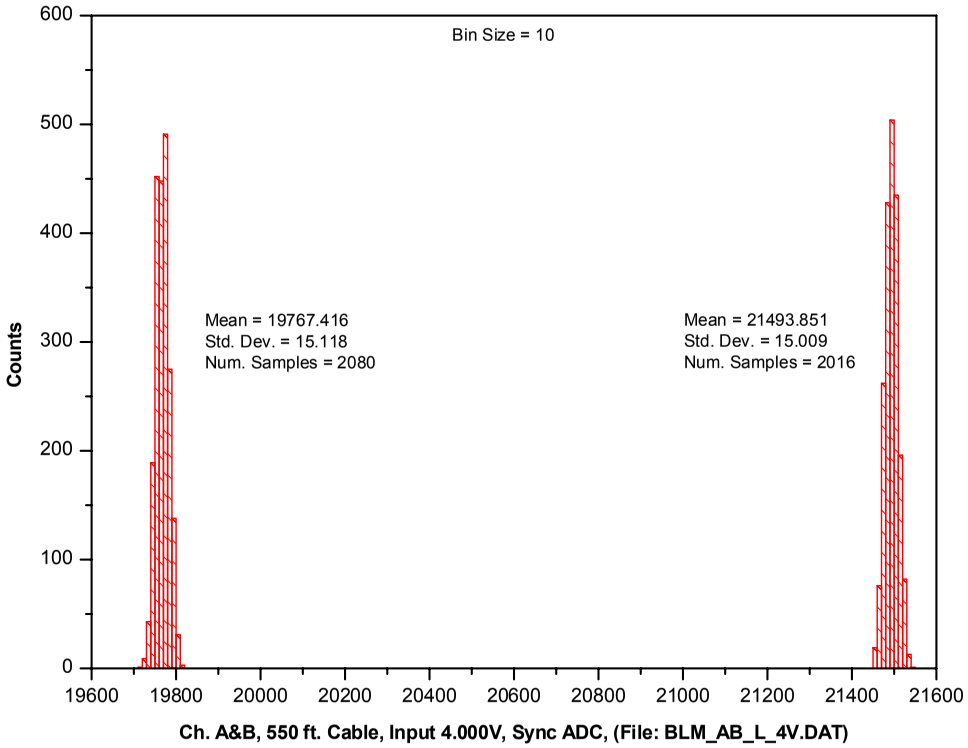
Figure 10.

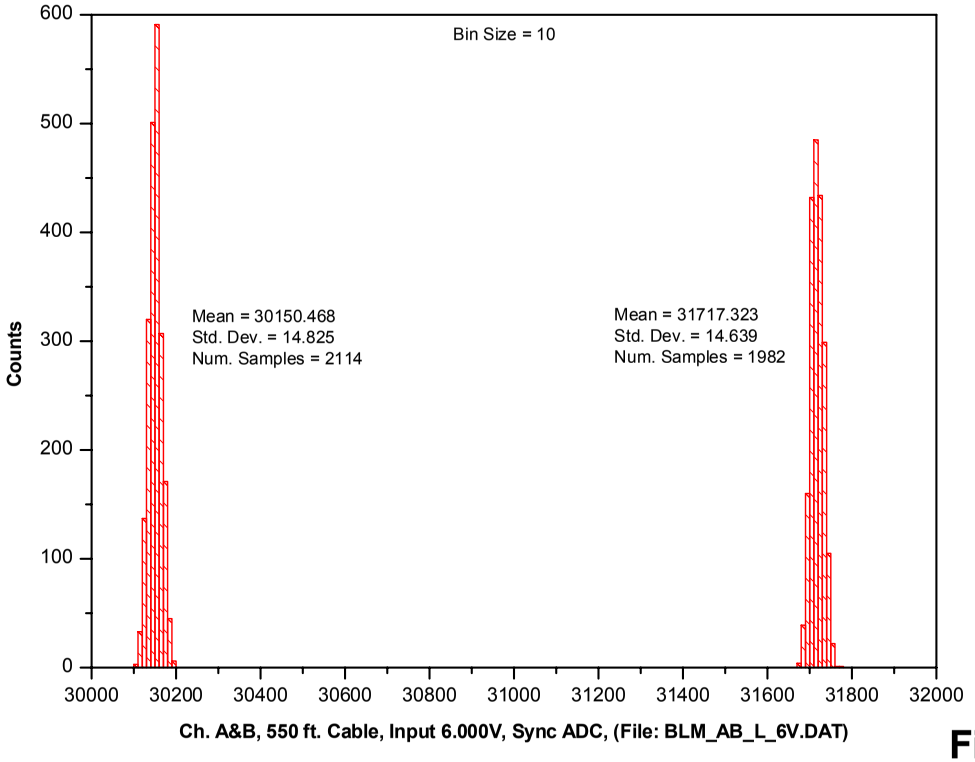


Ch. A&B, 550 ft. Cable, Input 10.000V, Sync ADC, (File: BLM_AB_L_10000.DAT)

Figure 11.


Bin Size = 10
Counts
Mean = 9379.528
Std. Dev. = 14.828
Num. Samples = 2031
Mean = 11271.243
Std. Dev. = 14.524
Num. Samples = 2065
Ch. A&B, 550 ft. Cable, Input 2.000V, Sync ADC, (File: BLM_AB_L_2V.DAT)


Bin Size = 10
Counts
Mean = 19767.416
Std. Dev. = 15.118
Num. Samples = 2080
Mean = 21493.851
Std. Dev. = 15.009
Num. Samples = 2016
Ch. A&B, 550 ft. Cable, Input 4.000V, Sync ADC, (File: BLM_AB_L_4V.DAT)


Bin Size = 10
Counts
Mean = 30150.468
Std. Dev. = 14.825
Num. Samples = 2114
Mean = 31717.323
Std. Dev. = 14.639
Num. Samples = 1982
Ch. A&B, 550 ft. Cable, Input 6.000V, Sync ADC, (File: BLM_AB_L_6V.DAT)

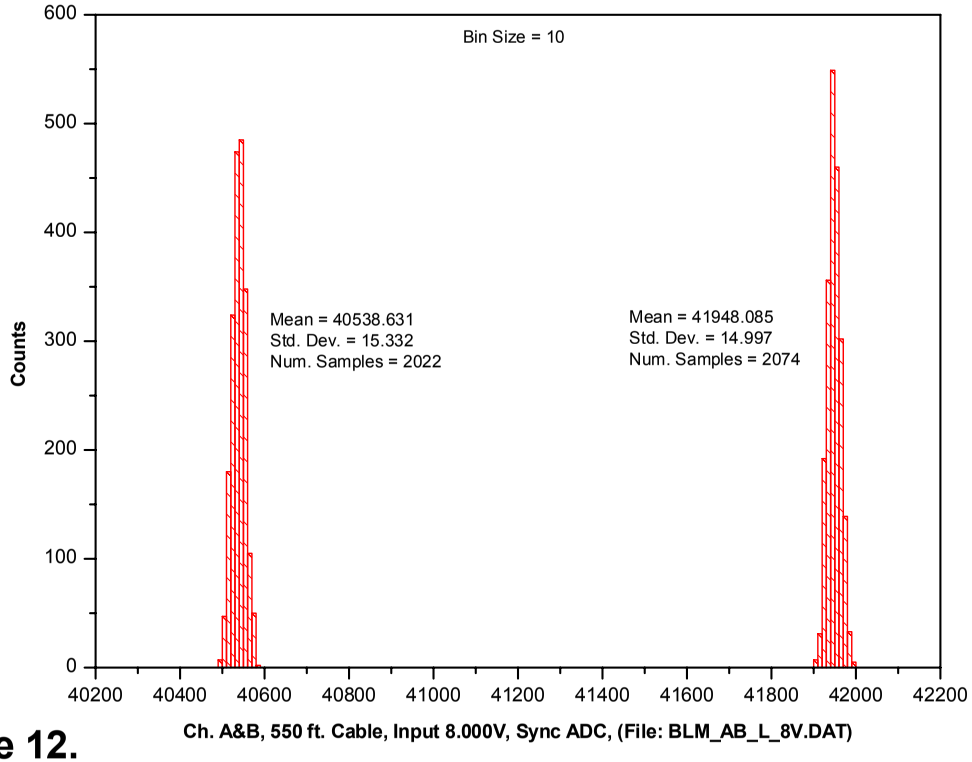
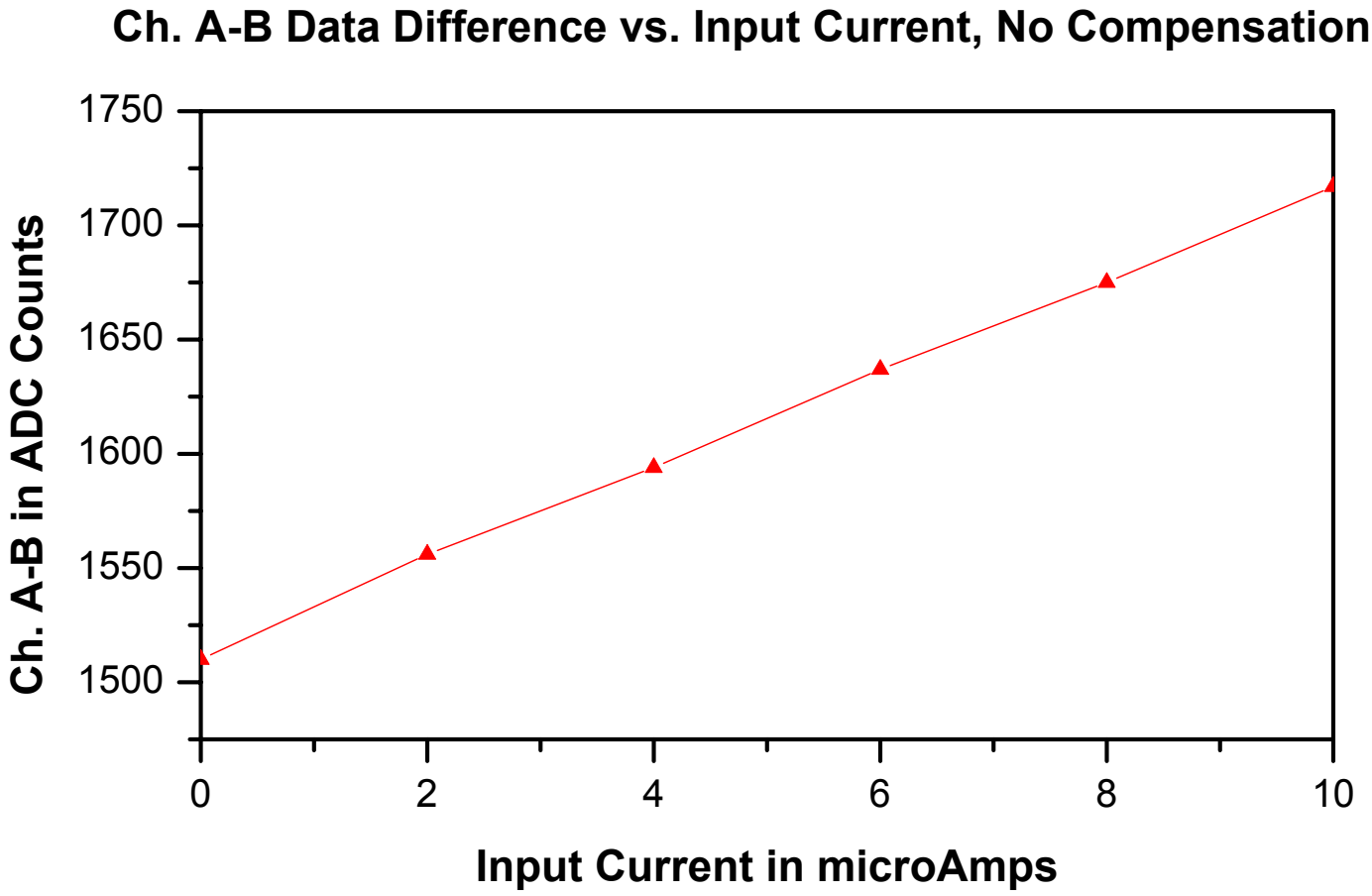

Bin Size = 10
Counts
Mean = 40538.631
Std. Dev. = 15.332
Num. Samples = 2022
Mean = 41948.085
Std. Dev. = 14.997
Num. Samples = 2074
Ch. A&B, 550 ft. Cable, Input 8.000V, Sync ADC, (File: BLM_AB_L_8V.DAT)

Figure 12.


Ch. A-B Data Difference vs. Input Current, No Compensation
Ch. A-B in ADC Counts
1750
1700
1650
1600
1550
1500
0
2
4
6
8
10
Input Current in microAmps

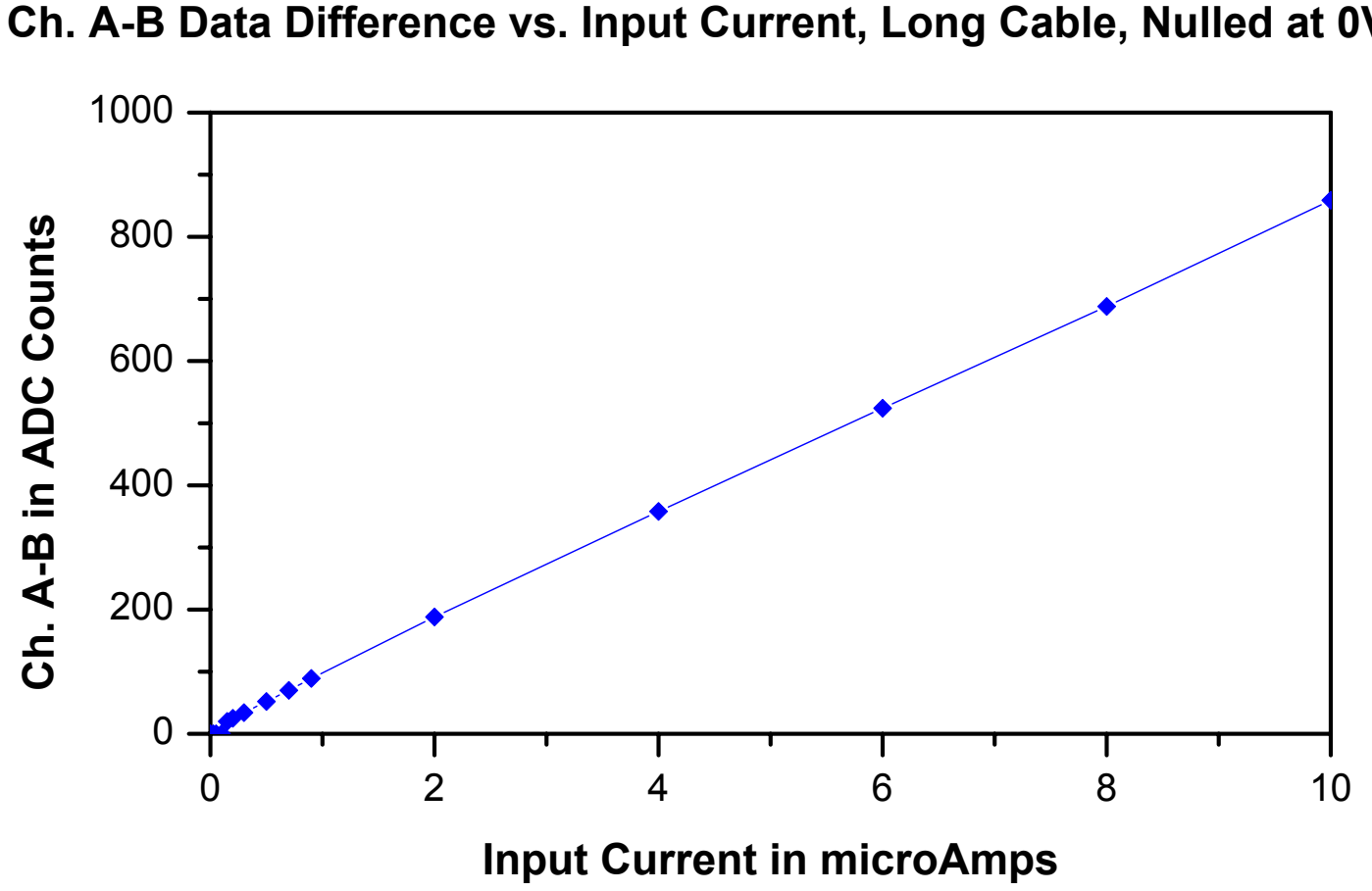

Ch. A-B Data Difference vs. Input Current, Long Cable, Nulled at 0V
Ch. A-B in ADC Counts
1000
800
600
400
200
0
0
2
4
6
8
10
Input Current in microAmps

Figure 13.

ACF2101 Test Setup Schematic

03/23/2004

(Offset Null and Offset Adj. Configuration)

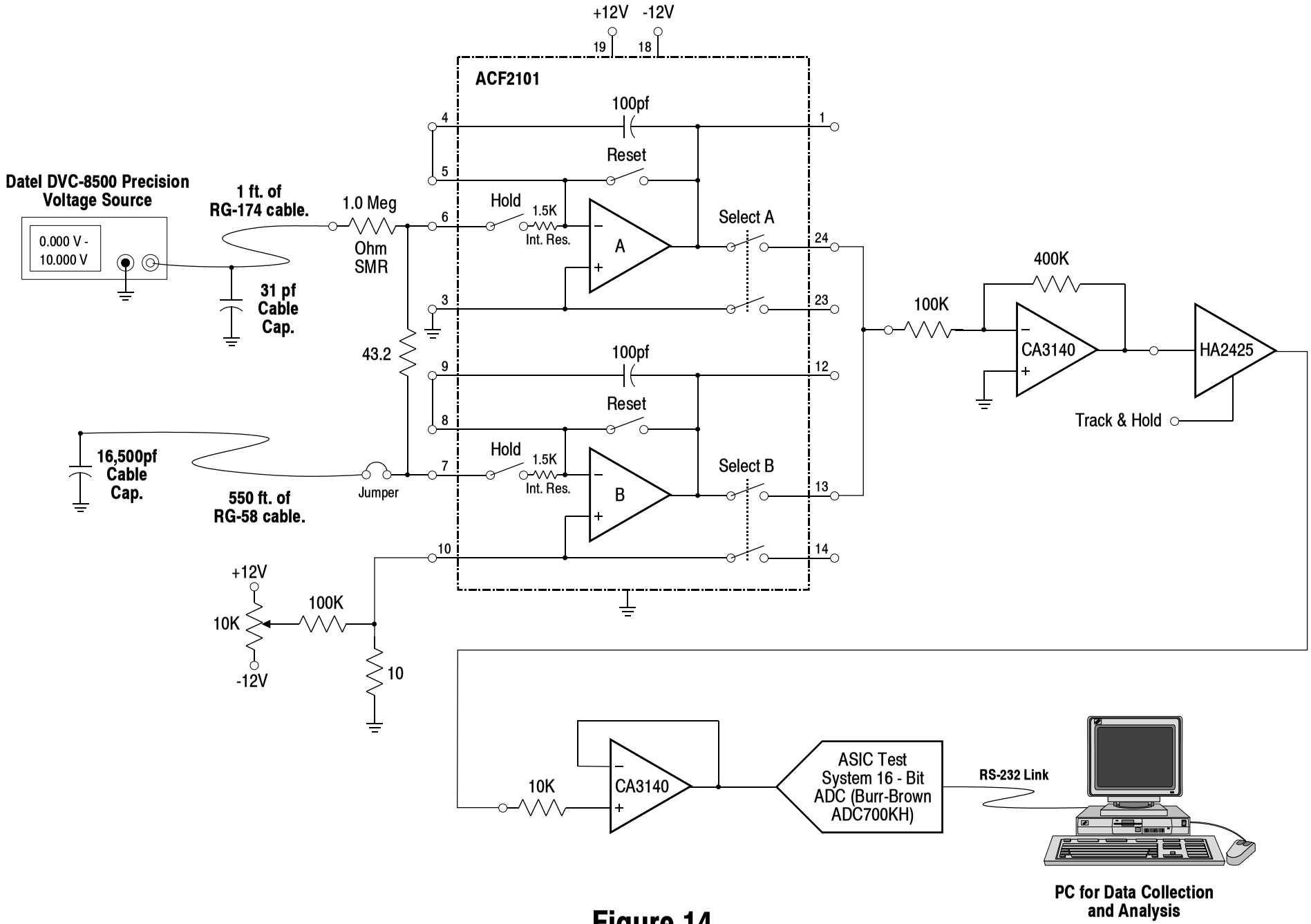


Figure 14.

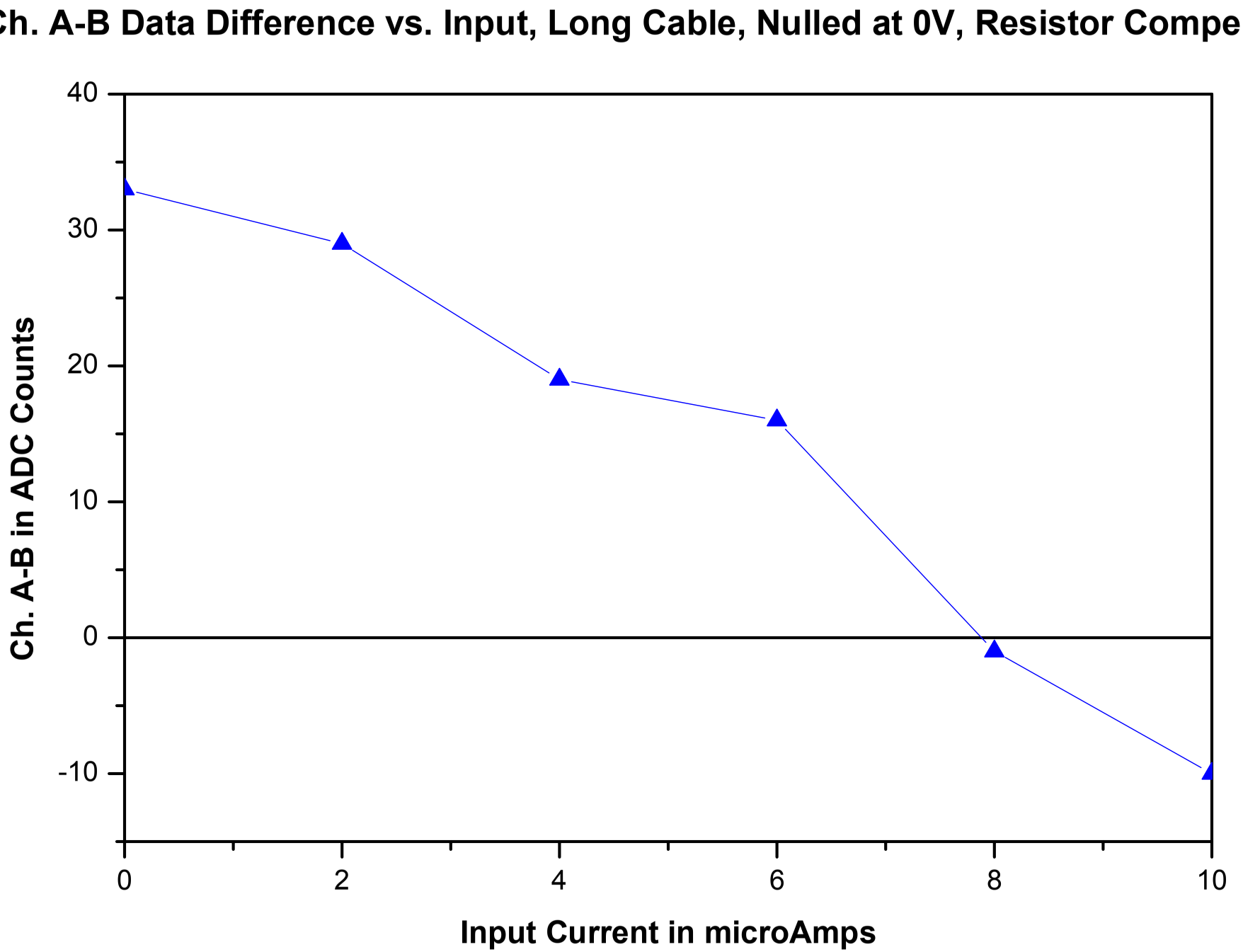

Ch. A-B Data Difference vs. Input, Long Cable, Nulled at 0V, Resistor Compensated
Ch. A-B in ADC Counts
40
30
20
10
0
-10
0
2
4
6
8
10
Input Current in microAmps

Figure 15.

Datasheets:

Texas Instruments/Burr-Brown, - ACF2101, Low Noise, Dual Switched Integrator. PDS-1078D (SBFS003) http://www.burr-brown.com/

Texas Instruments/Burr-Brown, - Improved Noise Performance of the ACF2101 Switched Integrator., Application Bulletin AB-053 (SBOA032) http://www.burr-brown.com/

Intersil, - HA-2420, HA-2425, Sample and Hold Amplifier., (FN2856.4) http://www.intersil.com/

Harris Semiconductor, - CA3140, CA3140A, 4.5 MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output., (File Number 957.3) http://www.harris.com/

Acknowledgements:

We would like to thank the following people for their assistance during the testing of the ACF2101: Craig Drennan for circuit suggestions, ideas, and advice. Marvin Olson for the loan of a BLM daughter card, ACF2101 devices, and 550 ft. of coaxial cable. And Charlie Nelson for circuit suggestions, ideas, and advice.