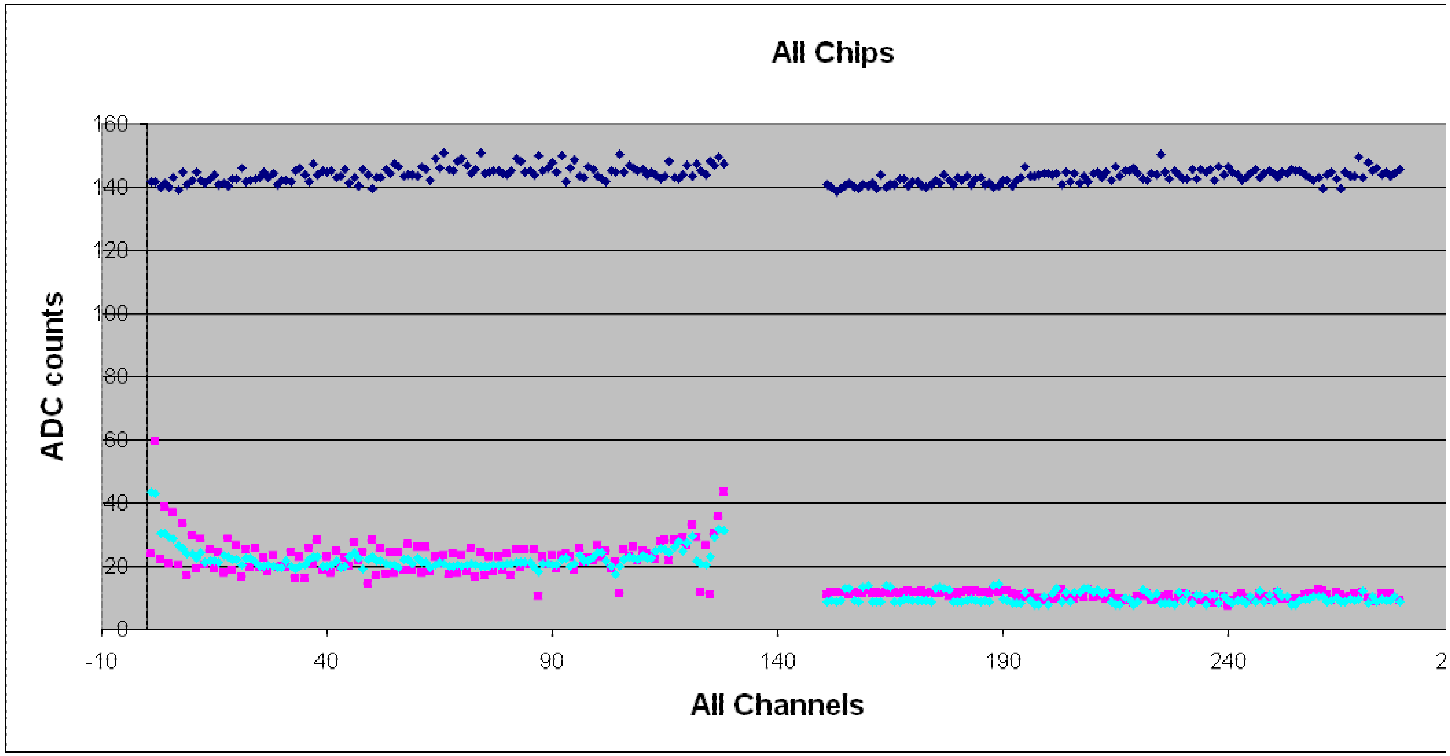
Module Tests

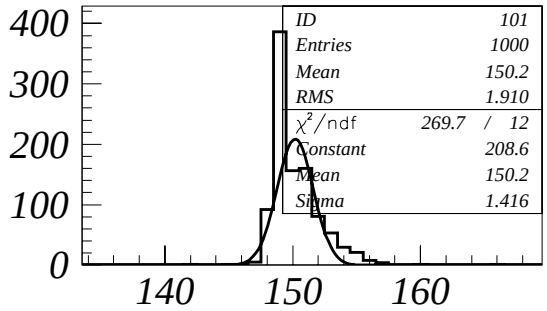
- Noise measurement using L0 prototype connected with only cable. ➔ capacitance of analog cable.
- L0/L1 prototype modules being tested. The basic functionality working OK, however… there are a few unresolved problems and misbehaviors.

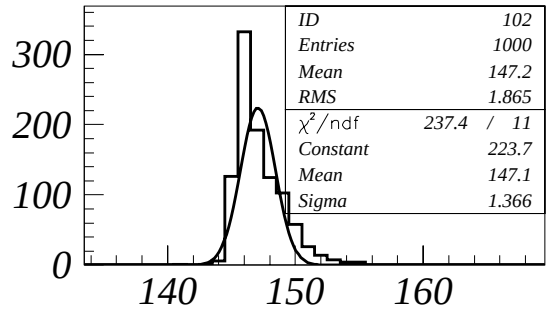
  - ➢ Noise due to (?????) preamp reset.
  - ➢ BW dependence not completely same as expected.
  - ➢ Big (and the same size of) noise in first a few events.
  - ➢ Too clean (no noise) in the rest of events for loaded channel.
  - ➢ Many zero ADC counts. ➔ firmware or operation dependence.

Noise Measurement by the Prototype with only cable connected

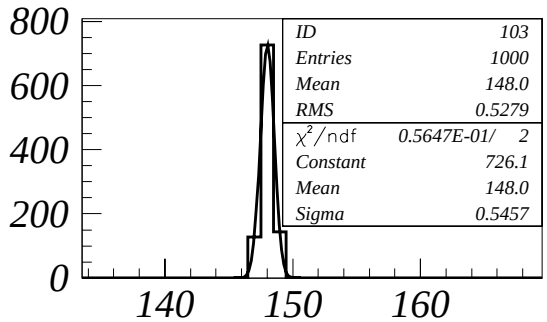


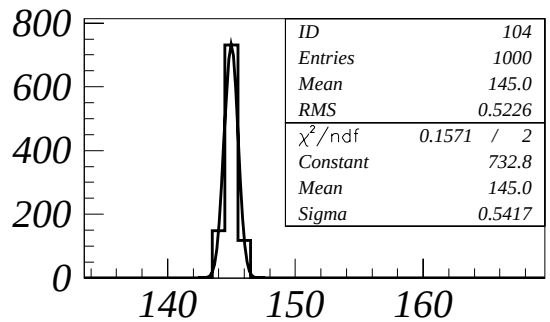
Noise Level (only cable bonded)



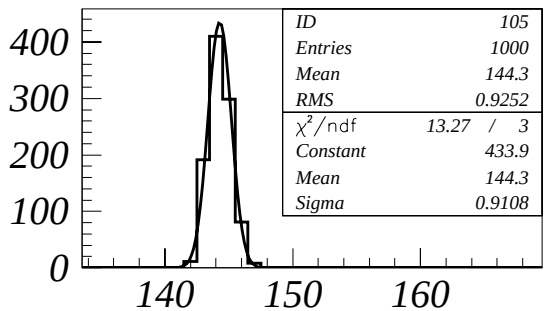


cable bonded





preamp kept resetting

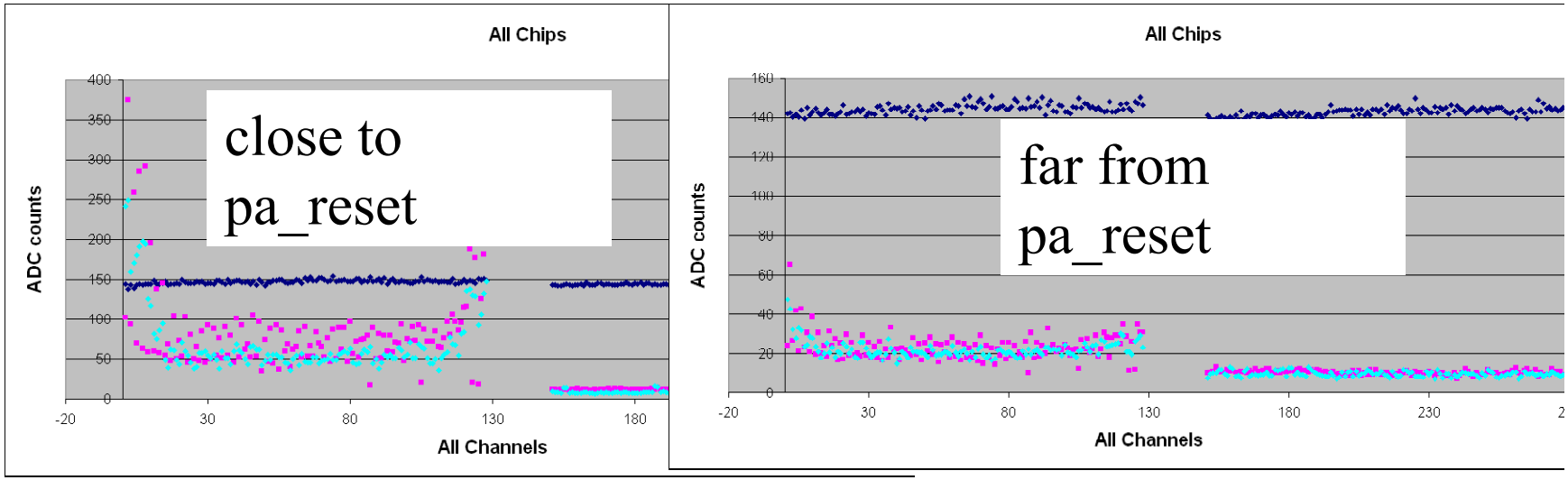


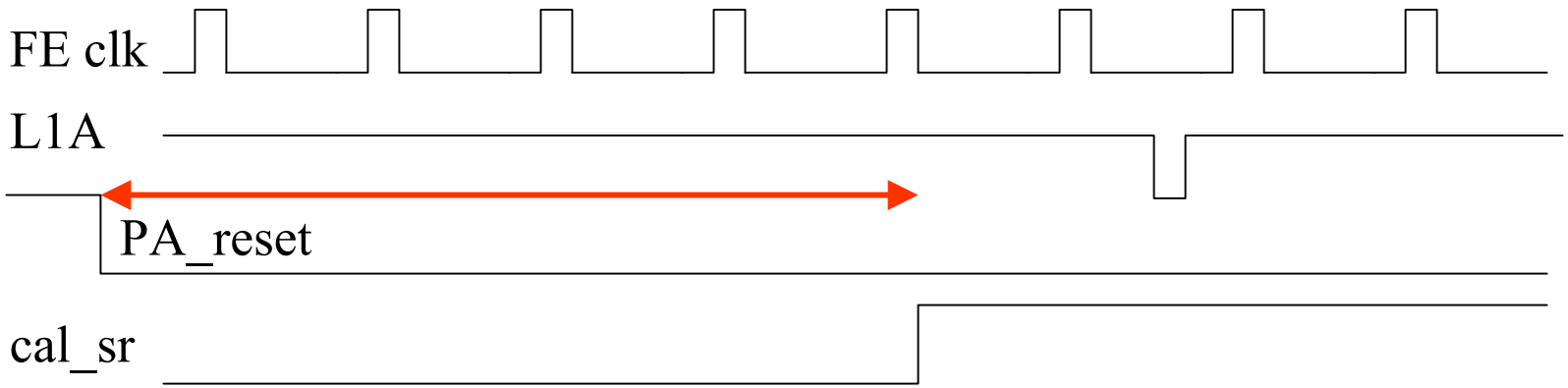
no cable bonded

Capacitance of Analog Cable

- Use RMS of pedestal distributions (not gaussian σ).
- RMS(bonded channel) = 1.88 ADC = 1320e.
- RMS(no load) = 0.93 ADC = 650e.
- Difference = 670e.
- ENC of SVX4 = [300 + 41C(pF)]e.
- Based on the slope above, 41C = 670e.
  ➔ C = 16.3pF.
- Measurement for single cable by LCR meter:
  15pF @1MHz, 16pF@100kHz.

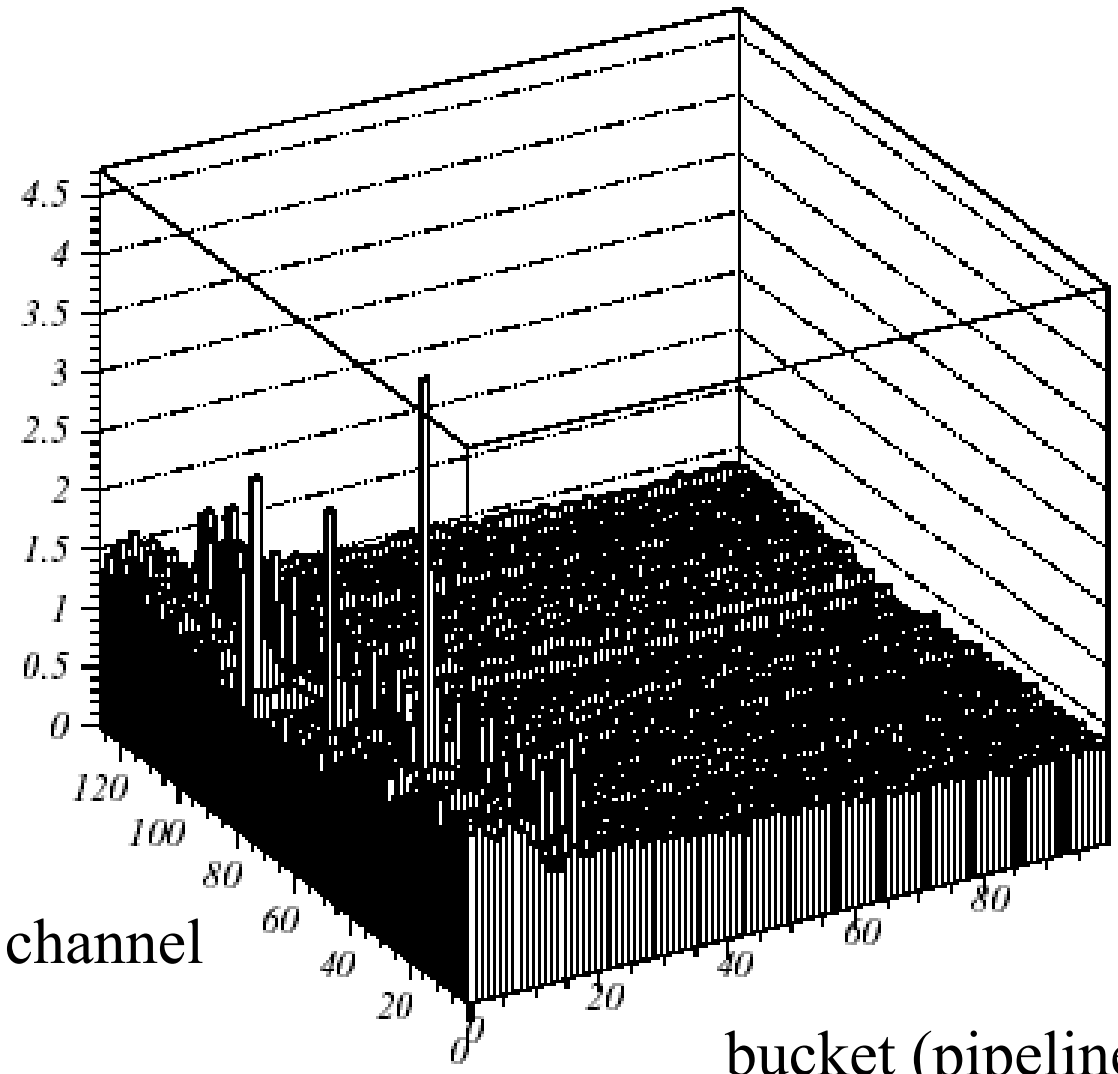
Noise & SVX4 operation





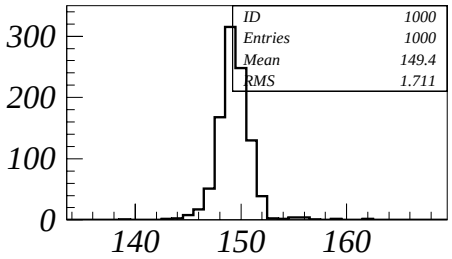
- PRD2(=refresh of reference cell) wrong in position???
- Known effect: closer the L1A, more noise. (I don't recommend pipeline depth = 1 or even 2.)

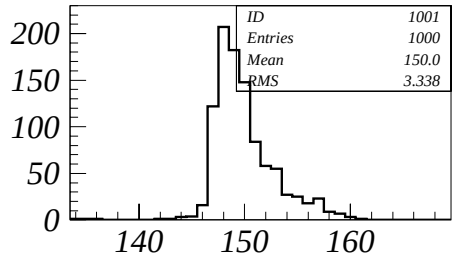
Old Measurement of Noise



Misbehaviors 1 (w/ cable only)

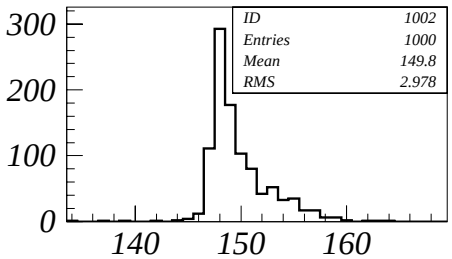
BW=0

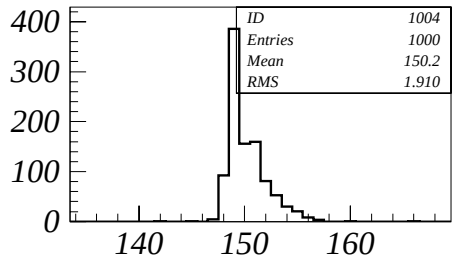




BW=1

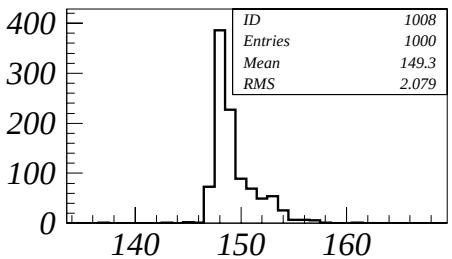
BW=2

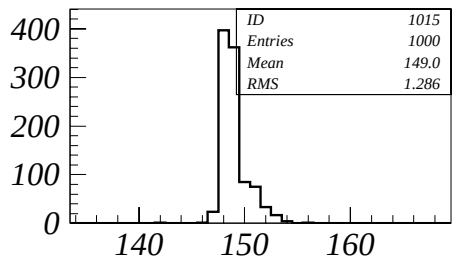




BW=4

BW=8

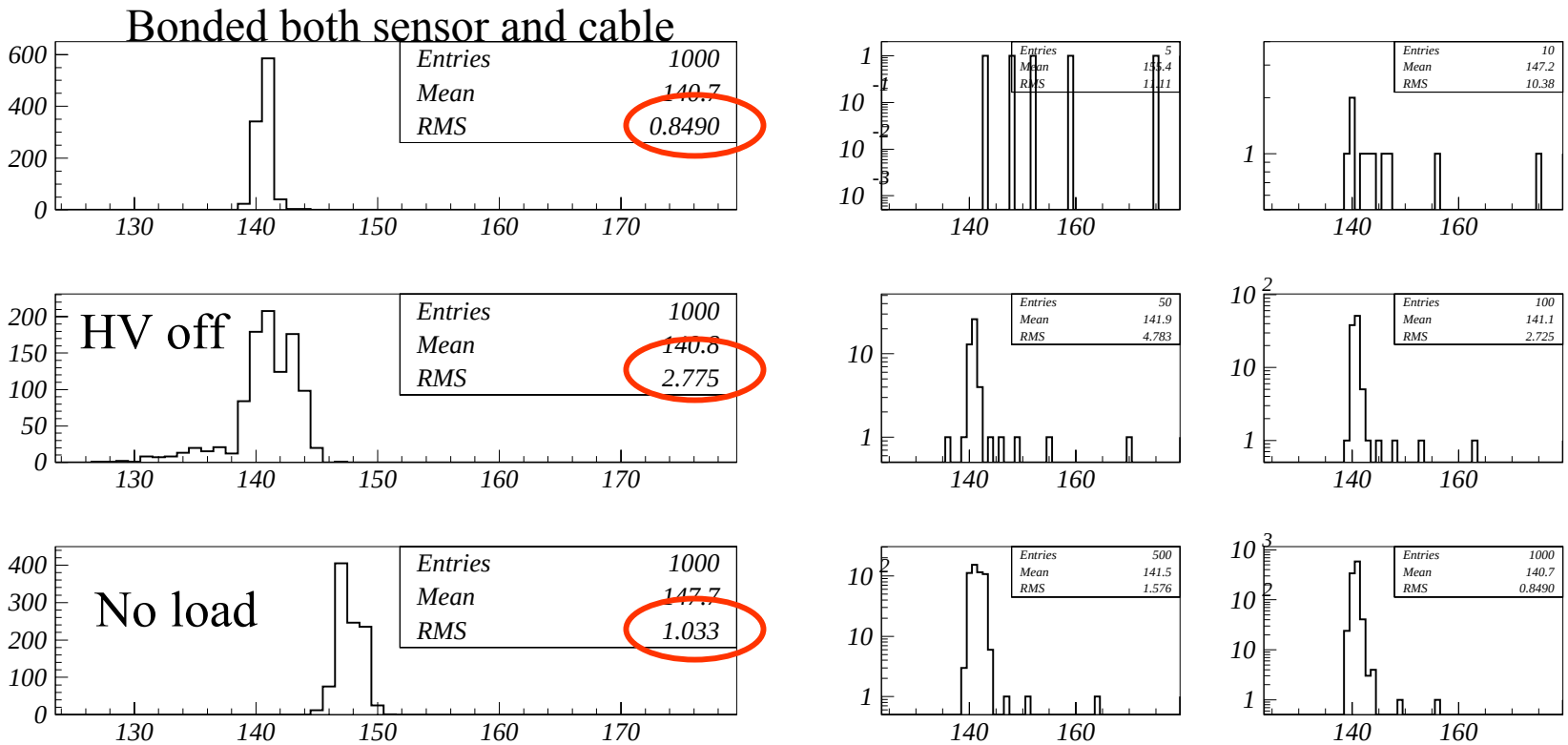




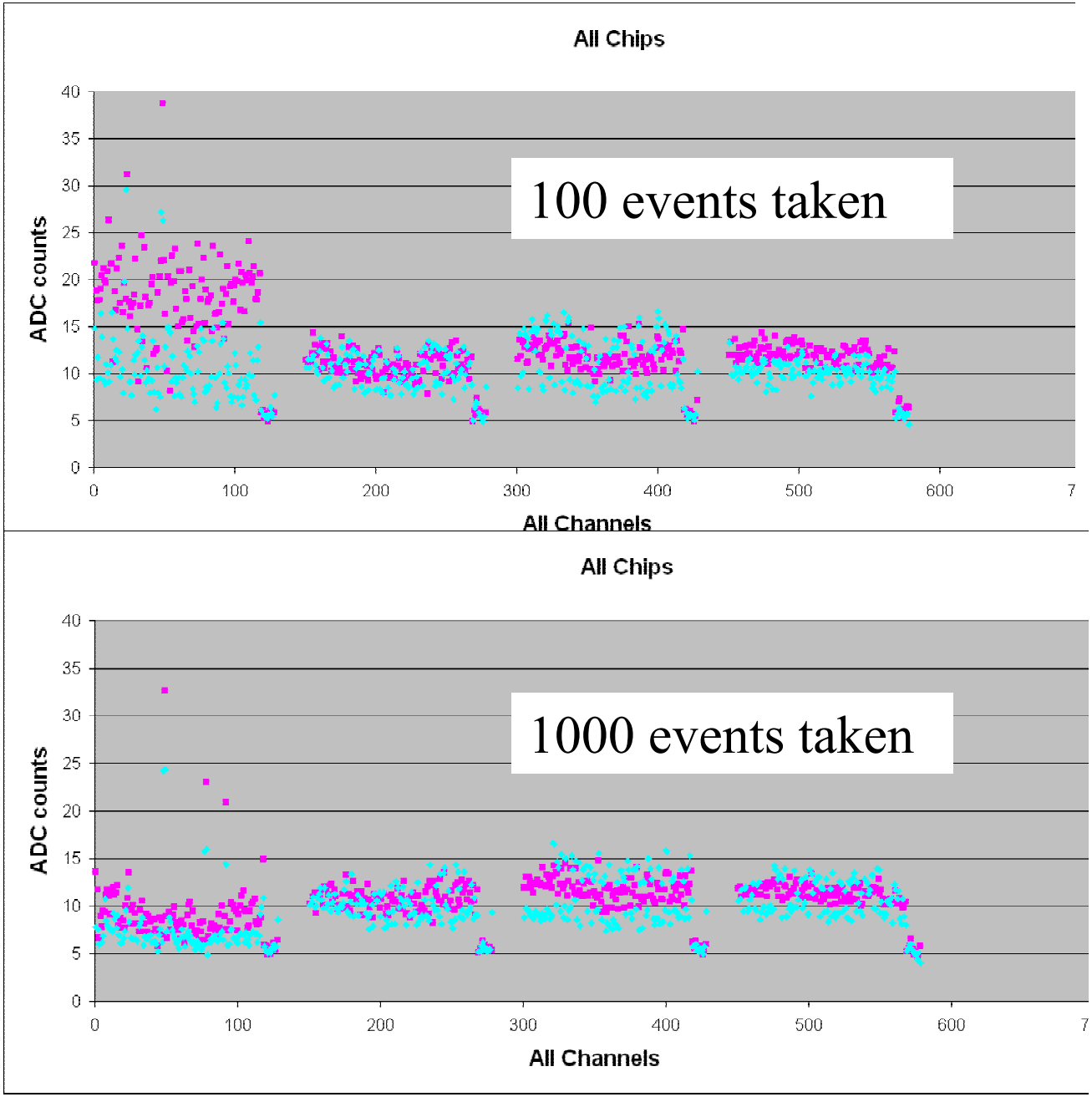
BW=15

- There is always high side tail.
- BW=0 unreasonable.

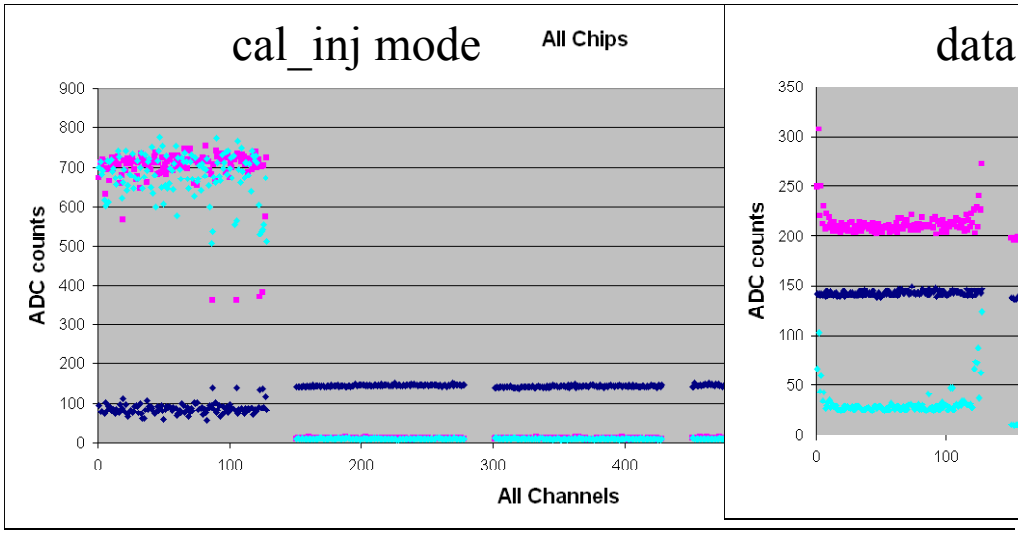
Misbehaviors 2 (w/ both cable and sensor)

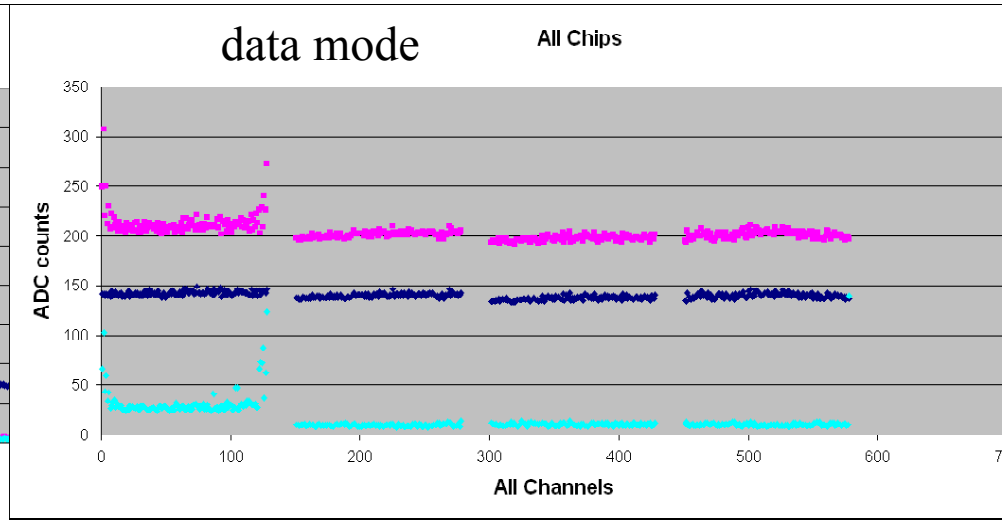


- A few first events always noisy.
- The rest is too less noisy.

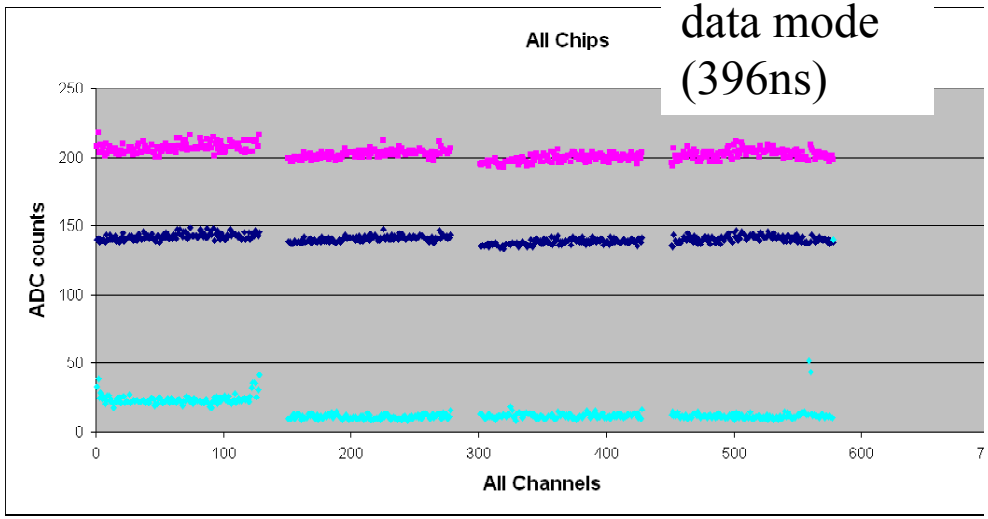

All Chips
ADC counts
All Channels
100 events taken
All Chips
ADC counts
All Channels
1000 events taken

Misbehavior 3 (by the older firmware)



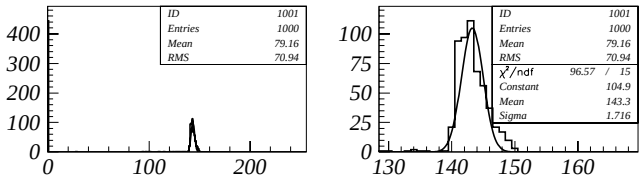


- There seems to be huge noise, but … (see next slide)

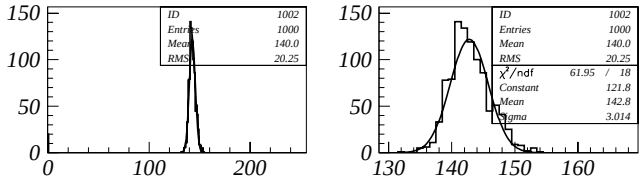


No ADC counts in data

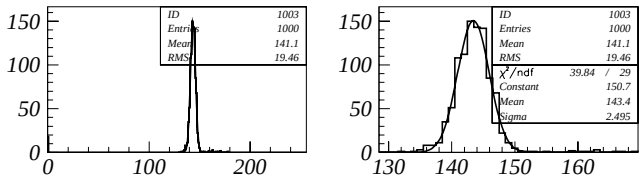
cal_inj mode

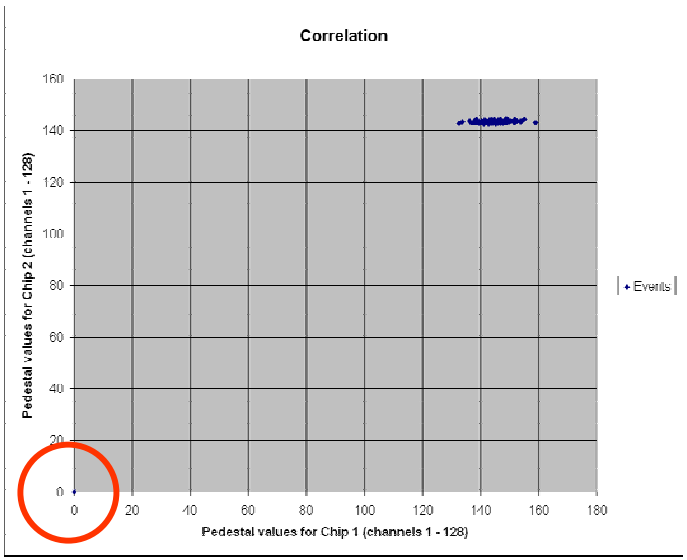


data mode



data mode (396ns)



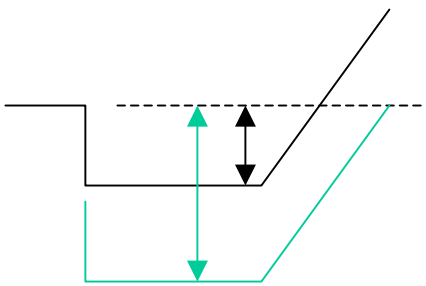


135.8671875	143.046875
152.21875	143.28125
141.5	144.2109375
0	0
146.015625	144.5
145.390625	143.09375
144.0234375	143.890625
144.6875	-375
144.9531	59375
148.2421	40625
146.453125	143.1171875
140.4609375	144.6484375
143.6875	143.4375
141.875	144.0078125
144.1015625	143.765625
145.296875	143.375
144.9609375	143.75
145.1328125	143.1875
141.9453125	143.0703125
0	0
149.140625	143.203125
155.1796875	143.2734375
139.96875	142.75
0	0
142.296875	144.0078125
147.4765625	143.46875

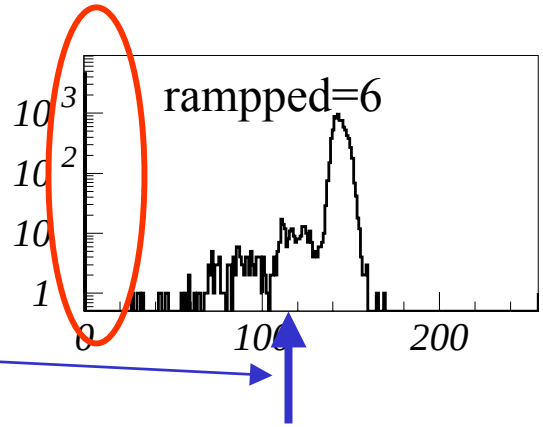
Avg. of chip 1 & 2

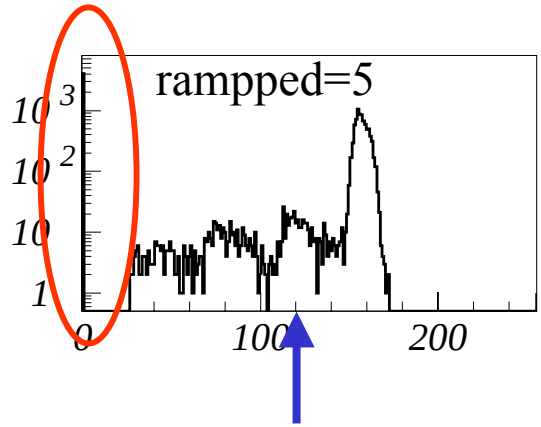
Pedestal Shape (cal_inject mode)

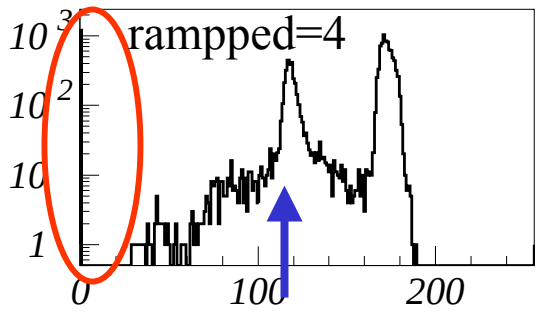
Lower limit of ADC counts in usual condition

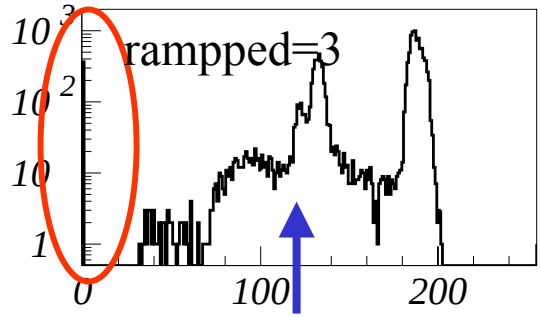


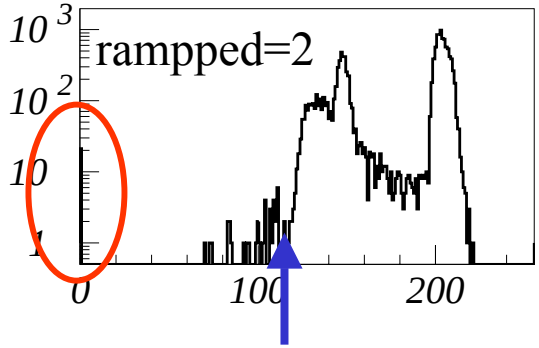
- Note the fraction of zero.

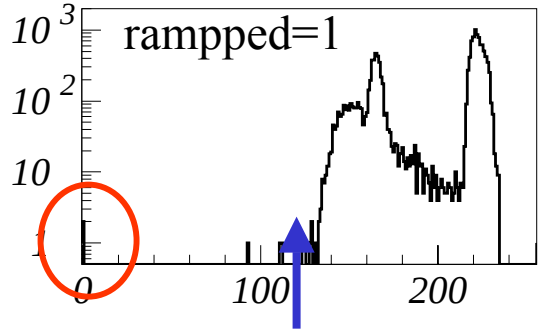




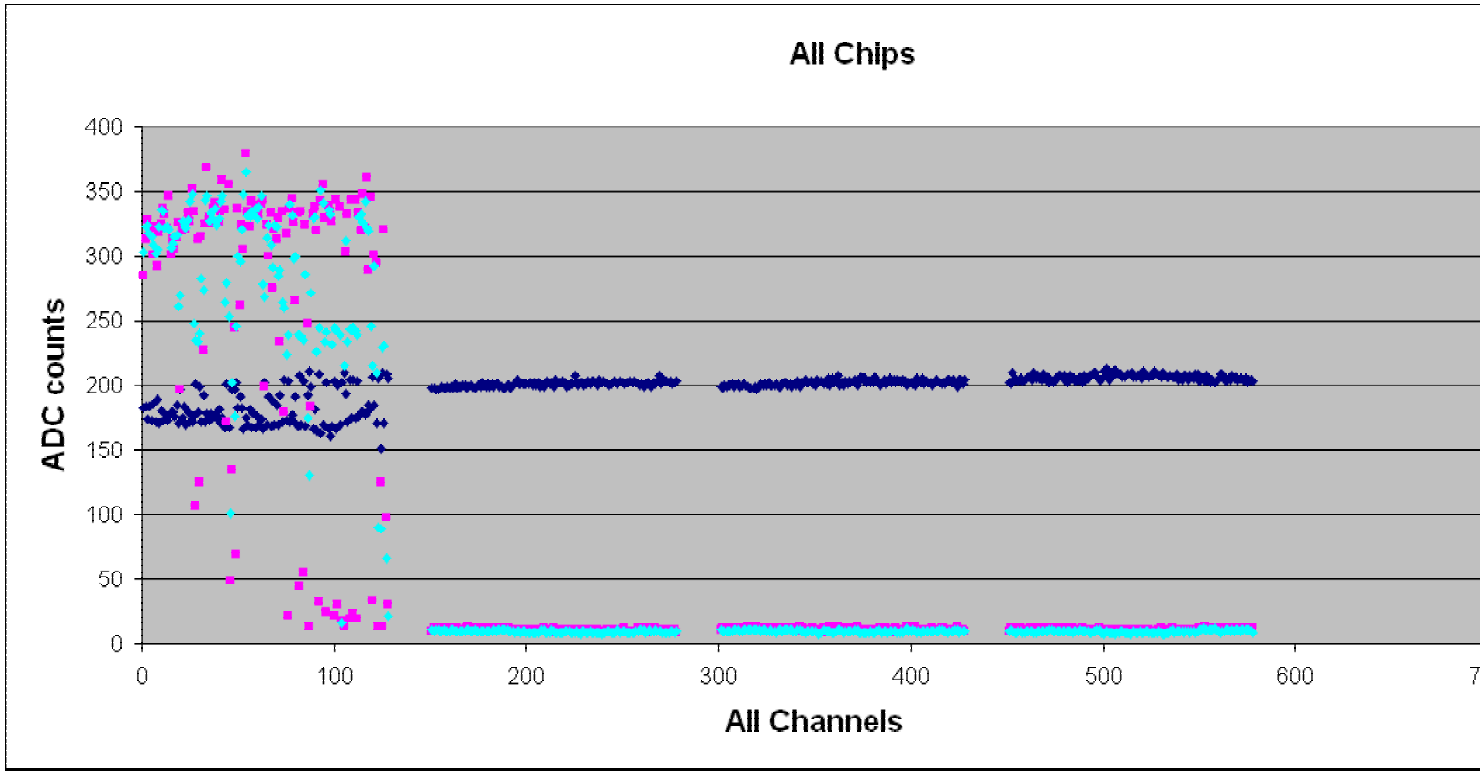






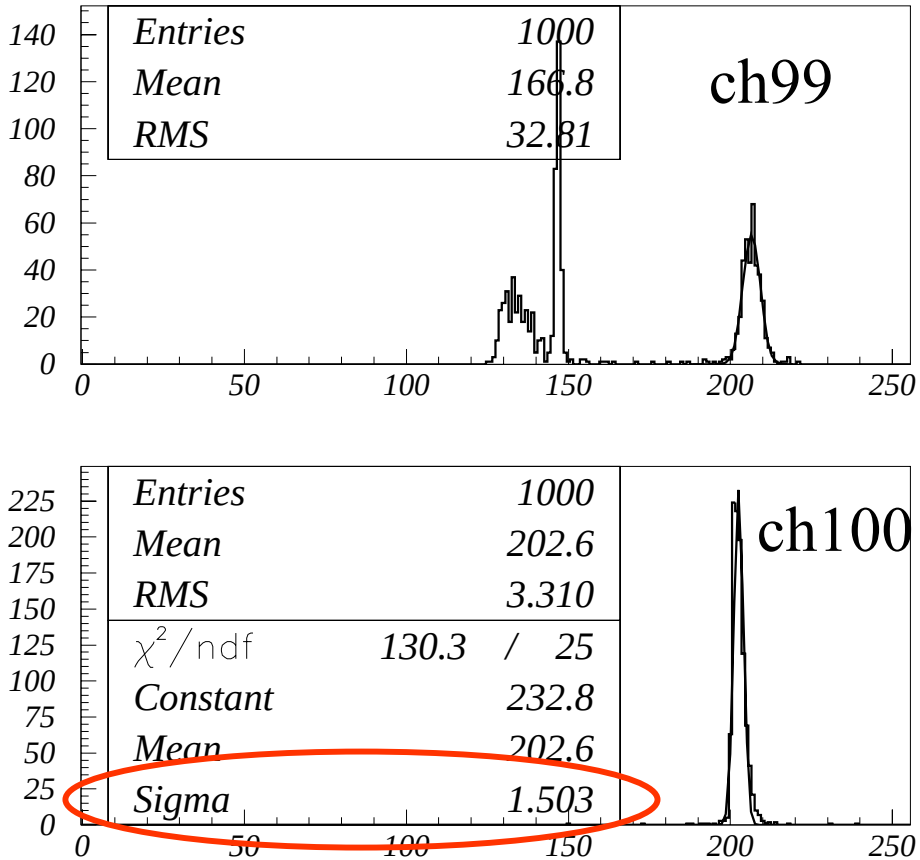


Even Odd Effect?



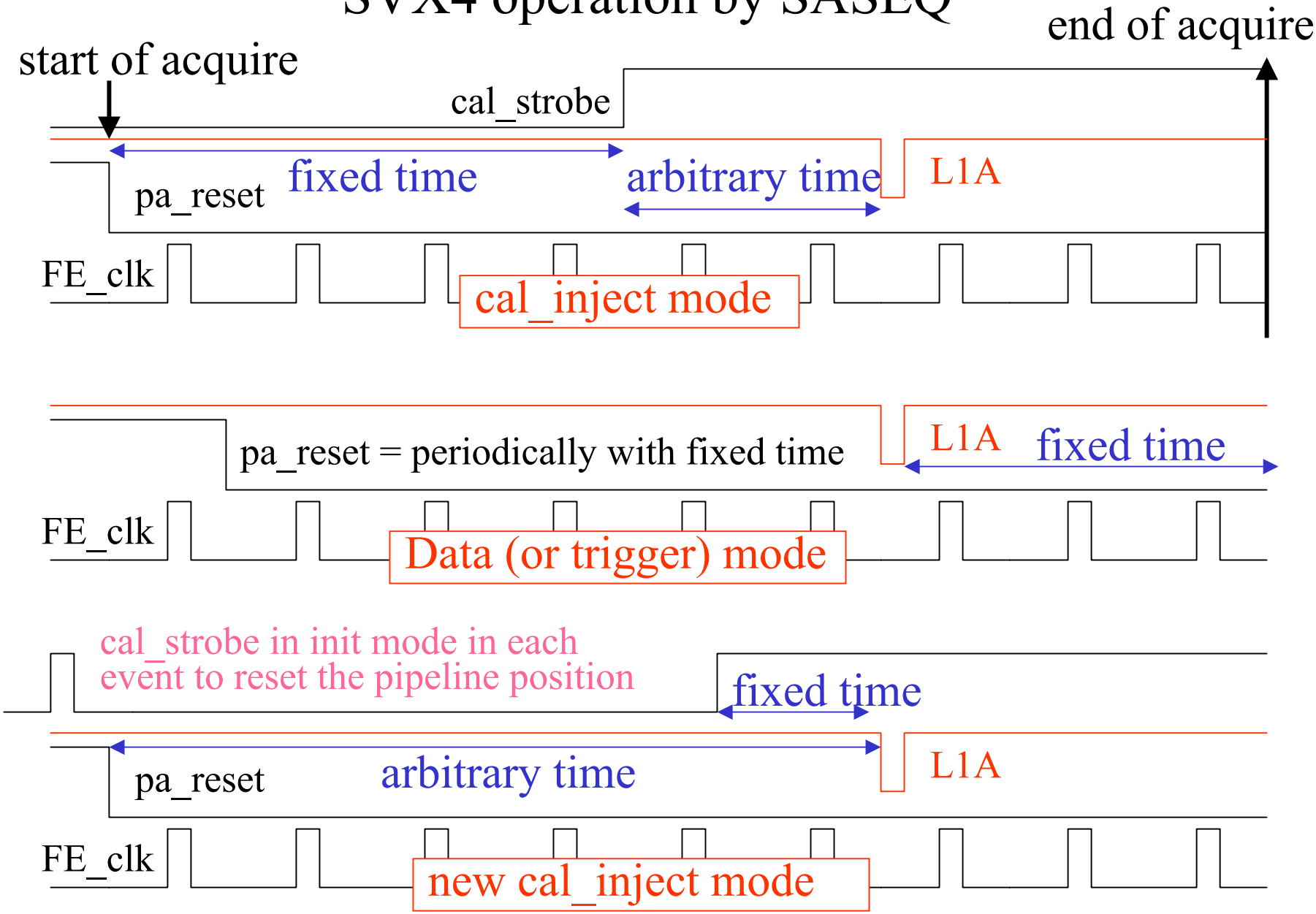
- The fraction of ADC=0 events differs between even and odd channel. → next page.

Raw ADC distributions



- Be careful to study noise. RMS is not enough to catch a real noise effect. ➔ always better to look at raw ADC distributions.

SVX4 operation by SASEQ



Summary

- L0/L1 module prototype testing in progress.
- Noise due to capacitive load by the analog cable is as expected. Capacitance ~ 16pF in the setup.
- Noise issue which might be related to preamp reset or other failure in the control sequence.
- Some misbehaviors. ← mishandling of control sequence?
- More works give us more puzzles/mystery…