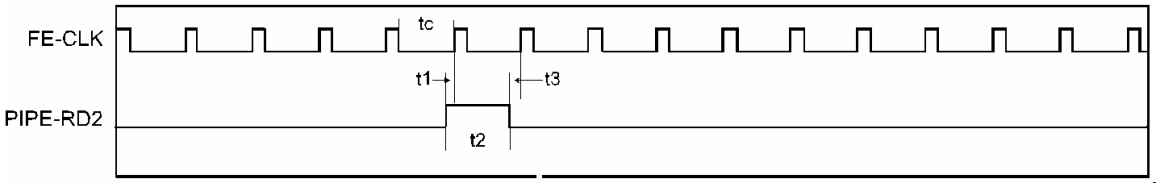
SB1W4
Applies to all wedges with the 37 nsec wide FECLK

1. All resistance measurements are OK. Do not ask me the numbers because they are NOT relevant.
2. Measured the Signals out of the FTM on the FIB timing cable with the break-out board. We found out something that we should have known already. This is a FIB with the ISL FECLK modification so the FECLK HIGH is 37 nsec wide instead of the original 27 nsec. The extra 10 nsec are added to FECLK HIGH before the rising edge.

As a consequence we are building a theory that could explain the STUCK LADDER behavior that has been bothering us for a while and potentially the source of a few broken DVDD Jumper connections.
I'm pasting in here part of the SVX3d DEVICE SPECIFICATION as written up in *Document # ESE-SVX-950703* back in 1996.

6) Reference Pipeline Reset



Parameters		Minimum	Maximum
PIPE-RD2↑ to FE-CLK↑	**t1**	**5 ns**	**tc - 5 ns**
PIPE-RD2 pulse width	**t2**	**???**	
PIPE-RD2↓ to FE-CLK↑	**t3**	**5**	**tc - 5 ns**

The reference pipeline reset must occur each time after the digitization is completed.While pipe-rd2 is high the write amplifier is connected to the reference cell so no data can be acquired but the pipeline cell pointer is still advanced. Because of this the pipe-rd2 should occur at a time when no data is present at the chip input. The pipeline cell, which has been digitized, is put back into the cell at the first clock after the falling edge of PIPE-RD2.

Let's now take a look at the timing of FECLK wrt PRD2 as measured with the break-out board at the FTM FIB timing cable. Figure 1 shows the relative timing for SB1W4 where there is a ISL-flavor-FIB installed while Figure 2 is taken from SB0W4 where the modification hasn't been applied

yet. In Figure 1 the cursors are measuring 6.4 nsec while in Figure 2 it is 14.8 nsec. With the ISL-flavor-FIBs we might be marginal on this delay. This theory is supported by:

1. The fact that the STUCK LADDER problem is more frequent in ISL than in SVXII.
2. Missing a PRD2 is quite similar to send a 5th L1A and we all know that the symptoms associated with the 5th L1A are STUCK CELL ID and HIGH OCCUPANCY on the N-side as we unfortunately experienced during RUN # 150948. Some bench studies supported this as can be seen in the following URL:

http://www-cdfonline.fnal.gov/cgi-bin/det-system-elog.pl?nb=silicon&action=view&page=122&frame=2&anchor=18:53:00

Lester is now responsible to find out how to deal with the problem.

Hopefully we will be able to implement a tested solution before the next store (Tuesday at midnight) so that we can have a few stores of data before the long shut-down and maybe declare the problem fixed before the shutdown itself. The approach is to choose the least labor extensive solution that can increase the time between the edges of the two signals. He is going to look at the system from the SRC down to the FFOs and then to the FIBs following the natural granularity of the system. Obviously if fixable at the SRC it will imply working on a single BOARD while if the work has to be done on the FIB we might have to deal with all 58 (+spares) of them. In conclusion it will be very good if:

- We work out the best possible solution to be tried as soon as possible on the bench first and then on the real system.
- We solve the problem in a time scale that is consistent with having feedback on the potential solution before the January shut-down starts

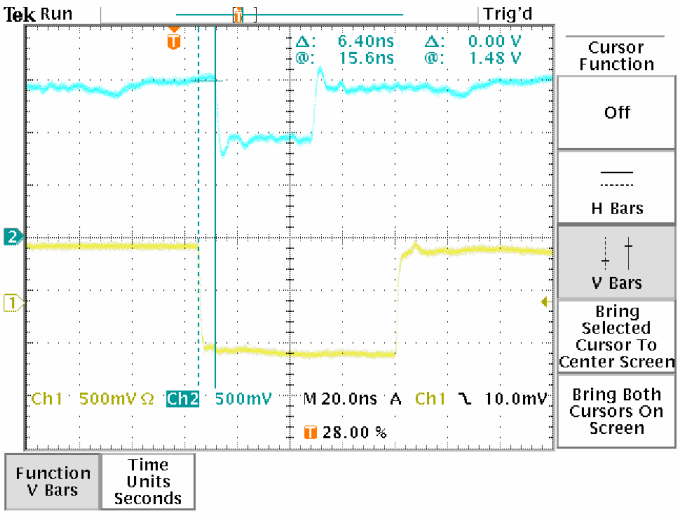


Figure 1. <u>SB1W4</u>. CYAN: FECLK+ measured with single ended probe. Yellow PRD2 measured with differential probe. SB1W5, SB2W8, SB0W6 are all similar to this picture.

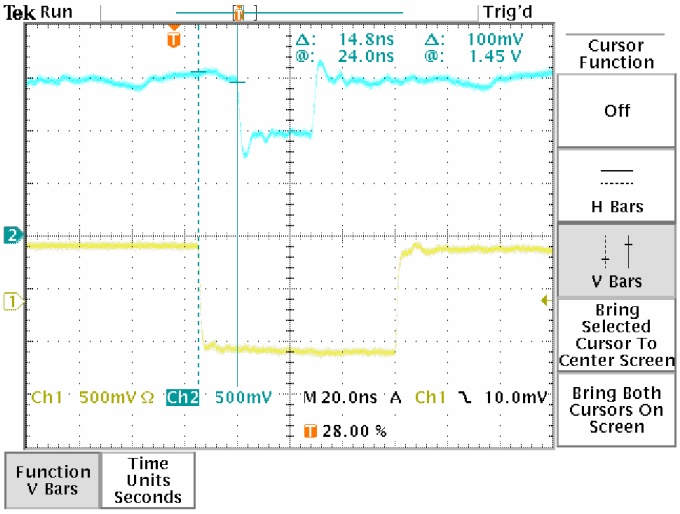


Figure 2. <u>SB0W4</u>. CYAN: FECLK+ measured with single ended probe. Yellow PRD2 measured with differential probe. SB0W5 is similar to this picture.