DØ Note 3213

Characteristics of 2sk369 Junction Field Effect Transistor for Run 2 Calorimeter Preamplifiers

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1 Introduction

The 2sk369 junction field effect transistor (jFET), built by Toshiba [1], will be used to form the input stage of the calorimeter preamplifiers for Run 2. The jFET acts as a low noise transconductance device and provides high open loop input impedance [1]. One of the factors that determines the open loop gain and the closed loop input impedance of the preamplifier is the value of the jFET transconductance at the bias point. We present measurements of the output and transfer characteristics of the 2sk369 transistor.

2 Model of jFET in Saturation Regime

A jFET consists of a conducting doped silicon channel between two terminals, usually called source (S) and drain (D). Along the length of this channel, a diode is constructed where the source or drain act as the first terminal of the diode. The second terminal of the diode forms the gate (G), which becomes the third terminal of the jFET.

During operation as a transistor, the potential difference applied between the gate and the source/drain is such that the diode is reverse-biased. Hence the depletion region of the diode, where no free carriers are available to

[1] Two jFETs will be used in parallel to reduce the intrinsic preamplifier noise by a factor of $1/\sqrt{2}$ for the same gain.

conduct current, extends into the conducting silicon channel between source and drain. By varying the gate voltage, the resistance of the S-D channel, and therefore the S-D current, can be controlled, providing transistor action.

For large drain currents, the potential drop between source and drain causes the voltage between gate and source (or drain) to become sufficiently large to "pinch-off" the conducting channel. This means that the depletion region extends all the way across the width of the channel, leaving no conducting region. This is called the saturation regime. In this situation, conduction proceeds through the pinched-off part of the channel by a different mechanism.

A useful property of the jFET in the saturation regime is that the source-drain current (henceforth referred to as drain current or I_D) is weakly dependent on the drain-source voltage (henceforth referred to as drain voltage or V_{DS}), and controlled mostly by the gate-source voltage (henceforth referred to as gate voltage or V_{GS}). The jFETs in the preamplifier will be biased to operate in the saturation regime. The gate acts as the input terminal. The gate voltage therefore controls the preamplifier output. Since the gate is reverse-biased, the gate input current is very low.

In the saturation regime, it has been found experimentally that the following relationship closely approximates the drain current [2]

$$I_D = g_0^2 (V_{GS} - V_T)^2 \tag{1}$$

where g_0 and V_T are parameters (V_T is generally referred to as gate threshold voltage). The transconductance g_m is defined as

$$g_m = \partial I_D / \partial V_{GS} \tag{2}$$

and is a function of I_D.

3 Measurement Apparatus

We use the Tektronix 576 Curve Tracer to measure I_D as a function of V_{DS} and V_{GS} for a number of jFETs. A schematic of the curve tracer is shown in figure 1. Curves of I_D *vs* V_{DS} are plotted for V_{GS} changed in 50 mV steps on an oscilloscope display. Photographs of these curves for a number of devices are shown in figure 2. For a given gate voltage, the drain current increases rapidly with increasing drain voltage initially. This is the linear or sub-saturation region. As drain voltage keeps increasing, saturation is achieved and the curves flatten out, the drain current showing much reduced dependence on the drain voltage. The saturation current then increases with increasing gate voltage, the different curves corresponding to different gate voltage settings differing by 50 mV. The horizontal scale is 1 V/div and the vertical scale is 1 mA/div.

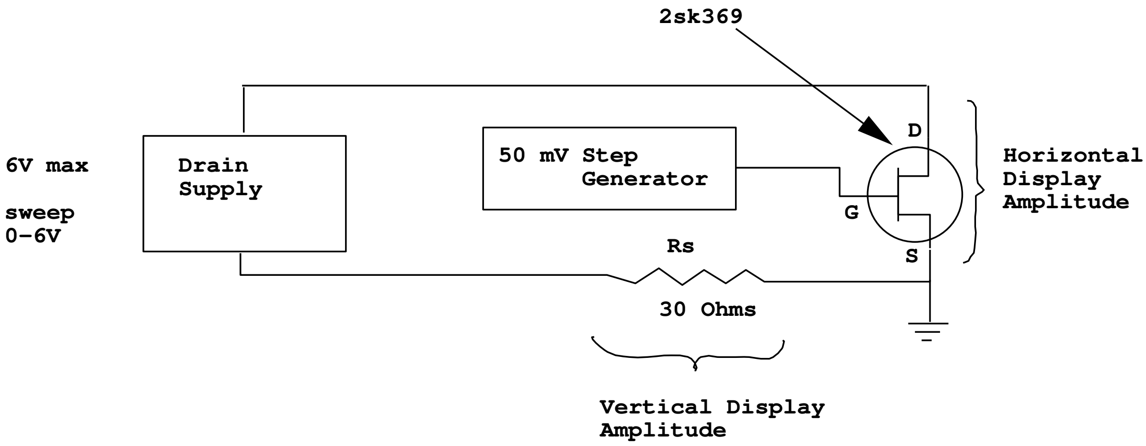

Figure 1: Schematic of the Tektronix 576 Curve Tracer.

The biasing conditions of the transistor in the preamplifier are reproduced for the second curve from the top. For this curve, $I_D = 6$ mA @ $V_{DS} = 5.3$ V. For each device-under-test, this condition is achieved by tuning the offset of the gate voltage generator, which accomodates the variation of g_0 and V_T from device to device.

4 Results

We first make measurements on a sample of 2sk369v transistors, an earlier version manufactured by Toshiba. We record I_D @ $V_{DS} = 5.3$ V for the five

Figure 2: Photographs of the Tektronix 576 Curve Tracer oscilloscope display showing curves of I_D vs V_{DS} for V_{GS} varying in steps of 50 mV.

values of V_{GS}. We then fit $\sqrt{I_D}$ as a linear function of V_{GS}, where we have arbitrarily set the lowest value of V_{GS} to zero. The fits for this sample are shown in figures 3, 4, 5 and 6. An error of 0.05 mA in the drain current readings is assigned. The fits show that equation 1 describes the behavior of the jFETs in saturation very well. The fitted slopes, which measure the g_0 parameter, are histogrammed in figure 7. We find a mean value for g_0 of 9.3×10^{-3} $\sqrt{\text{mA}}/\text{mV}$ with an r.m.s. of 2.8×10^{-4} $\sqrt{\text{mA}}/\text{mV}$ for 34 devices. From this value of g_0, and using equations 1 and 2, we obtain the mean $g_m(@I_D = 6\text{ mA})= 45.4\text{ m}\Omega^{-1}$ with an r.m.s. spread of $1.4\text{ m}\Omega^{-1}$.

Since g_m is linearly related to the gate voltage, we can also calculate it for a drain current of 6 mA by taking the second difference of the drain current *vs* gate voltage measurements. The distribution of g_m measured this way, using a second set of readings on the same sample of 36 2sk369v jFETs, is shown in figure 8. The mean value of $g_m(@I_D = 6\text{ mA}) = 44.6\text{ m}\Omega^{-1}$ with an r.m.s. spread of $1.4\text{ m}\Omega^{-1}$ is obtained, consistent within binning errors of the first method [2].

We perform the latter measurement for a sample of 40 2sk369gr jFETs, which is the version of the transistors we will use for building the Run 2 preamplifiers. The distribution of $g_m(@I_D = 6\text{ mA})$ is shown in figure 9. The mean value of $g_m(@I_D = 6\text{ mA}, V_{DS} = 5.3\text{ V}) = 45.6\text{ m}\Omega^{-1}$ with an r.m.s. spread of $0.87\text{ m}\Omega^{-1}$ is obtained for this sample.

The tuning of the gate voltage generator offset needed to bias all the test devices identically gives us an idea of the spread in the threshold voltage from device to device. For a subset of the 2sk369gr devices measured, we recorded the magnitude of the change in the offset from one device to the next. A histogram of these variations is shown in figure 10. Variations in the threshold voltage lead to variations in the preamplifier first stage output bias voltage. As figure 10 shows, the variation is on average 20 mV, while differences of 50 mV between two jFETs can occur.

Finally, we measure the output conductance of one transistor, defined as $\partial I_D/\partial V_{DS}$ in saturation, from the slope of the flat part of the curves shown in figure 2. The output impedance, defines as $\partial V_{DS}/\partial I_D$, is measured to be 14 k$\Omega$ for the 2sk369v and 13 kΩ for the 2sk369gr, for $I_D = 6$ mA and $V_{DS} = 5.3$ V.

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[2]The second method does not suffer from binning errors.

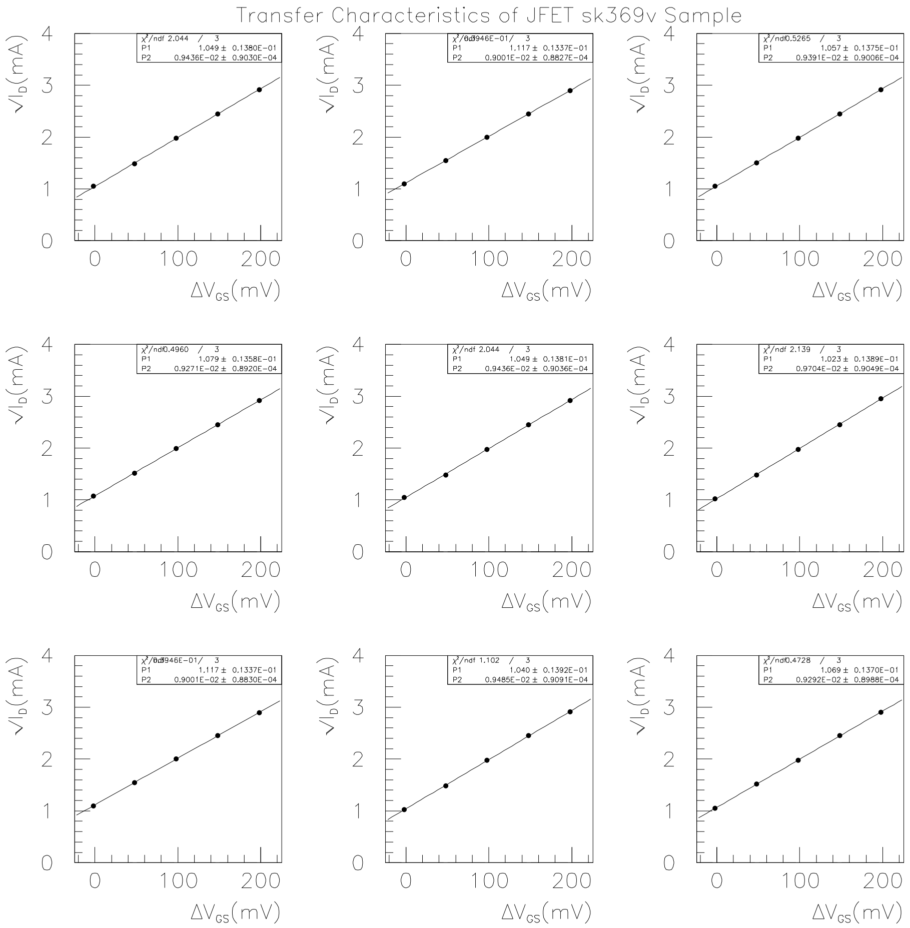

Figure 3: Linear fits to $\sqrt{I_D}$ *vs* ΔV_{GS} data for a sample of 2sk369v jFETs.

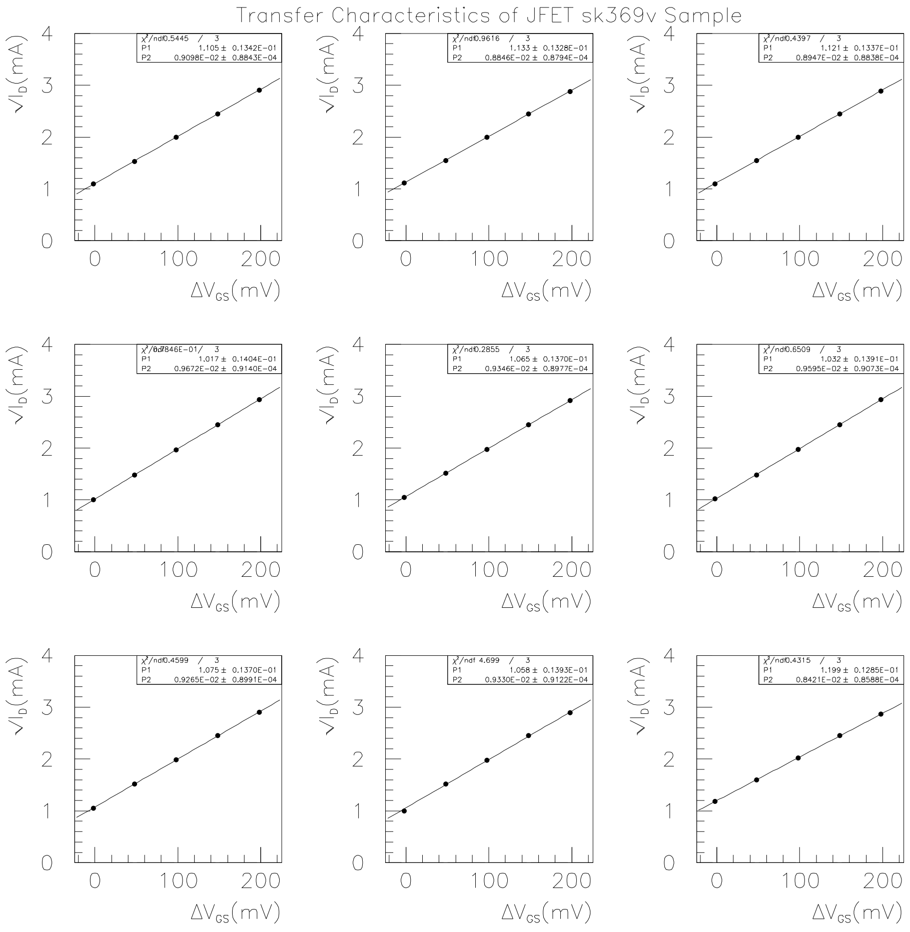

Figure 4: Linear fits to $\sqrt{I_D}$ *vs* ΔV_{GS} data for a sample of 2sk369v jFETs.

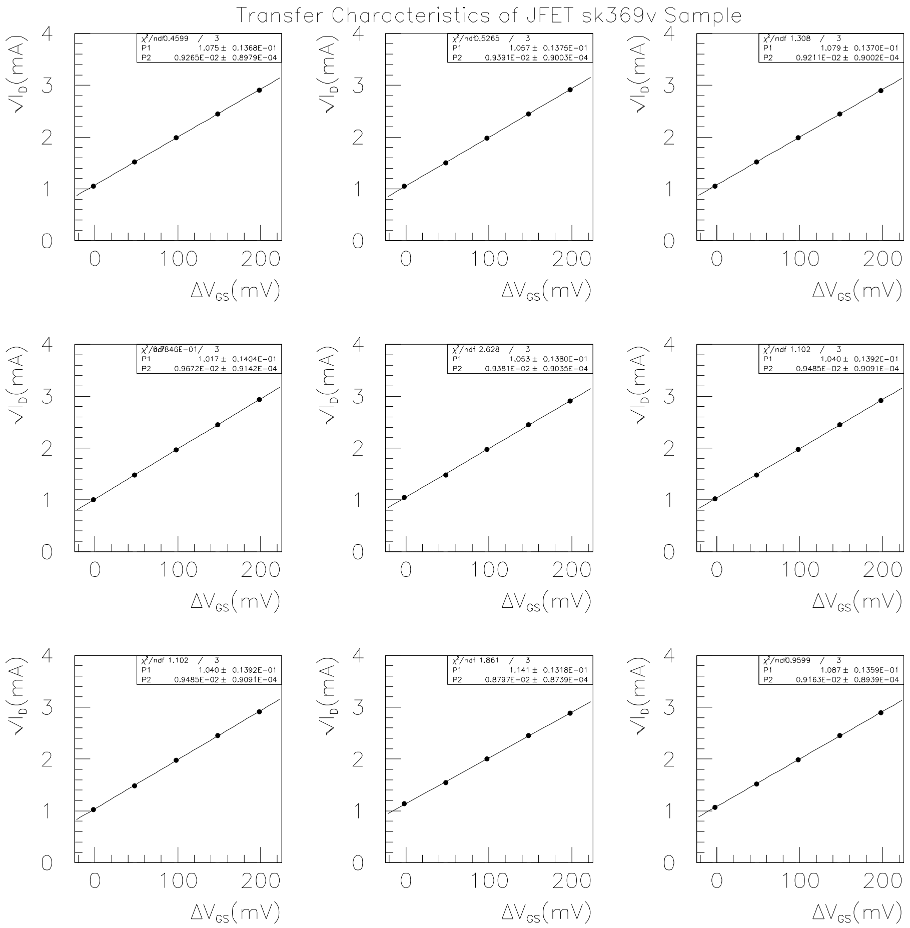

Figure 5: Linear fits to $\sqrt{I_D}$ *vs* ΔV_{GS} data for a sample of 2sk369v jFETs.

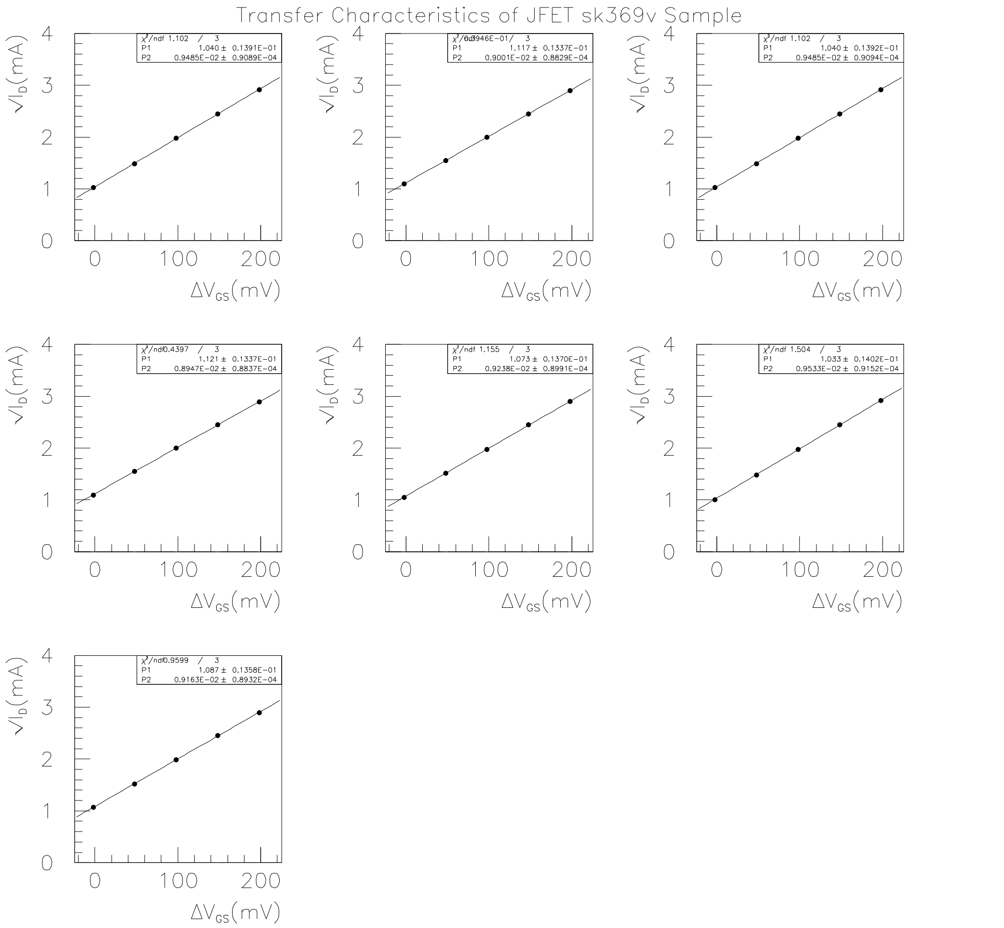

Figure 6: Linear fits to $\sqrt{I_D}$ *vs* ΔV_{GS} data for a sample of 2sk369v jFETs.

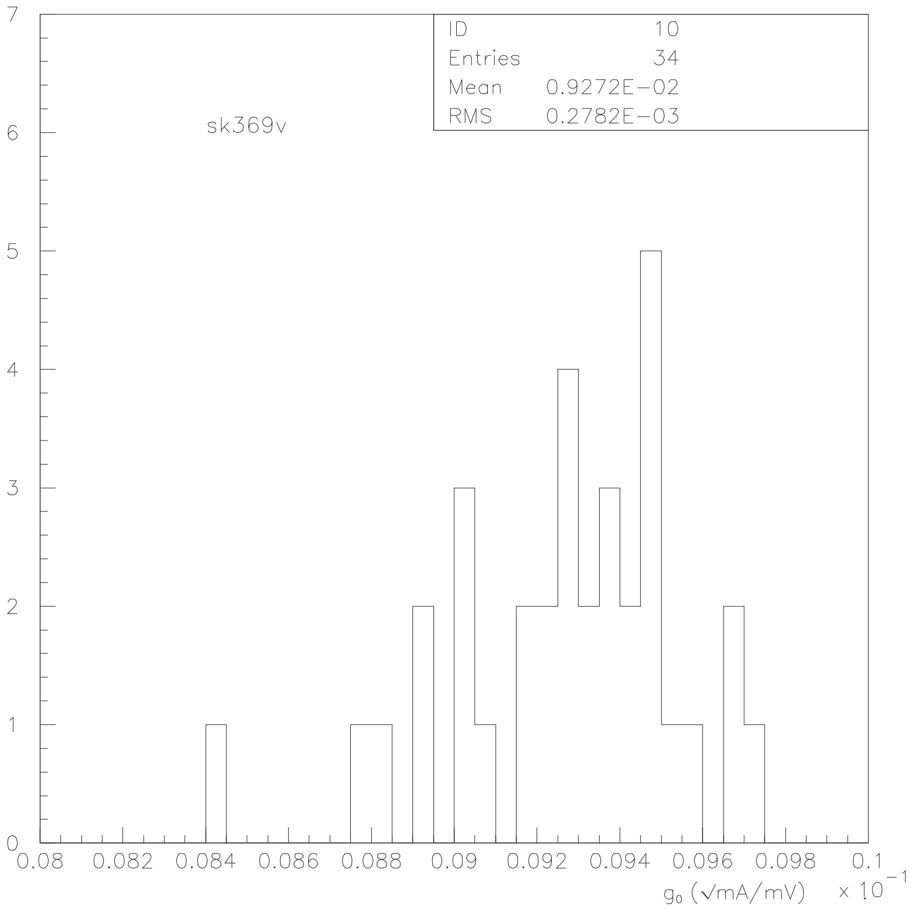

Figure 7: Proportionality parameter g_0 extracted from the linear fits to $\sqrt{I_D}$ *vs* ΔV_{GS} data for a sample of 2sk369v jFETs.

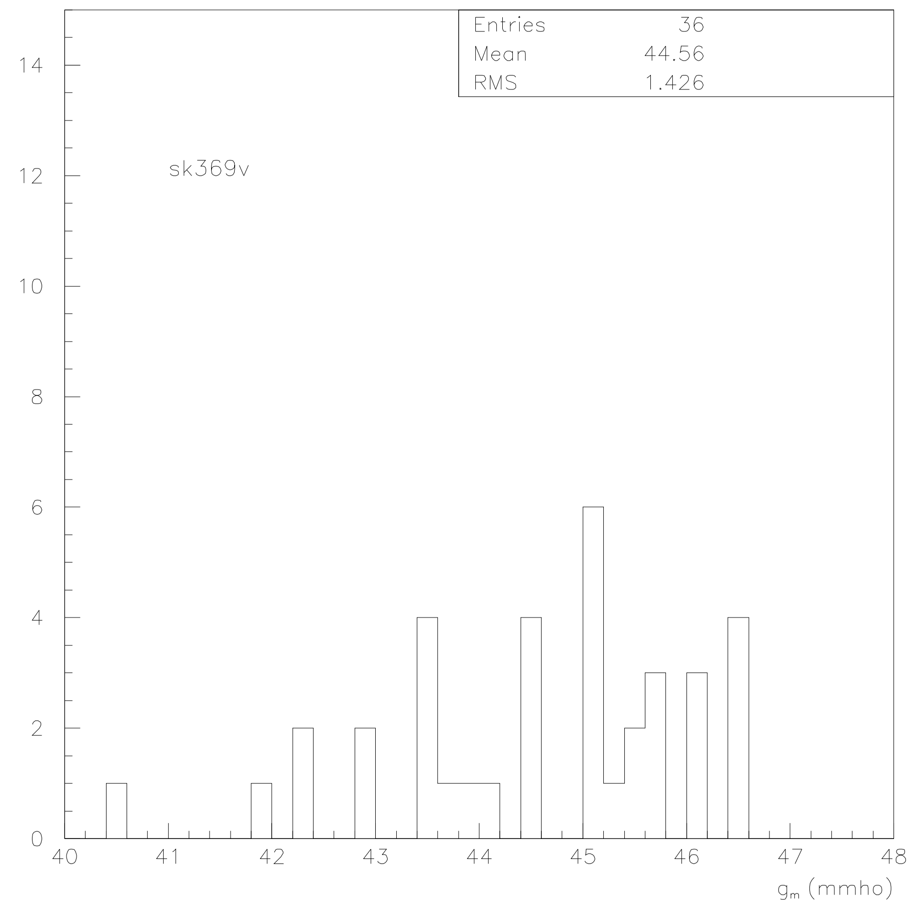

Figure 8: Transconductance measurements for a sample of 2sk369v jFETs, @I_D =6 mA and V_{DS} = 5.3 V.

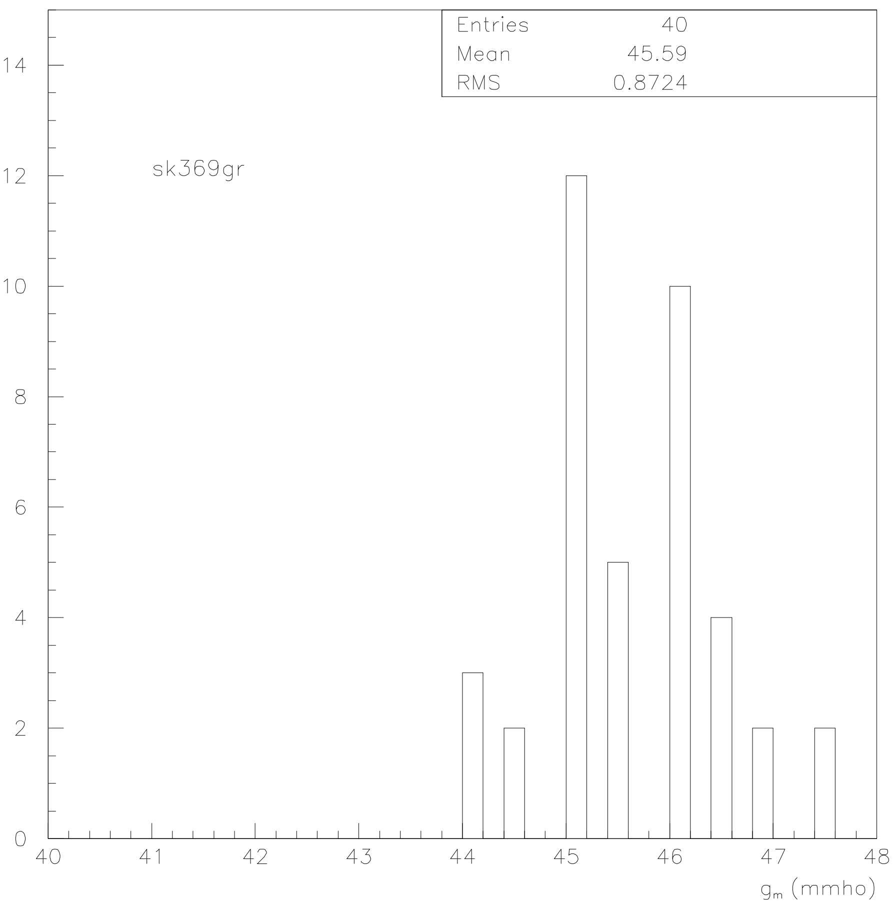

Figure 9: Transconductance measurements for a sample of 2sk369gr jFETs, @I_D =6 mA and V_{DS} = 5.3 V.

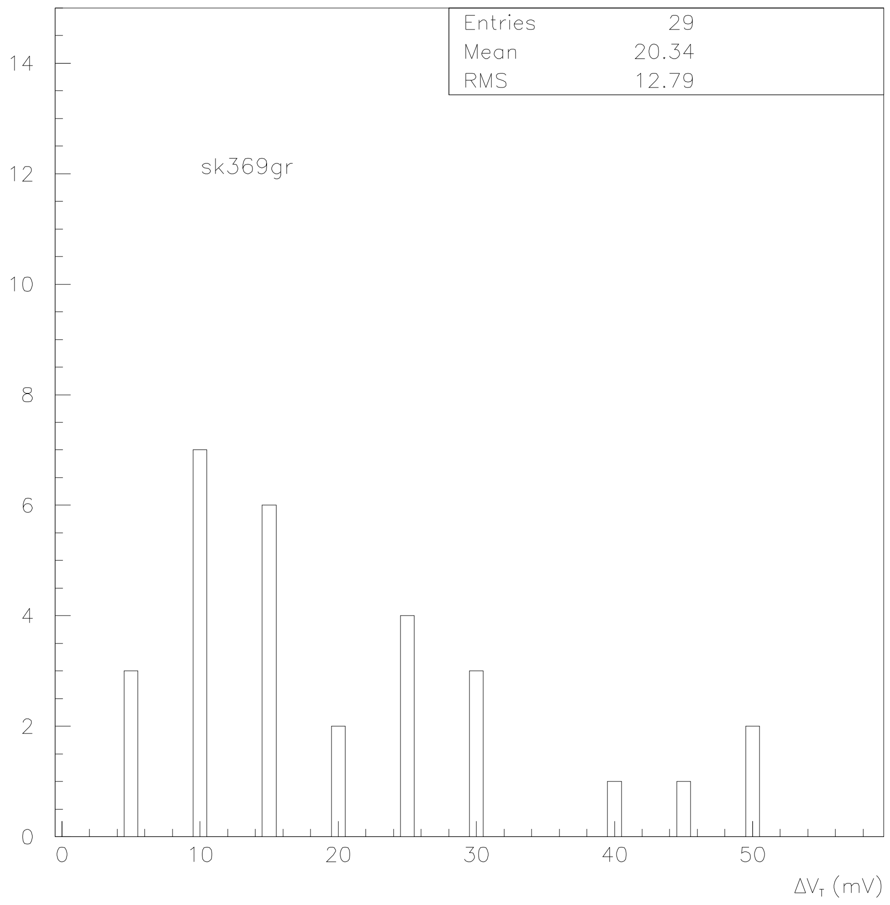

Figure 10: Magnitude of the device-to-device variation in the gate threshold voltage for a sample of 2sk369gr jFETs (measured to the nearest 5 mV).

5 Conclusions

The Toshiba 2sk369 junction field effect transistor will be used to form the input of the calorimeter preamplifier in Run 2. The transistor will be biased with a drain current of approximately 6 mA and drain voltage of approximately 5.3 V. Under these conditions, the jFET transconductance is measured to be 45.6 mΩ^{-1}. The drain current is proportional to the square of the gate voltage above threshold. The drain-source impedance is measured to be 13 kΩ. The device-to-device variation in the gate threshold voltage is on average 20 mV.

References

[1] Please see attached specifications provided by Toshiba, kindly obtained by Lynn Bagby.

[2] Ben G. Streetman, *Solid State Electronic Devices,* second edition, Prentice-Hall, Inc. (1980).