Firmware-only Implementation of Time-to-Digital Converter (TDC) in Field-Programmable Gate Array (FPGA)

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Abstract— A Time-to-digital converter (TDC) implemented in general purpose field-programmable gate array (FPGA) for the Fermilab CKM experiment will be presented. The TDC uses a delay chain and register array structure to produce lower bits in addition to higher bits from a clock counter. Lacks of direct controls that custom chip design has, the FPGA implementation of the delay chain and register array structure must solve two major problems: (1) The logic elements used for the delay chain and register array structure must be placed and routed by the FPGA compiler in a predictable manner, which directly affect the uniformity of the TDC binning and short-term stability. (2) The delay variation due to temperature and power supply voltage must be compensated to assure the long-term stability. We use the chain structures in the existing FPGA that the venders designed for general purpose such as carry algorithm or logic expansion to solve the first problem. To compensate the delay variation, we have studied several digital compensation strategies that can be implemented in the same FPGA device. Some bench top test results will also be presented in this document.

***Index Terms*—Front End Electronics, TDC, FPGA, Firmware**

I. Introduction

THE Fermilab CKM experiment is proposed to measure branching ratio of $K^+ \rightarrow \pi^+ \nu\nu$ events. The experiment uses continuous kaon beam and detects decay products. Time-to-digital converters (TDC) are used on all channels to measure the arrival time of hits come from the charged decay products. The binning size required is 1 ns. The experiment also requires that the TDC device must have no intrinsic dead time.

There are many motivations of using general-purpose field-programmable gate array (FPGA) to implement the TDC without using any external circuits. In the FPGA, a counter keeps clock count as the higher bits of the input time, which provides a coarse measurement accurate to a clock cycle. The lower bits that represent finer measurement beyond the clock cycle are generated in a delay chain and register array structure, as in many previous custom designed TDC devices. (See Fig. 1)

To implement the delay chain and the register array in FPGA, one must solve two major problems:

1. In the FPGA development software, a logic cell can be physically placed in nearly any place depending on the optimization algorithm the software uses. The routing may also be unpredictable to the user. If the logic cells used for the delay chain and register array are placed and routed in this fashion, the propagation delay of each delay step will not be uniform. One could certainly place and route these logic cells manually, but that would be very time consuming. So a methodology to control the physical location and routing automatically is thus demanded.
2. The logic cell delays will vary with temperature and power supply voltage. In many applications such as serial communication and custom designed TDC, a reference voltage is adjusted to make the compensation. But in FPGA, digital compensation method that needs no extra external circuits is more attractive than analog compensation.

In this document, we will discuss these two problems in detail and we will also present results from bench top tests.

II. Primary Strategies

A. Using Existing Chain Structures

In the FPGA available today, there exist chain structures that the vendors designed for general-purpose applications such as carry algorithm or logic expansion. These chain structures provide short predefined routes between identical logic elements. They are ideal for TDC implementation. We have used the "cascade" chain structure originally for the fast logic expansion in the Altera ACEX 1K devices for our TDC bench top tests.

B. Digital Compensation

The delay time of the logic element may vary with temperature and power supply voltage. However, the input

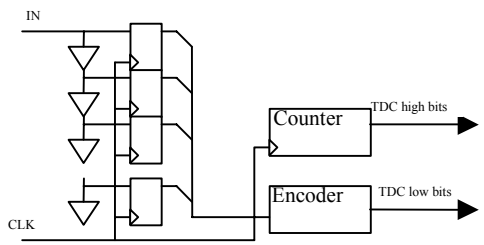

Fig. 1. The TDC implemented in FPGA. The delay chain and register array structure provides fine time measurement.

clock provides a known and stable period that can be used as an on chip timing standard. To make use of this timing standard, one can implement the delay chain with total propagation time longer than the clock period. With this longer delay chain, some input signals being registered by a clock edge can be registered again by the next clock edge. The separation of the two registered points reflects propagation speed of the input signal in the delay chain at certain temperature and power supply voltage. From this information, one can calibrate the delay chain speed and make the compensation to the TDC output result.

III. Bench Top Test Results

We have used the "cascade" chain structure in the Altera ACEX 1K devices (EP1K10QC208-1 and -2) for our TDC tests. The "cascade" delay chain that we used in our tests had 48 steps. Each step in the chain fed into a D type flip-flop register of the same logic element. The clock frequency we used in the tests was 70 MHz. The leading edge caught by the register array was encoded and sent out every clock cycle.

A. TDC Uniformity and Short-Term Stability

Fig 2 shows a test result of the TDC output as a function of the signal input time. The input signal was derived from the system clock and its arrival time was changed by adjusting the length of delay cable. About 570 measurements were made for each point and the means of the measurements were plotted. One can see from the plot that the least significant bit (LSB) bin size of the TDC for the cascade chain of this device is 0.47 ns. One would also expect some non-uniformity due to internal layout structure of the device. However, even without using any knowledge about the device structure, a simple linear fit matches the measurement points better than 1 LSB.

To understand short-term stability, the standard deviations of the measurements were calculated and plotted in Fig 3. The x-axis is the fractional portion of the TDC mean. If the arrival times of the measurements for one input delay were centered to one TDC bin N, the fractional portion of the TDC mean would be 0. If, on the other hand, the arrival times were centered in the middle of two adjacent TDC bins N and N+1, this value would be 0.5, and at this point, the standard deviation contributed purely by binning would be 0.5 LSB. One can see that the measured standard deviation can be explained by this binning effect, and the contribution due to other sources is negligible. Therefore in this test device, the intrinsic short-term instability, if there was any, was significantly smaller than 0.5 LSB.

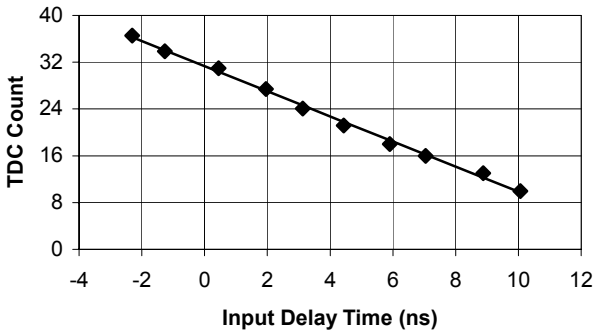

Fig. 2. TDC output as a function of the input time delay.

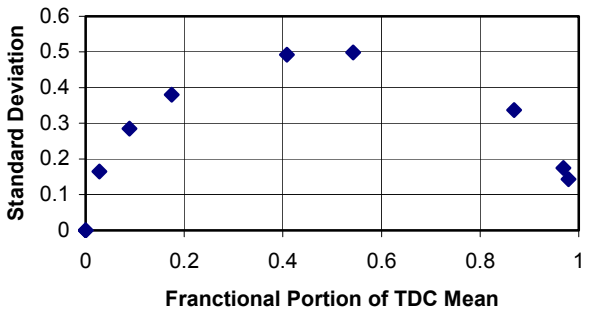

Fig. 3. Standard deviation plotted as a function of fractional portion of the TDC mean.

B. Digital Compensation for Long-Term Stability

A test was done to study the digital compensation method. Input signals with fixed arrival time relative to the system clock were fed into the TDC device. Each input signal was registered two times by two clock edges and hence produced two TDC numbers. We changed power supply voltage from 2.5 V to 1.8 V; both TDC numbers followed the change significantly. Note that the voltage range was artificially chosen to emulate the worst possible conditions.

From the two TDC numbers, one can calculate the delay chain speed. The speed at given condition can be averaged over multiple measurements to reduce the digitization errors. Using the delay chain speed information, the true delay time represented by the first TDC number can be calculated and the compensation can be made. Fig. 4 shows the two TDC numbers and the compensated time of the input signal. One can see that the variation of the compensated value is less than 1 LSB over the entire range.

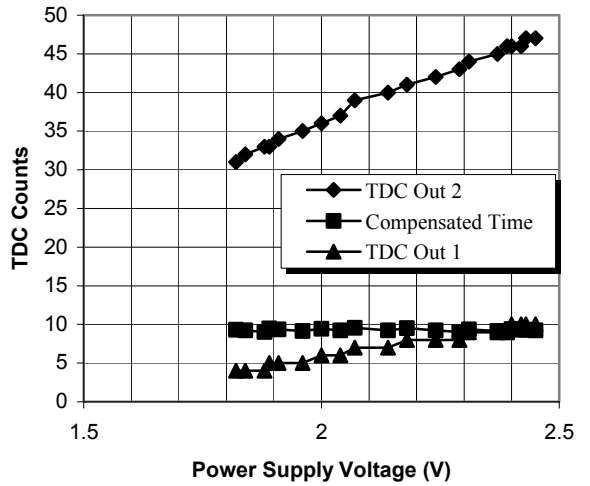

Fig. 4. TDC outputs vary with power supply voltage. The signal time compensated with digital algorithm is shown with square marker.